HIGHLY STABLE INTEGRATED RC-BASED FREQUENCY REFERENCES

BY

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DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois Urbana-Champaign, 2023

Urbana, Illinois

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ABSTRACT

Monolithic RC-based frequency references have been a viable alternative to traditional crystal or MEMS-based oscillators due to their low power consumption, compact size, and lack of requirement for costly off-chip components. However, their inferior frequency accuracy resulting from non-linear temperature sensitivity and aging has restricted their use to systems that can tolerate a frequency inaccuracy of ∼1%. There have been several attempts to improve accuracy and expand the use of these references to applications requiring medium to high stability clock sources. However, these efforts face challenges such as circuit-level imperfections, uncompensated high-order temperature coefficients (TCs), poor power efficiency, and the need for resistors with opposing TCs that may not be obtainable in all processes. Furthermore, despite some literature demonstrating a satisfactory short-term inaccuracy of less than ±600 ppm, their commercial deployment is restricted by the lack of information about their aging behavior and the inability to assure their performance over their lifetime.

First, this thesis presents power-efficient techniques to reduce the non-linear temperature sensitivity of fully-integrated CMOS RC oscillators and proposes methods for performing first- and second-order temperature compensation without the need for resistors with opposite TCs. Using the proposed three-point digital trim, a prototype 100-MHz frequency-locked loop (FLL)-based RC oscillator fabricated in a 65-nm CMOS process achieves an inaccuracy of ±140 ppm over −40 °C to 95 °C, 83-ppm/V voltage sensitivity, 1.3-ppm Allan deviation floor, and 1-μW/MHz power efficiency. When only a single-point trim is performed using multiple linear regression model obtained from strong correlation between three switched resistors, the frequency inaccuracy is ±587 ppm over −40 °C to 95 °C.

Second, in order to address the aging issue, this thesis proposes a temperature- and aging-compensated RC oscillator (TACO) in which the long-term drift of the main oscillator is compensated by periodically locking its frequency to that of the less-aged reference oscillator. A prototype 100-MHz FLL-based RC oscillator fabricated in a 65-nm CMOS process achieves an inaccuracy of ±1030 ppm from from −40 °C to 85 °C after 500 hours of accelerated aging at 125 °C, with 5.1-ps_{rms} period jitter and a power efficiency of 1.4 μW/MHz.

To my parents and my sister for their love and support.

ACKNOWLEDGMENTS

I would like to express my deepest gratitude to my advisor, Prof. Hanumolu, for his unwavering support and guidance throughout my Ph.D. program and research. Working under his supervision and being a member of his research group has been an exceptional privilege. He provided me with extensive knowledge, motivation, and patience, and helped me overcome the many obstacles and challenges I encountered in my research, writing papers, and this thesis. Prof. Hanumolu always had faith in my abilities and pushed me to exceed my own expectations, guiding me to develop my problem-solving, writing, and presenting skills. I am profoundly grateful for his kindness, generosity, and care, without which my research would not have been possible.

I would also like to extend my sincere appreciation to the members of the integrated circuits and systems group, specifically Yongxin Li, Nilanjan Pal, Ruhao Xia, Ahmed Abdelrahman, Tianyu Wang, Mahmoud Abdelwahab Khalil, and Mohamed Badr Younis, for their support and assistance throughout my research. They were not only my colleagues and teammates but also my friends, with whom I shared unforgettable experiences and many tape-outs. I learned a lot from them both technically and personally, and I will always be grateful for their contribution to my research.

Furthermore, I would like to express my gratitude to my committee members, including Prof. Rosenbaum, Prof. Shanbhag, Prof. Banerjee, and Prof. Zhou, for their invaluable feedback, direction, and encouragement.

Last but not least, I extend my deepest appreciation to my parents and sister for their unwavering love, support, and sacrifice. Their devotion has been a driving force in my life, and they have always been there for me in my darkest moments. Without their patience and unconditional support, I would not have been able to achieve this work.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Stable frequency references serve many essential purposes such as timekeeping for calendar functions often referred to as a real-time clock (RTC) and providing reference clock for radios, processors, and micro-controllers. These applications have different requirements for operating frequency and short/long-term frequency stability (jitter/Allan deviation). For instance, an RTC for Bluetooth Low Energy (BLE) requires a 32.768 kHz clock source with less than $\pm$500 ppm frequency inaccuracy operating under very stringent power consumption while BLE radios need high frequency, low-jitter reference clocks with less than $\pm$40 ppm accuracy across the entire operating temperature range. Additionally, an ever-growing demand for smaller form-factor devices mandates integration of such references on a single chip. While quartz crystal-based references can achieve the desired frequency accuracy, they are power inefficient, take a long time to startup, and occupy large area, and therefore incur a heavy penalty in terms of increased form factor. Therefore, there is a demand for techniques to implement power-efficient frequency references that can be fully integrated in a standard CMOS technology, maintain excellent frequency stability over a wide temperature range, and ensure their performance over their lifetime.

Integrated CMOS frequency references using on-chip time constants are becoming popular as potential replacements for bulky quartz crystal or MEMS-based oscillators. However, they all suffer from unfavorable tradeoffs between accuracy, power consumption, noise, and cost. For example, LC-based references can achieve excellent accuracy ($< \pm$200 ppm) [1–4], but consume significant power and occupy large area, especially when the output frequency is low ($<$ 100 MHz). References based on thermal diffusivity of bulk silicon [5] are shown to achieve sub-1000 ppm inaccuracy but require heaters that increase power consumption. On the other hand, RC time-constant based references occupy a small area and consume little power [6]. However, their poor frequency accuracy resulting from their non-linear temperature sensitivity and aging has limited their usage to systems that can tolerate large frequency

inaccuracy (∼1%). For instance, the non-linear temperature dependence of the resistor and comparator offset/delay limits the accuracy of open-loop RC relaxation oscillators, which further degrades significantly in the presence of voltage variations [7]. Furthermore, the long-term accuracy of RC oscillators can be significantly degraded by aging, with a drift of more than 5000 ppm.

Several efforts are underway to improve the accuracy of RC oscillators and extend their use to applications requiring medium to high stability clock sources. For example, closed-loop RC oscillators based on the frequency-locked loop (FLL) architecture [8] can decouple the trade-off between output frequency and comparator-induced errors and improve immunity to voltage perturbations. However, these efforts still face challenges such as circuit-level imperfections [9], large uncompensated high-order TC [10], poor power efficiency [11–14], or the need for resistors with opposing temperature coefficients (TCs) [10] that may not be available in all processes. Additionally, even though some literature have demonstrated a good short-term inaccuracy of less than ±600 ppm [9–16], their commercial deployment is limited by the lack of information about their aging behavior and the inability to guarantee their performance over their lifetime.

Given the foregoing drawbacks, this thesis presents techniques that address the challenges faced by current approaches in maintaining accuracy and power consumption. Specifically, this thesis proposes power-efficient RC oscillators that can accurately and reliably cancel out the TCs of resistors and compensate the long-term frequency drift caused by aging without the need for external stable sources such as quartz crystals or MEMS devices.

1.2 Thesis Organization

The focus of this thesis is on developing temperature and aging compensation techniques to realize good frequency accuracy with low power consumption. The dissertation consists of four chapters organized as follows:

In Chapter 2, the design of a power-efficient FLL-based temperature-compensated oscillator (TCO) is discussed. It leverages three high-resolution switched resistors (SRs) to compensate the first- and second-order TCs of the oscillator output frequency. The proposed architecture utilizes a low-leakage switched capacitor resistor (SCR) and a temperature-insensitive reference resistor composed of the SRs to achieve excellent temperature stability with low power consumption without the need for power-hungry high-resolution ADCs.

Chapter 3 presents an FLL-based temperature- and aging-compensated RC oscillator (TACO) with good power efficiency. It compensates the long-term drift of its main os-

cillator by periodically locking its frequency to that of the less-aged reference oscillator. To improve the long-term stability of the TACO, it employs techniques such as the use of higher activation energy (E_a) resistors, switched dual RC-branches to mitigate stress from DC-current-induced electromigration (EM), and duty cycling to slow down the aging rate of the reference oscillator.

Chapter 4 concludes the discussion about the proposed design techniques for temperature and aging compensation presented in this thesis.

CHAPTER 2

TEMPERATURE-COMPENSATED RC OSCILLATOR

2.1 Introduction

Monolithic RC-based frequency references have been attractive alternatives to bulky crystal oscillators in many applications. They consume lower power, occupy a small area, and do not require costly off-chip components [7,9–27]. However, poor frequency accuracy resulting from non-linear temperature sensitivity has limited their usage to systems that can tolerate large frequency inaccuracy (∼1%). A relaxation oscillator is one of the most commonly used forms of an RC oscillator whose frequency is defined by an RC product and the delay of a comparator. Because the comparator's delay has a large temperature coefficient (TC), it needs to be much smaller than the RC time constant to achieve good temperature stability. Meeting this requirement either limits the output frequency or significantly increases power consumption [7, 17–22]. One way to overcome these drawbacks is by locking the period of a ring oscillator to the time constant of a reference RC network using a frequency-locked loop (FLL) [9–16, 23–28]. Because the reference capacitor has minimal temperature sensitivity, the TC of the resistor mainly limits the temperature stability of FLL-based RC oscillators. Several efforts are underway to address this impairment. The most common among them use two optimally scaled resistors with opposite TCs in parallel such that the total resistance becomes almost temperature-independent [23]. However, a large MOSFET switch matrix needed to set this optimum combination introduces a large high-order temperature dependency and degrades the supply sensitivity of the oscillator. This drawback is addressed in [10] by using only two opposite TC resistors switched using pulse density modulated sequences generated by $\Delta\Sigma$ modulators. Because there is only one switch in series with each resistor, the supply sensitivity degradation and higher-order TCs are minimized. Consequently, the RC oscillator in [10] could achieve excellent supply sensitivity, precise first-order temperature compensation, and good power efficiency (1 μW/MHz). However, uncompensated higher-order TCs limited the temperature stability to at best ±530 ppm. Furthermore, it requires resistors with opposite TCs, which may not be available in all pro-

cesses. Higher-order compensation schemes based on finely-tuned analog networks [9] can alleviate some of these drawbacks, but they are susceptible to circuit-level imperfections [9]. Digital FLL-based architectures are amenable for higher-order TC compensation, but the analog to digital converters (ADCs) needed to generate the quantized error signal consume significant power, degrading the oscillator's power efficiency (5-13.8 μW/MHz) [11–14].

This thesis presents circuit techniques to reduce RC oscillator's TC nonlinearity and proposes methods for performing first- and second-order temperature compensation without power-hungry ADCs or opposite-TC resistors. A 100-MHz FLL-based RC oscillator prototype is fabricated in a 65-nm CMOS process, and it achieves an inaccuracy of $\pm$140 ppm (2.1 ppm/°C) from -40 °C to 95 °C after three-point trim, 83-ppm/V voltage sensitivity, 1.3-ppm Allan deviation floor, and power efficiency of 1 μW/MHz. In addition, after single-point trim at room temperature (RT) using the strong correlation between three switched resistors, the prototype achieves an inaccuracy of $\pm$587 ppm (8.7 ppm/°C).

The rest of the chapter is organized as follows: Section 2.2 presents the proposed architecture. Circuit implementation details of key building blocks are described in Section 2.3. Experimental results from the test chips are presented in Section 2.4. Key contributions of this chapter are summarized in Section 2.5.

2.2 Proposed Architecture

A simplified block diagram of the proposed temperature compensated oscillator (TCO) is shown in Fig. 2.1. It is composed of a frequency-locked loop (FLL) that locks the period of a voltage-controlled oscillator (VCO) to a scaled reference RC time-constant, $R_{REF}C_R$, where R_{REF} is the reference resistor and C_R is the capacitance of switched-capacitor resistor (SCR) [10]. The proposed architecture has two voltage dividers. The first voltage divider formed by a low-leakage SCR, and a second-order compensated reference resistor, R_{REF}, generates a frequency-dependent voltage, V_{FB}. The second voltage divider is formed by two resistors $3R_D$ and R_D of the same type and generates a fixed reference voltage $V_{REF} = V_{DD}/4$. The integrator integrates the difference between V_{FB} and V_{REF} and produces a control voltage V_C to the VCO. The divided output clock of the VCO is fed to the SCR via a non-overlapping clock generator. In steady-state, thanks to the significant loop gain of the FLL, the ratio of average SCR resistance, R_{SCR}, and R_{REF} is kept constant such that

$$R_{SCR} : R_{REF} = 3R_D : R_D \tag{2.1}$$

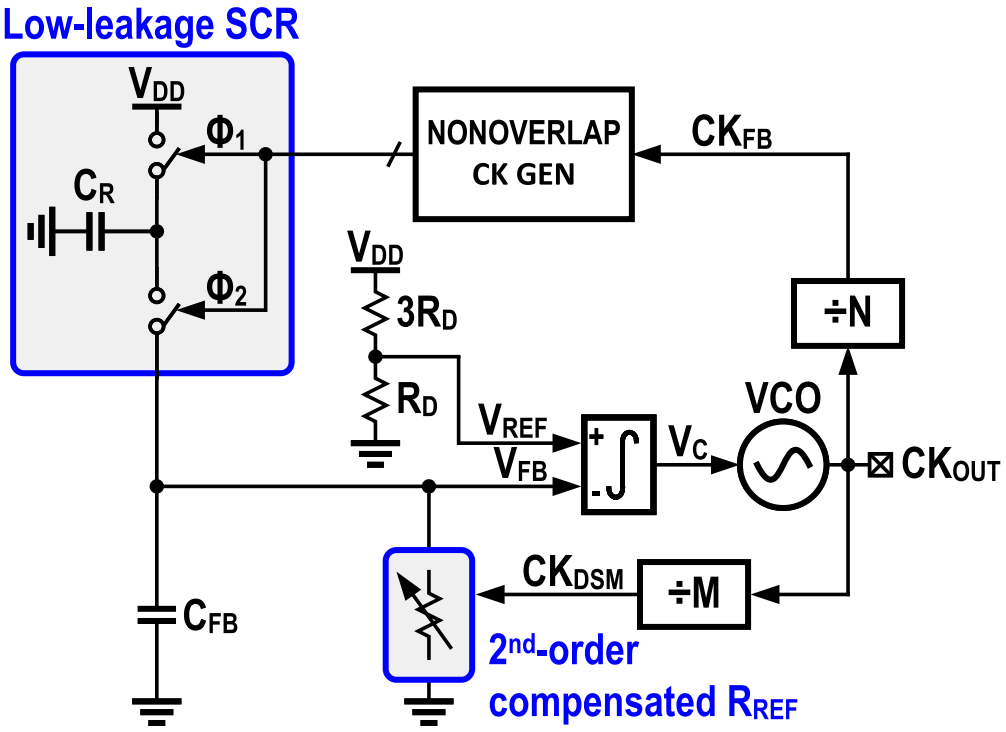


Figure 2.1: Proposed TCO architecture.

where $R_{SCR} = N/F_{OUT}C_R$ and N is the division ratio of feedback clock divider in the FLL loop. TCO's output frequency, F_{OUT}, can be calculated from Eq. (2.1) as

$$F_{OUT} = \frac{N}{3R_{REF}C_R}. \tag{2.2}$$

Equation (2.2) reveals the accuracy of F_{OUT} is primarily dictated by the temperature and supply sensitivity of $R_{REF}C_R$. Therefore, we propose a method described in Section 2.2.2 and 2.2.3 to perform first- and second-order TC compensation of the reference time constant and significantly improve F_{OUT}'s stability. Because second-order effects such as switch leakage in the SCR introduce higher-order temperature dependencies that complicate temperature compensation, we first look at SCR design.

2.2.1 SCR's Non-Idealities and Mitigation Techniques

Several second-order effects in the conventional SCR make its resistance a non-linear function of temperature and V_{DD} and significantly degrade F_{OUT} accuracy. First, the off-state leakage of MOSFET switches introduces an offset in the output frequency and limits the frequency accuracy. The impact of leakage on the SCR can be modeled by a resistor R_P connected in

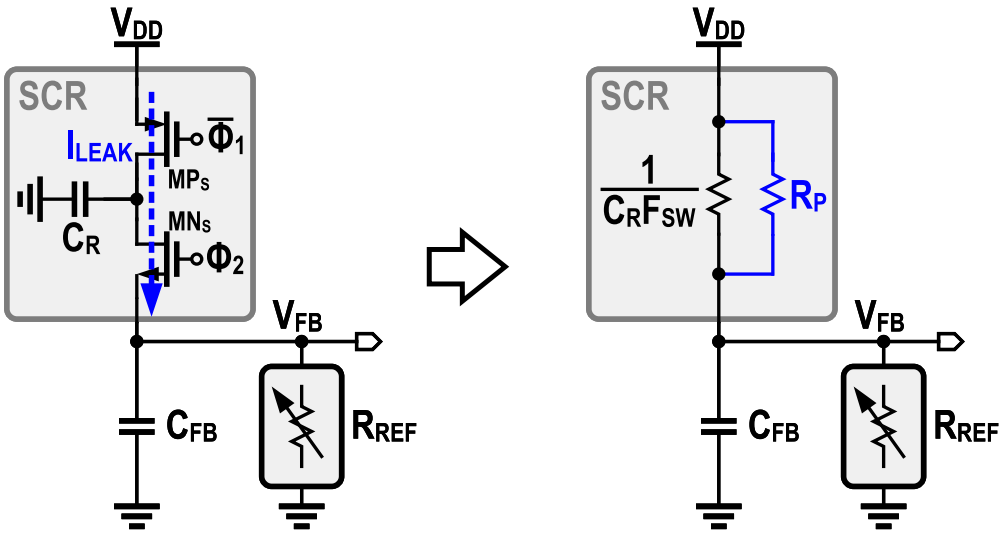


Figure 2.2: Effect of switch leakage currents in a conventional SCR.

parallel with the SCR, as shown in Fig. 2.2. In the presence of R_P, Eqs. (2.1) and (2.2) get modified as follows:

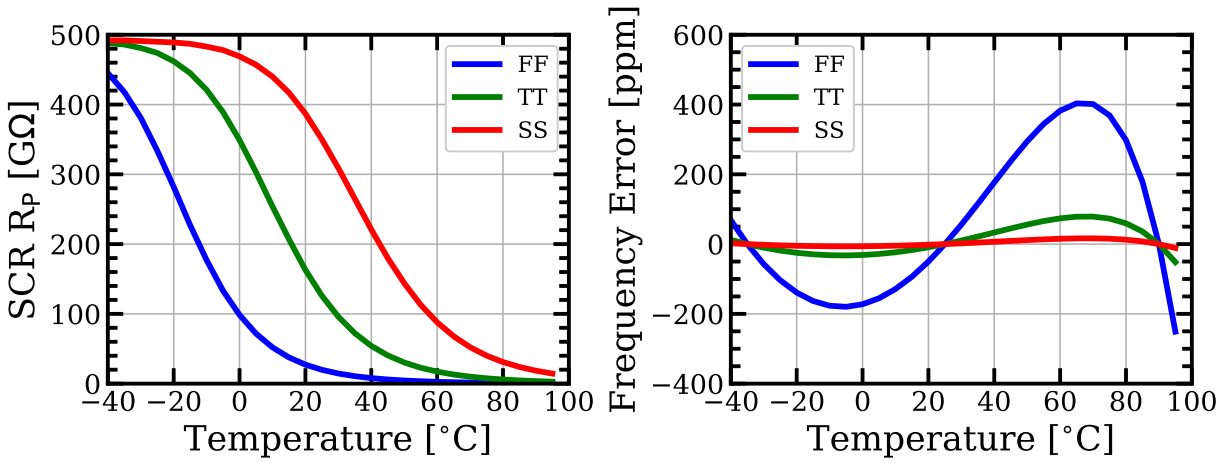
$$R_{SCR} \parallel R_P : R_{REF} = 3R_D : R_D \tag{2.3}$$

$$F_{OUT} = \frac{N}{3R_{REF}C_R} - \frac{N}{R_P C_R}. \tag{2.4}$$

Equation (2.4) reveals that leakage-resistor R_P introduces an offset in the output frequency of $\Delta F_{OUT} = -N/R_P C_R$. Because R_P is a highly non-linear function of temperature as illustrated by Fig. 2.3(a), high-order TC compensation of F_{OUT} is required to overcome its impact. However, even with three-point trimming, an error caused by ΔF_{OUT} as shown in Fig. 2.3(b) significantly limits the frequency accuracy.

To mitigate this effect, a low-leakage SCR shown in Fig. 2.4 is proposed. When Φ_1 is low and Φ_2 is high, the off-state leakage current of the PMOS switch (MP_C) is steered away from C_{FB} to the buffer output using a transmission gate (TG_P) [29–31]. PMOS transistor (MP_S) is added to prevent C_R from being connected to the buffer output. Because MP_S source is connected to $V_{BUF} = V_{DD}/4$ and its drain is discharged to $V_{DD}/4$, V_{DS} of MP_S equals zero, thus significantly reducing its leakage. Similarly, NMOS transistor (MN_S) and transmission gate (TG_N) prevent leakage current of NMOS switch (MN_C) from flowing into C_{FB}. Transistors MP_{CI} and MN_{CI} are dummies to reduce charge injection and clock feedthrough [32]. With the proposed low-leakage SCR, the magnitude of R_P is significantly increased, as shown in Fig. 2.5(a), making its effect on frequency error negligible after three-point trimming, as illustrated in Fig. 2.5(b).

The second non-ideality of SCR is introduced by the finite C_{FB} to C_R ratio, which causes



(a) (b)

Figure 2.3: Simulated SCR imperfection: (a) Equivalent leakage resistor, R_P, versus temperature. (b) Frequency error caused by R_P after three-point trim.

the average value of V_{FB} to deviate from its ideal steady-state value of $V_{FB} = V_{DD}/(1 + N/(R_{REF}C_RF_{OUT})) = V_{DD}/4$ [10, 31], making the SCR resistance a non-linear function of both V_{DD} and temperature. Consequently, SCR conductance becomes a non-linear function of the switching frequency, and therefore F_{OUT}. To mitigate this detrimental effect, two parallel SCRs (SCR_1 and SCR_2) that operate in a ping-pong (or time-interleaved) manner using two phases with a relatively large C_{FB} to C_R ratio of 100 : 1 are used. This ping-pong operation reduces voltage ripple at node V_{FB} compared to a standalone SCR operating in one phase and relaxes the trade-off between the ripple and C_{FB}. This arrangement minimizes the deviation of average V_{FB} to less than one ppm from its ideal value.

Finally, the incomplete settling of V_R and V_{FB} makes the SCR's effective resistance depend on switch on-resistance, which is sensitive to both temperature and V_{DD} variations. The effective SCR resistance is given by [10, 33]

$$R_{SCR} = \frac{T}{C_R}\frac{1+e^{-\gamma}}{1-e^{-\gamma}} = \frac{T}{C_R}\coth(\frac{\gamma}{2}) \tag{2.5}$$

where $\gamma = T/(R_SC_R)$, R_S is the MOS switch resistance, and T $(= N/F_{OUT})$ is the switching period of SCR. All the switches were sized large enough such that $\gamma > 16$ to make the error introduced by incomplete settling to less than 1 ppm. In sum, the secondary effects in the SCR are mitigated by the above circuit techniques, thus improving intrinsic frequency accuracy thereby reducing the burden on the temperature compensation scheme described next.

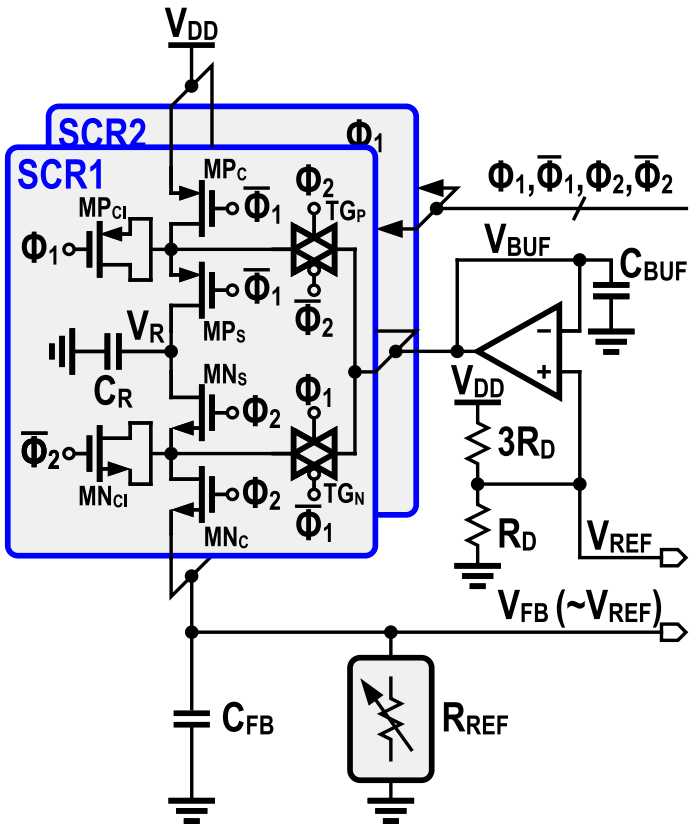
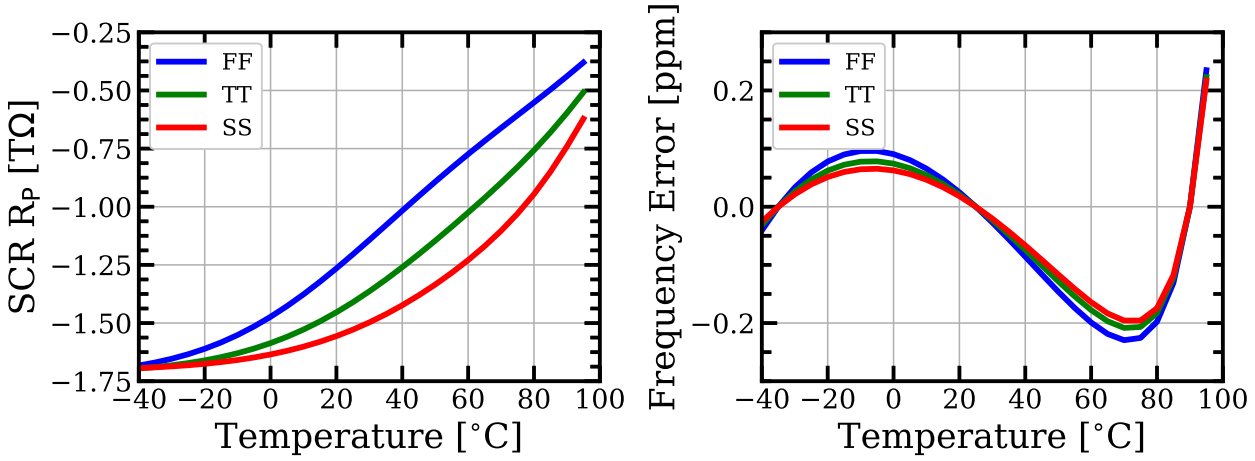


Figure 2.4: Proposed low-leakage SCR.



(a) (b)

Figure 2.5: Effect of leakage in the proposed SCR: (a) R_P versus temperature. (b) Frequency error caused by R_P after three-point trim.

2.2.2 Second-order Compensated Reference Resistor

The switched resistor technique [34] is used to implement the reference resistor because of its high-resolution tunability and small higher-order TCs [10]. To compensate for the first- and

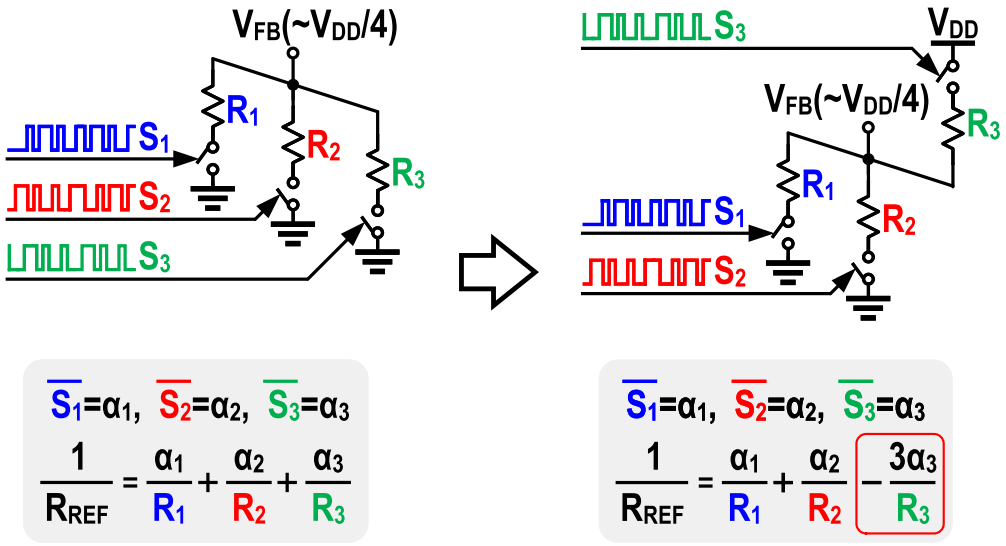


Figure 2.6: Proposed way to add negative sign in R_{REF} equation.

second-order TCs of the oscillator's output frequency, at least three resistors with different TCs are needed (see Fig. 2.6). Denoting the average of switch-controlling sequences S_1, S_2, and S_3 by α_1, α_2, and α_3 respectively, the conductance of the reference resistor and the output frequency can be written as

$$\frac{1}{R_{REF}} = \frac{\alpha_1}{R_1} + \frac{\alpha_2}{R_2} + \frac{\alpha_3}{R_3} \tag{2.6}$$

$$F_{OUT} = \frac{N}{3R_{REF}C_R} = \alpha_1 F_1 + \alpha_2 F_2 + \alpha_3 F_3 \tag{2.7}$$

where

$$F_i = \frac{N}{3R_i C_R}, \ i = 1, 2, 3. \tag{2.8}$$

There exists some optimum α_1, α_2, and α_3 at which the TCO output frequency, F_{OUT}, is insensitive to the temperature at least to the first- and second-order. These optimum alphas can be determined uniquely by using a three-point trimming method. To this end, F_{OUT} is measured at three temperatures, T_1, T_2, and T_3, and the desired frequency, F_{DES}, is expressed in terms of the unknown α_{1OPT}, α_{2OPT}, and α_{3OPT} as follows:

$$F_{DES} = \alpha_{1OPT}F_1(T_1) + \alpha_{2OPT}F_2(T_1) + \alpha_{3OPT}F_3(T_1) \tag{2.9}$$

$$F_{DES} = \alpha_{1OPT}F_1(T_2) + \alpha_{2OPT}F_2(T_2) + \alpha_{3OPT}F_3(T_2) \tag{2.10}$$

$$F_{DES} = \alpha_{1OPT}F_1(T_3) + \alpha_{2OPT}F_2(T_3) + \alpha_{3OPT}F_3(T_3) \tag{2.11}$$

Solving Eqs. (2.9), (2.10), and (2.11) yields α_{1OPT}, α_{2OPT}, and α_{3OPT}. However, when these calculations were performed with p-poly, n-diffusion, and p-diffusion resistors for R_1, R_2, and R_3, respectively, α_{3OPT} turned out to be negative, as shown in Fig. 2.7(a). Unfortunately, such a negative α_{3OPT} cannot be realized because the average of sequence S_3 can only be between [0, 1). Note that even though the p-poly resistor has an opposite sign first- and second-order TCs compared to the other two resistors, it cannot guarantee that all α_{1OPT}, α_{2OPT}, and α_{3OPT} are positive. Another combination consisting of only positive TC resistors (n-poly, n-diffusion, and p-diffusion) also results in a negative α_{3OPT} (see Fig. 2.7(b)). Therefore, a method to realize a negative α_{OPT} is needed for performing second-order compensation.

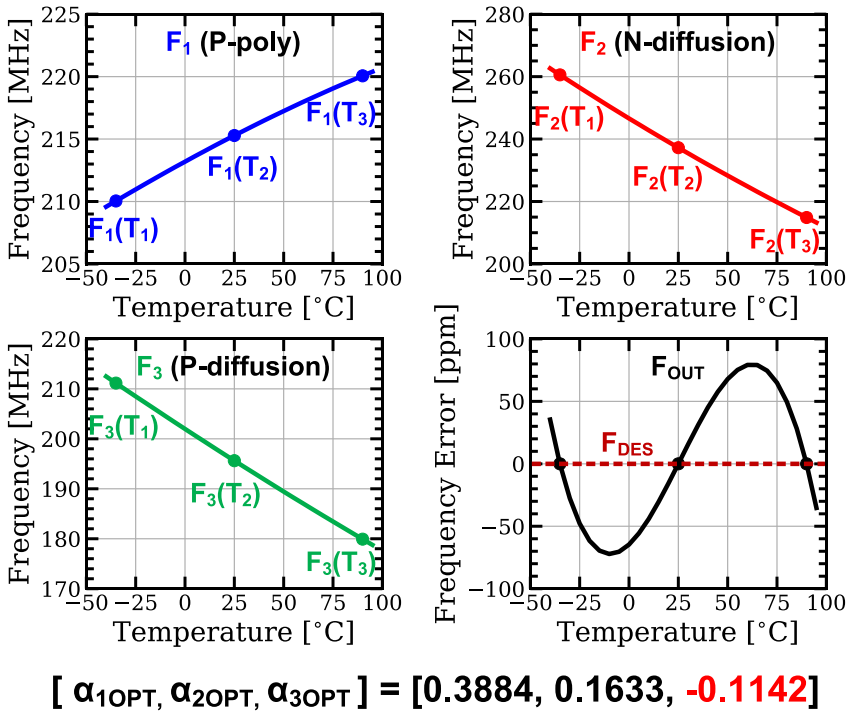
Figure 2.6 shows the proposed method to address the issue of negative α_{OPT}. Switched resistor R_3, which was previously connected to the ground terminal, is now connected to V_{DD}. As a result, it pulls up node V_{FB} instead of pulling it down, behaving as a negative resistor as indicated by the negative sign in the last term of the R_{REF} equation shown at the bottom of Fig. 2.6. The 3× factor is a result of V_{FB} being forced to be equal to $V_{REF} = V_{DD}/4$ by the FLL in steady-state. The details of the complete reference resistor are shown in Fig. 2.8. Resistors R_1, R_2, and R_3 are controlled by sequences, S_1, S_2, and S_3 generated by three first-order $\Delta\Sigma$ modulators. Each resistor can be either connected to ground or V_{DD} using low-leakage switches controlled by signals SEL_1, SEL_2, and SEL_3. If the calculated α_{1OPT}, α_{2OPT}, and α_{3OPT} are between zero and one (see case 1 in Fig. 2.8), all the SEL signals are set to zero, and the α_{OPT}s are quantized to 17-bit digital words D_1, D_2, and D_3 and fed to the $\Delta\Sigma$ modulators. If some α_{OPT}s are negative, the corresponding SEL signal is set to one and the corresponding digital word is set to $|\alpha_{OPT}|/3$ to compensate for the 3× factor described earlier. For example, if α_{OPT3} is negative as shown in case 2 of Fig. 2.8, SEL_3 is set to one, D_3 is set to $|\alpha_{OPT3}|/3$, resulting in R_{REF} and F_{OUT} of

$$\frac{1}{R_{REF}} = \frac{\alpha_{1OPT}}{R_1} + \frac{\alpha_{2OPT}}{R_2} - \frac{|\alpha_{3OPT}|}{R_3} \tag{2.12}$$

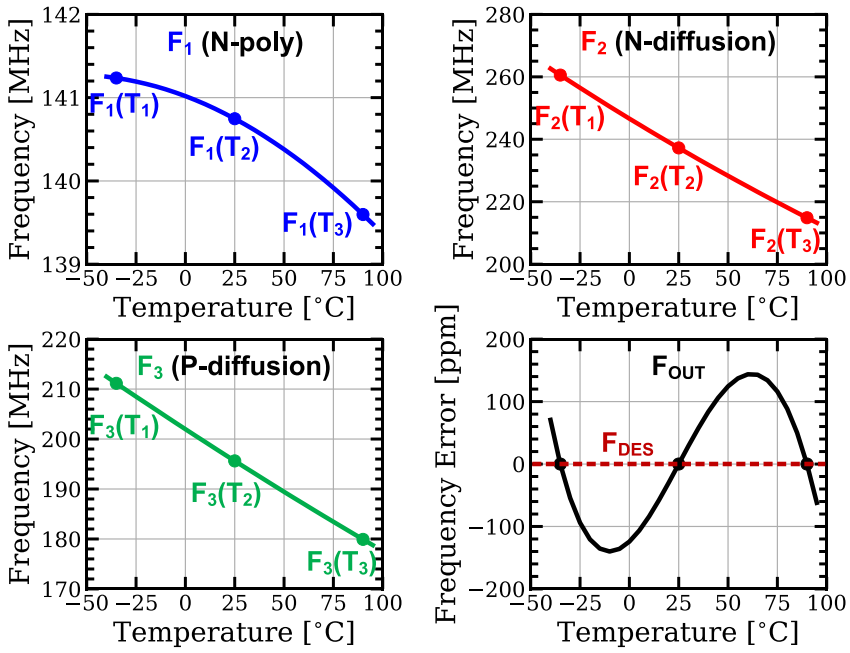
$$F_{OUT} = \alpha_{1OPT}F_1 + \alpha_{2OPT}F_2 - |\alpha_{3OPT}|F_3 \tag{2.13}$$

This programmability eliminates the need for resistors with opposite TCs, a restriction that plagued prior designs [10].

The off-state leakage of MOS switches used in the switched resistor introduces temperature- and α-dependent offsets in the reference resistor and the output frequency as expressed



(a)



(b)

Figure 2.7: Simulated F_1, F_2, F_3, three-point trimmed F_{OUT}, and α_{OPT}s (a) with p-poly resistor and (b) with n-poly resistor.

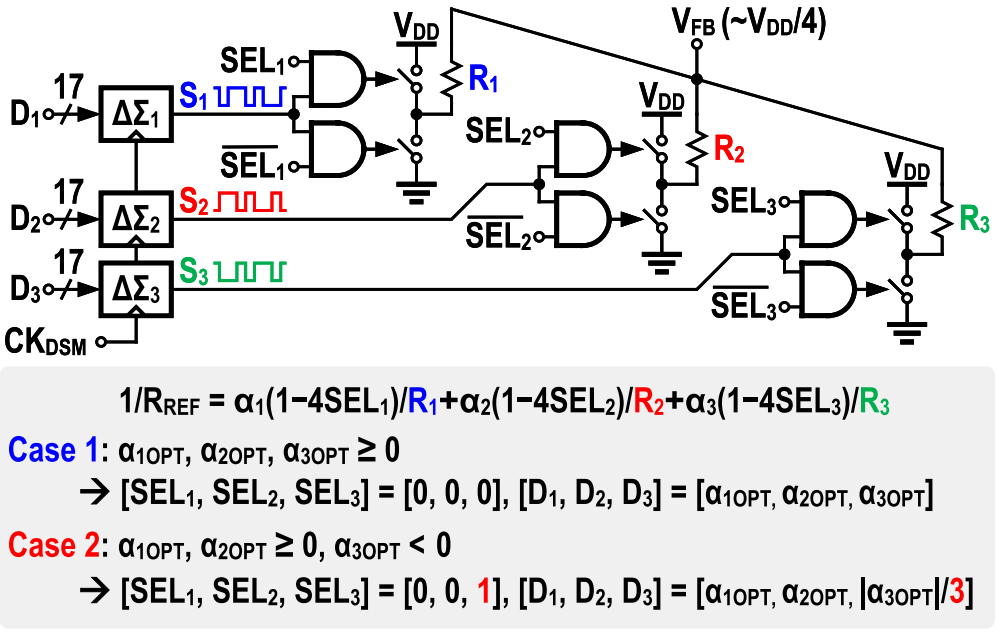


Figure 2.8: Proposed reference resistor schematic.

below [10]

$$\frac{1}{R_{REF}} = \frac{\alpha_1}{R_1} + \frac{1-\alpha_1}{R_{OFF}} + \frac{\alpha_2}{R_2} + \frac{1-\alpha_2}{R_{OFF}} + \frac{\alpha_3}{R_3} + \frac{1-\alpha_3}{R_{OFF}} \tag{2.14}$$

$$F_{OUT} = \alpha_1 F_1 + \alpha_2 F_2 + \alpha_3 F_3 + (3 - \alpha_1 - \alpha_2 - \alpha_3) F_{OFF} \tag{2.15}$$

where R_{OFF} is off resistance of the switched resistor and $F_{OFF} = N/(3R_{OFF}C_R)$. To mitigate these undesirable offsets, leakage reduction techniques used in the SCR are employed in the switched resistors. They help achieve $R_{OFF} > 0.9$ TΩ and $F_{OFF} < 0.5$ ppm, making the leakage effect on frequency error negligible. The unity-gain buffer used for the low-leakage SCR is shared with the switched resistors to reduce power consumption and save area.

2.2.3 Trimming Process

The three-point trimming process is illustrated in Fig. 2.9. First, all switched resistors are connected to ground by setting SEL_1, SEL_2, and SEL_3 signals to zero. Then, the temperature is set to T_1 and output frequencies $F_1(T_1)$, $F_2(T_1)$, and $F_3(T_1)$ are measured by setting [S_1, S_2, S_3] = [1, 0, 0] (for measuring F_1), [S_1, S_2, S_3] = [0, 1, 0] (for measuring F_2), or [S_1, S_2, S_3] = [0, 0, 1] (for measuring F_3), respectively. This process is repeated at two other temperatures, T_2 and T_3, and the resulting nine measured frequencies are used to set up the system of equations shown in Fig. 2.9. Solving these equations yields an estimate of alpha values,

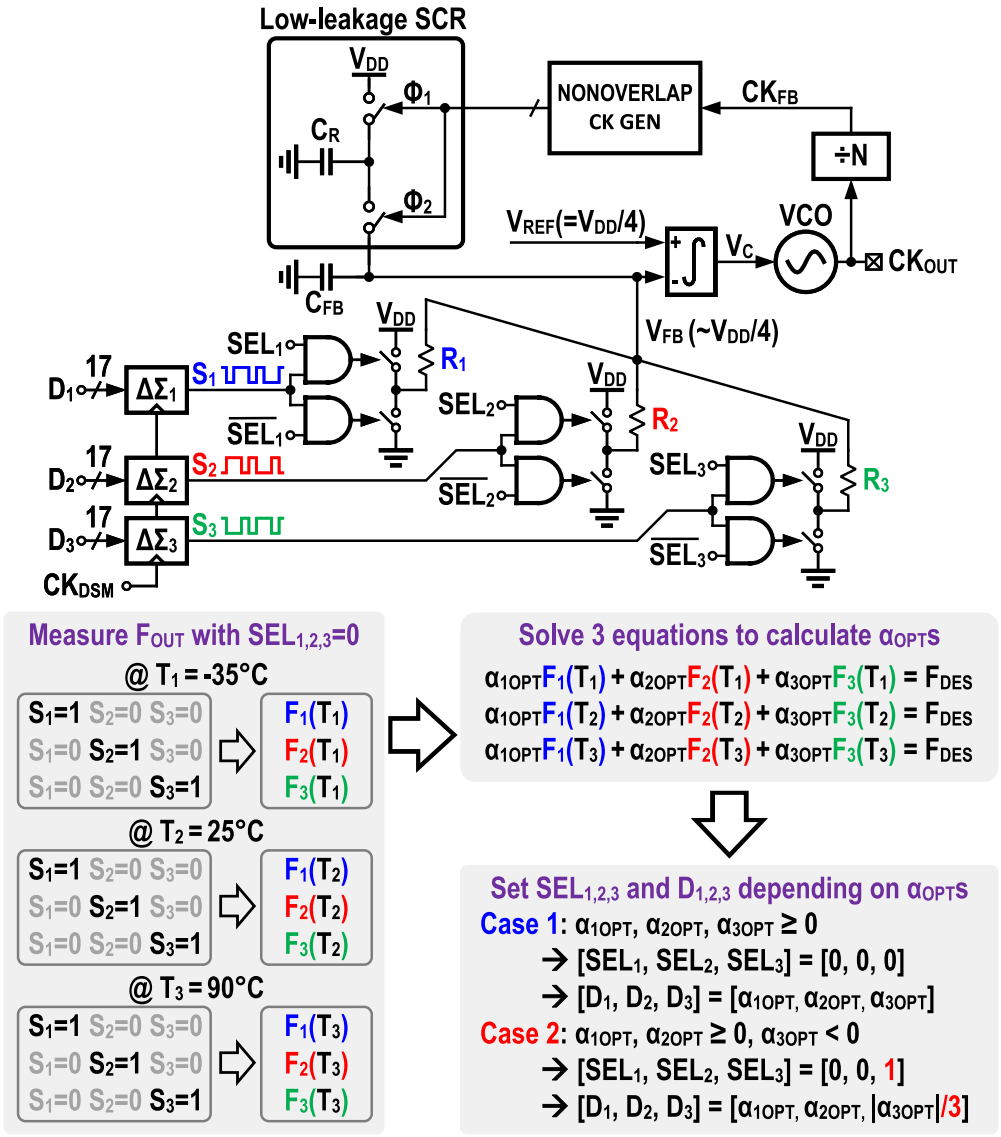


Figure 2.9: Three-point trimming logic.

which are then fine-tuned to obtain α_{1OPT}, α_{2OPT}, α_{3OPT}. They are quantized to 17-bit digital words D_1, D_2, and D_3. $\Delta\Sigma$ modulators are used to truncate the 17-bit digital words to 1-bit pulse-density modulated signals used to control the switched resistors, providing better than 8-ppm frequency tuning resolution. If an α_{iOPT} turns out to be negative, SEL_i and D_i are set to 1 and $|\alpha_{iOPT}|/3$, respectively (see Fig. 2.9).

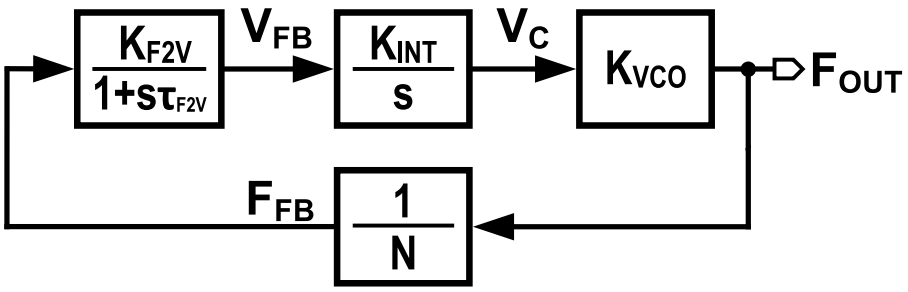


Figure 2.10: Linearized FLL model.

2.2.4 Frequency-Locked Loop Design

The linearized FLL model shown in Fig. 2.10 is utilized to determine the loop parameters and ensure the TCO's stable closed-loop operation. The transfer function of SCR can be derived as a low-pass filter with a gain of K_{F2V} and a time constant of τ_{F2V} [10] where

$$K_{F2V} = \frac{V_{DD}}{F_{FB}} \frac{R_{REF} C_R F_{FB}}{(1 + R_{REF} C_R F_{FB})^2} \tag{2.16}$$

$$\tau_{F2V} = \frac{R_{REF}(C_{FB} + C_R/2)}{1 + R_{REF} F_{FB} C_R}. \tag{2.17}$$

In steady-state, thanks to FLL's large loop gain, the ratio of R_{SCR} to R_{REF} equals three to one, which allows K_{F2V} and τ_{F2V} to be rewritten as

$$K_{F2V} = \frac{3V_{DD}}{16F_{FB}} = \frac{3V_{DD}}{16} \frac{N}{F_{OUT}} \tag{2.18}$$

$$\tau_{F2V} = \frac{1}{8}\left(1 + 2\frac{C_{FB}}{C_R}\right) \frac{N}{F_{OUT}}. \tag{2.19}$$

From Fig. 2.10, the loop gain, $LG(s)$, is given by

$$LG(s) = \frac{K_{F2V}}{1 + s\tau_{F2V}} \frac{K_{INT}}{s} \frac{K_{VCO}}{N} \tag{2.20}$$

where K_{INT} is the integrator gain and K_{VCO} is the voltage-to-frequency gain of the VCO. In the TCO prototype, the unity gain frequency, ω_{UGF}, is designed to be much smaller than $1/\tau_{F2V}$ and is equal to

$$\omega_{UGF} \approx \frac{3}{16} \frac{V_{DD} K_{INT} K_{VCO}}{F_{OUT}}. \tag{2.21}$$

To ensure FLL stability and suppress $\Delta\Sigma$ quantization error, ω_{UGF} is set to be about 1 kHz.

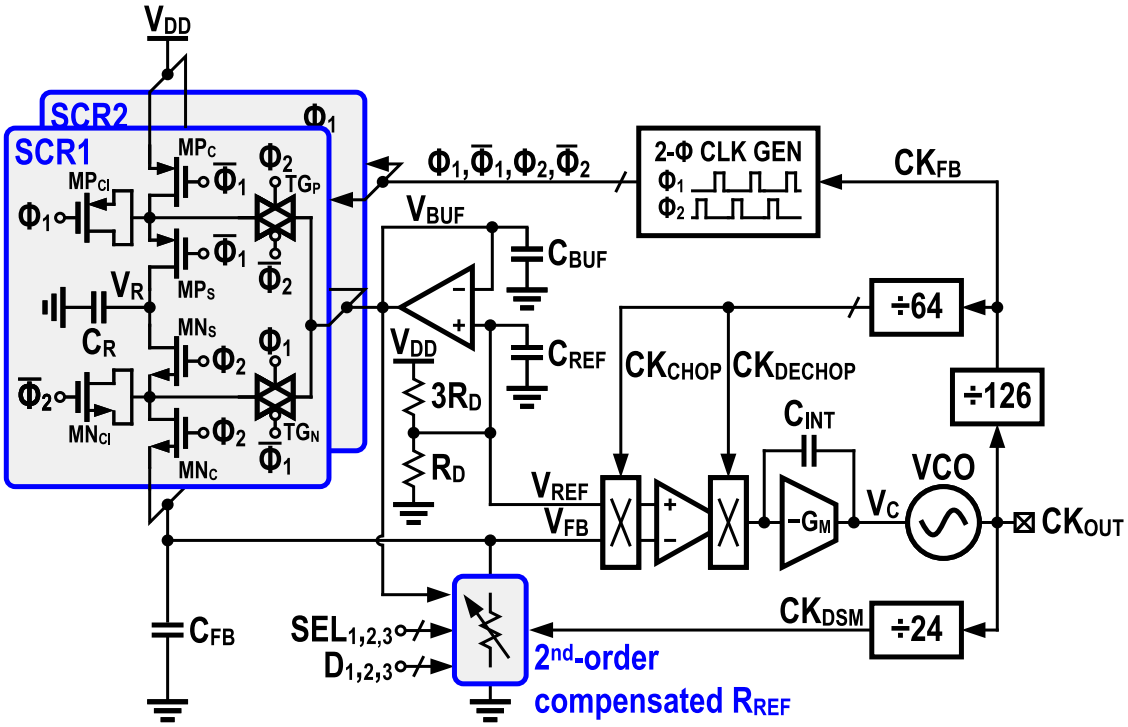


Figure 2.11: Complete TCO architecture.

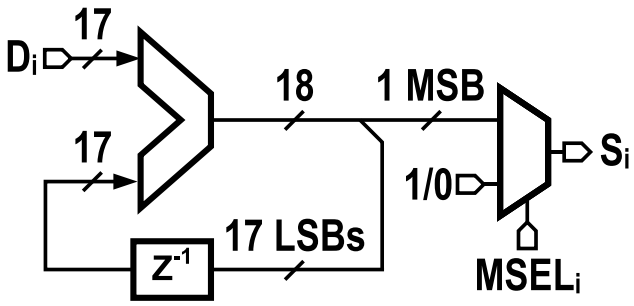


Figure 2.12: First-order ΔΣ modulator.

2.3 Circuit Implementation

The complete architecture of the proposed TCO is shown in Fig. 2.11. A VCO generates a 100-MHz output clock and feeds to a frequency divider (division ratio of 126) that produces about 0.8-MHz feedback clock, CK_{FB}. A non-overlapping clock generator produces phases Φ_1 and Φ_2 used in two low-leakage SCRs (SCR_1 and SCR_2) from CK_{FB}. Each SCR has a capacitance C_R implemented using a 0.5-pF MIM capacitor with a TC of -15.7 ppm/°C, whose effect is also compensated after trimming. To linearize the SCR's conductance versus switching frequency characteristic, a capacitor, $C_{FB} = 50$ pF, is connected at the V_{FB} node. The three resistors in the reference resistor are switched using three pulse density modulated

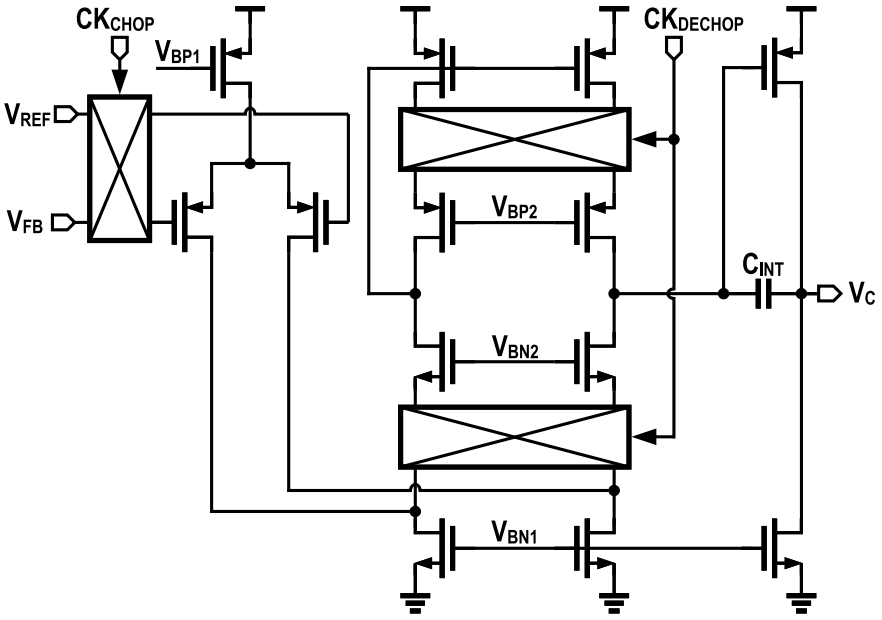


Figure 2.13: Schematic of the two-stage integrator.

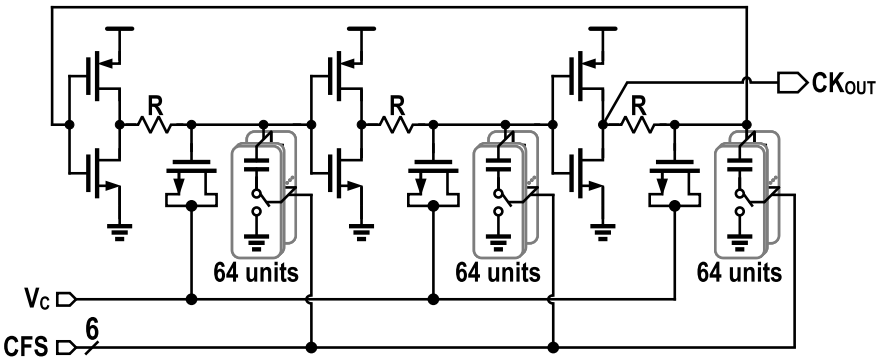


Figure 2.14: Schematic of the voltage-controlled ring oscillator.

sequences S_1, S_2, and S_3, each of which is generated by a first-order $\Delta\Sigma$ modulator, shown in Fig. 2.12. The $\Delta\Sigma$ modulator implemented using an error-feedback topology clocked at 4.2 MHz quantizes a 17-bit digital word, D_i, to a 1-bit pulse density modulated sequence, S_i. The optimum average values for the three sequences are determined using the three-point trimming process described earlier in Section 2.2.3. The loop is closed by a high-gain two-stage integrator implemented using $G_M - C$ topology depicted in Fig. 2.13. The integrator's first stage is chopped to suppress flicker noise and temperature-dependent offset, improving Allan deviation and temperature stability. The 12 kHz chopping/de-chopping clocks are generated by dividing the feedback clock. The second stage of the integrator is used for increasing the gain and implementing the large integrator time constant using a modest capacitor C_{INT} = 30 pF. The Miller effect causes a dominant pole at the output of the

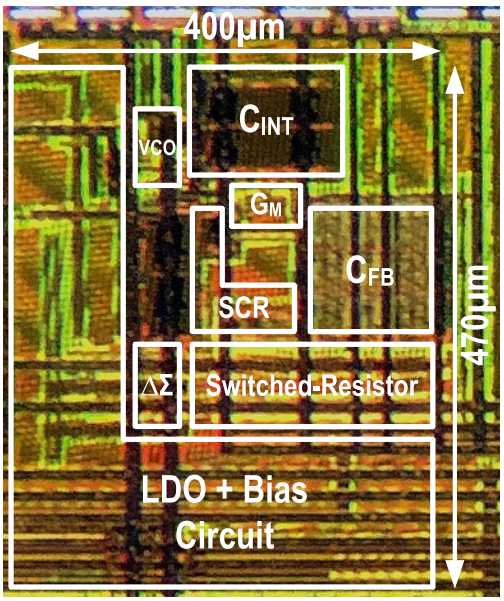


Figure 2.15: Die micrograph.

first stage, thereby stabilizing the loop and limiting the loop bandwidth to 1 kHz needed to suppress $\Delta\Sigma$ modulators' shaped quantization error. Thanks to the integrator's high gain, the DC loop gain is more than 100-dB needed to suppress VCO's supply and temperature sensitivity adequately. The schematic of the VCO is shown in Fig. 2.14. It comprises three delay cells implemented using an inverter, a fixed poly resistor, and controllable capacitors. The temperature sensitivity of the delay cell is dominated by the sensitivity of the resistor and the capacitors. The nominal oscillator frequency is coarsely tuned to 100 MHz using 6-bit binary-weighted MOM capacitor arrays and finely tuned using MOS varactors.

2.4 Measurement Results

A prototype TCO was fabricated in a 65-nm CMOS process and packaged in a plastic QFN package. The die micrograph is shown in Fig. 2.15. To fully characterize the impact of resistor TC on frequency inaccuracy, eight different resistors (two poly resistors, two diffusion resistors, and four composite silicide resistors) were implemented in the prototype with the option of choosing any three out of them to be used in the TCO. The prototype occupies an area of 0.19 mm^2 and draws 84.5 μA from a 1.2 V supply with on-chip LDOs generating 0.9 V for the VCO and digital blocks and 1.0 V for analog blocks. The prototype's power breakdown is shown in Fig. 2.16. The VCO consumes more than 50% of the total power, while the digital blocks such as the dividers, clock generators, and $\Delta\Sigma$ modulators (DSMs)

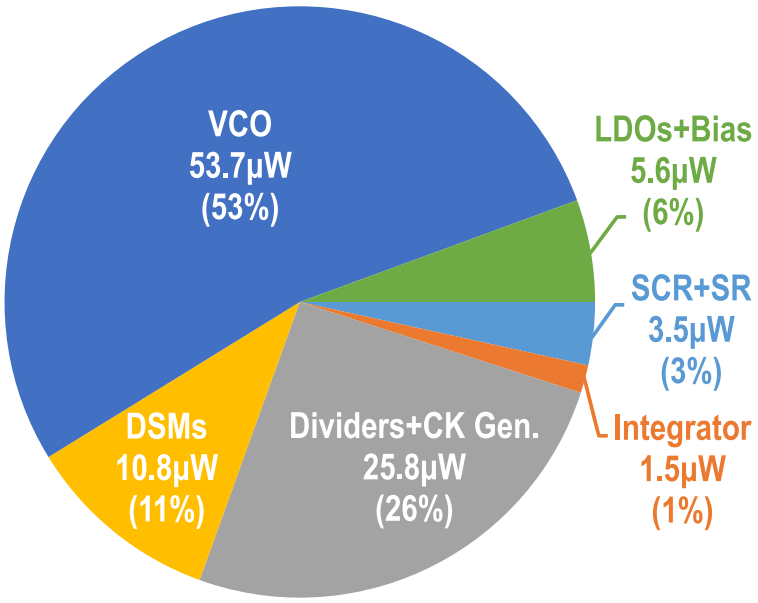
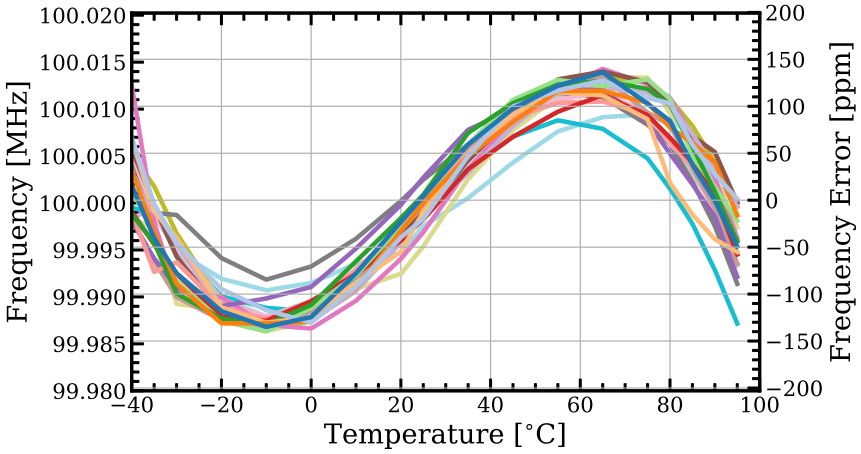


Figure 2.16: Power breakdown of the prototype.

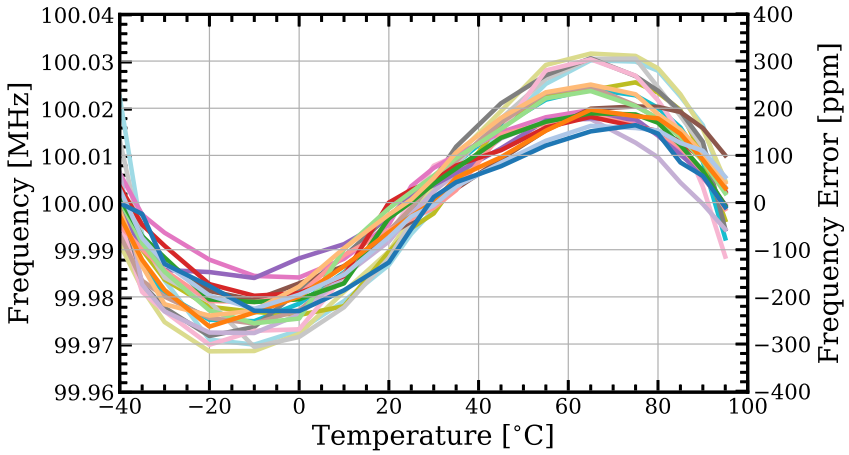
consume 36.6 μW (∼37%) from the 1.2 V supply. SCR, the switched resistors and the integrator consume only 5% of the total power.

2.4.1 Performance with Three-point Trim

D_1, D_2, and D_3 are determined for each sample by trimming the TCO at three temperatures (−35 °C, 25 °C, and 90 °C) for $F_{OUT} = F_{DES} = 100$ MHz. Figure 2.17(a) shows the measured F_{OUT} and residual frequency error for twenty samples using R_1 (189-kΩ negative TC p-poly resistor), R_2 (positive TC 171-kΩ n-diffusion resistor), and R_3 (208-kΩ positive TC p-diffusion resistor). The frequency inaccuracy is less than ±140 ppm over −40 °C to 95 °C, which corresponds to a residual TC of 2.1 ppm/°C in the box method. It represents about 4× improvement over first-order compensated TCO [10]. The inaccuracy at three trim temperature points is not zero, which we believe is limited by ±0.2-°C short-term temperature variation of our temperature chamber (TestEquity Model 107) during trimming. The measured supply sensitivity shown in Fig. 2.18(a) is 83 ppm/V over a V_{DD} range of 1.1 to 2.5 V. Frequency inaccuracy is also measured with all positive TC resistors by replacing R_1 with a positive TC 289-kΩ n-poly resistor to demonstrate the proposed temperature compensation technique without needing resistors with opposite TCs. The inaccuracy for twenty samples shown in Fig. 2.17(b) is less than ±316 ppm over −40 °C to 95 °C (4.7 ppm/°C in box method), which is larger than the inaccuracy with the p-poly resistor mainly due to the higher third-order TC of the n-poly resistor. The measured supply sensitivity with an



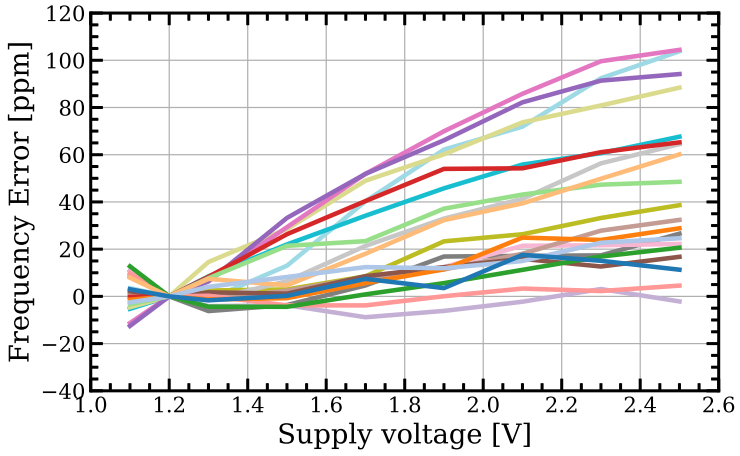
(a)



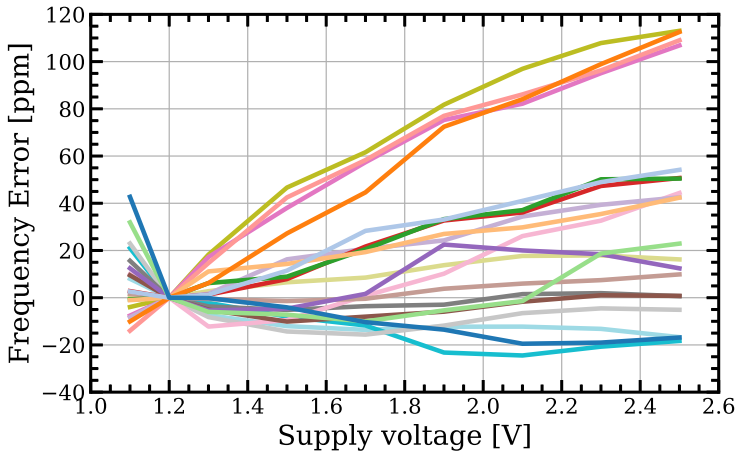
(b)

Figure 2.17: Measured temperature stability after three-point trim (a) with p-poly resistor and (b) with n-poly resistor.

n-poly resistor is 98 ppm/V over a V_{DD} range of 1.1 to 2.5 V as shown in Fig. 2.18(b), which does not show an apparent discrepancy from the supply sensitivity with a p-poly resistor. The worst-case frequency inaccuracy presented in Fig. 2.17 is more than the simulated frequency inaccuracy shown in Fig. 2.7. We believe this is caused by the differences between the resistor TCs in the simulation models and the fabricated parts.



(a)



(b)

Figure 2.18: Measured supply sensitivity (a) with p-poly resistor and (b) with n-poly resistor.

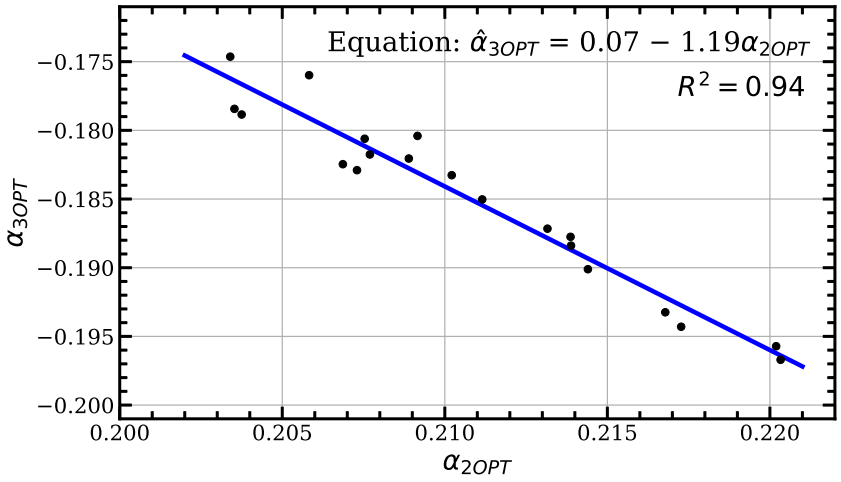
2.4.2 Performance with Single-point Trim

The obtained α_{1OPT}, α_{2OPT}, and α_{3OPT} after three-point trim from twenty samples using a p-poly resistor, n-diffusion resistor, and p-diffusion resistor exhibited a strong correlation between them, as shown in Fig. 2.19. The scatterplot of α_{3OPT} versus α_{2OPT} illustrates this correlation clearly, indicating the data can be fit using a linear regression line (see Fig. 2.19(a)) given by

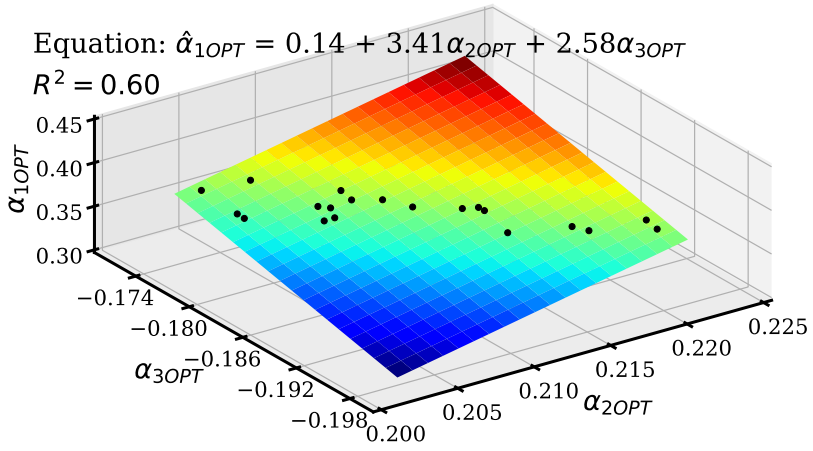
$$\hat{\alpha}_{3OPT} = 0.0661 - 1.191\alpha_{2OPT}. \tag{2.22}$$

The calculated R-squared (R^2) value is 0.94, indicating excellent fitting accuracy.

The scatterplot of α_{1OPT} versus both α_{2OPT} and α_{3OPT} with the multiple linear regression



(a)



(b)

Figure 2.19: Scatterplot of (a) α_{3OPT} versus α_{2OPT} with linear regression line and (b) α_{1OPT} versus both α_{2OPT} and α_{3OPT} with multiple linear regression plane.

plane is depicted in Fig. 2.19(b). It shows a strong correlation ($R^2 = 0.60$) when the multiple linear regression plane is

$$\hat{\alpha}_{1OPT} = 0.1377 + 3.413\alpha_{2OPT} + 2.576\alpha_{3OPT}. \tag{2.23}$$

By substituting Eq. (2.22) into Eq. (2.23) for α_{3OPT}, $\hat{\alpha}_{1OPT}$ can be written as a function of α_{2OPT}, and is given by

$$\hat{\alpha}_{1OPT} = 0.3079 + 0.3442\alpha_{2OPT}. \tag{2.24}$$

Using Eqs. (2.22) and (2.24), single-point trim is performed at 25 °C using binary search

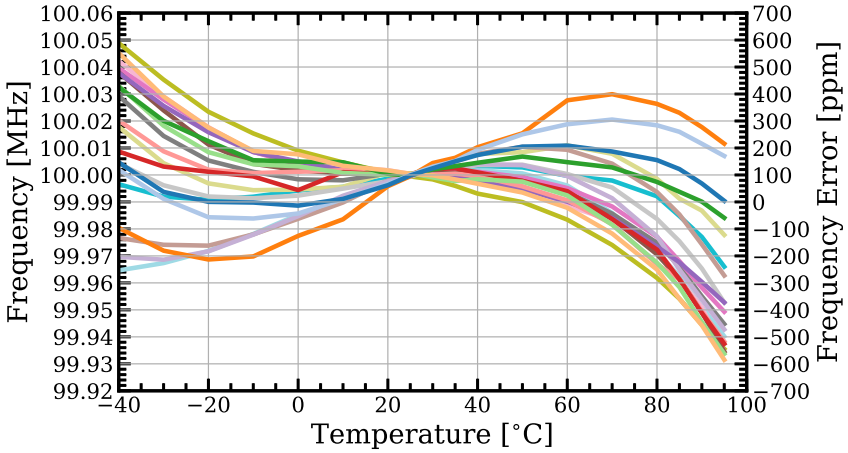
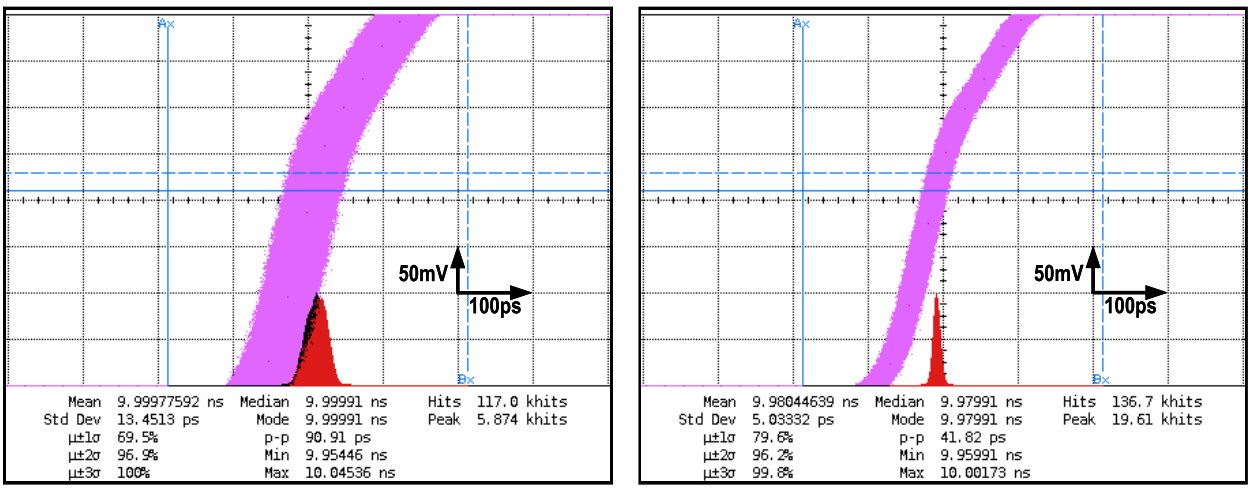


Figure 2.20: Measured temperature stability after one-point trim over twenty samples different from the twenty samples used to calculate linear regression equations.

for α_{2OPT} to force $F_{OUT} = 100$ MHz. $\hat{\alpha}_{1OPT}$, α_{2OPT}, $\hat{\alpha}_{3OPT}$ are quantized to 17-bits and assigned to D_1, D_2, and D_3, respectively. The measured F_{OUT} and residual frequency error with the one-point trim over twenty samples (from the same batch but different from the twenty samples used to calculate linear regression equations) are shown in Fig. 2.20, and the measured frequency inaccuracy is ±587 ppm from −40 °C to 95 °C, which is equivalent to a residual TC of 8.7 ppm/°C in the box method. The inaccuracy decreases to ±474 ppm (7.6 ppm/°C) with a relaxed temperature range of −40 °C to 85 °C, which is comparable to the inaccuracy achieved with two-point trim in [10].

2.4.3 Output Clock Performance

The measured output period jitter is 13.4 ps_{rms} compared to the 5-ps_{rms} period jitter of the open-loop ring oscillator (see Fig. 2.21). The shaped quantization error of ΔΣ modulators is the dominant period jitter contributor. They contribute about 86% of the total TCO's jitter, with the rest (14%) coming mostly from the VCO. When the ΔΣ modulator's sampling frequency was doubled, the period jitter reduced to 7.7 ps_{rms} and the power consumption increased by ten μW. The Allan deviation for a 1-second stride is 25.5 ppm without chopping, reduces to 1.6 ppm with chopping, and reaches a floor of 1.3 ppm over a 10-second stride in Fig. 2.22.



(a) (b)

Figure 2.21: Period jitter of (a) closed-loop TCO (b) open-loop ring oscillator.

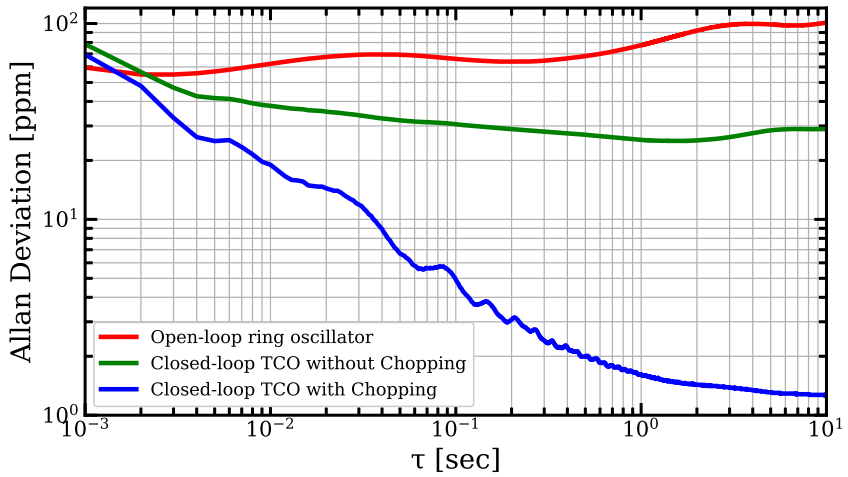


Figure 2.22: Allan deviation.

Table 2.1: Performance summary and comparison with state-of-the-art on-chip RC oscillators.

	This Work		Jiang [12] ISSCC21	Cristiano [25] VLSI20	Griffith [20] ISSCC14	Mehta [22] JSSC22	Ji [28] ISSCC22	Khashaba [10] JSSC21	Gurleyuk [14] JSSC22		Choi [13] JSSC21	Zhang [9] JSSC18
Process	65nm		180nm	180nm	65nm	5nm	180nm	65nm	180nm		65nm	180nm
Frequency [Hz]	100M		16M	116k	33k	77M	2.3M	32M	16M		28M	24M
Power [W]	101μ		158μ	694n	0.19μ	840μ	7.6μ	34μ	220μ		142μ	360μ
Power Efficiency [μW/MHz]	1		9.9	5.98	5.9	10.9	3.3	1.06	13.8		5	15
Trimming Points	1+batch	3	1+batch			2				2+batch		3
TC [ppm/°C]	8.7	2.1	5.2	8.7	38.2	36	18.9†	8.4	5.9	1.4	2.56	10*
Temp Range [°C]	−40 to 95		−45 to 85	−15 to 85	−20 to 90	−40 to 125	−40 to 125	−40 to 85	−45 to 85		−40 to 85	−40 to 150
Voltage Sensitivity [ppm/V]	83**		2000	3800	900	14000	5100	80**	1200		2900	100**
Voltage Range [V]	1.1 to 2.5		1.6 to 2.0	1.8 to 2.0	1.15 to 1.45	1.1 to 1.35	1.3 to 2.0	1.1 to 2.3	1.6 to 2.0		0.85 to 1.05	1.8 to 5.0
# of Samples	20		18	10	5	8	11	6	20		16	200
Area [mm^2]	0.19**		0.14	1.2	0.015	0.015	0.14	0.18**	0.3		0.06	0.17**
Period Jitter [ps$_{\text{rms}}$]	13.4		10.2	-	-	60	-	24.4	39.9		7	-
ADEV Floor [ppm]	1.3		0.35	4	4	-	9	2.5	0.32		2	-

* Worst case=μ+3σ ** With on-chip LDO † Worst case

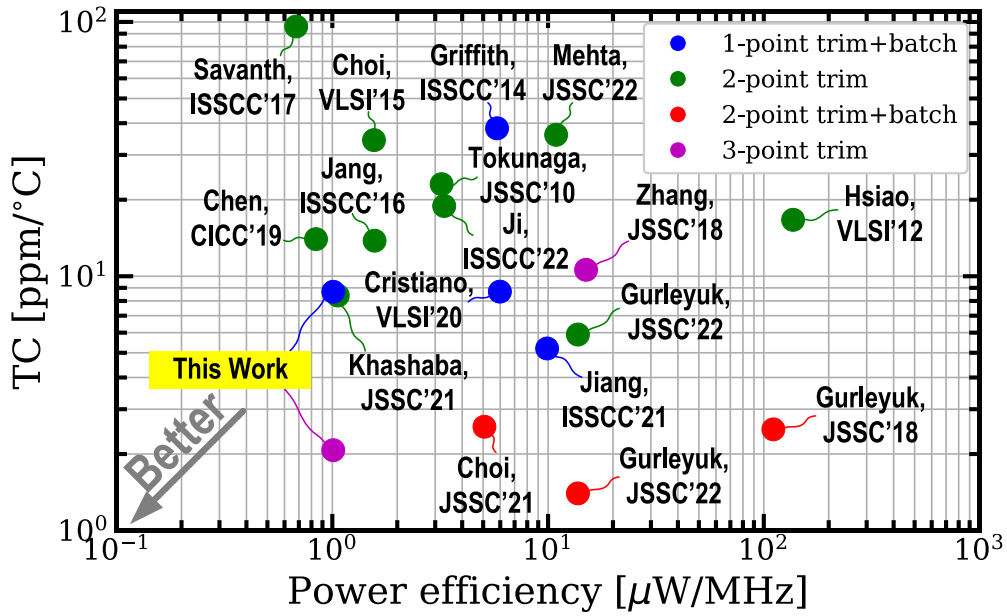


Figure 2.23: Temperature coefficient versus power efficiency.

Table 2.1 and Fig. 2.23 summarize the performance of the TCO and compare it to state-of-the-art RC oscillators. The proposed TCO achieves excellent power efficiency and temperature stability after trimming at three points.

2.5 Conclusion

A method for precise and robust compensation of the resistor TC using a parallel combination of three switched resistors digitally controlled by pulse-density modulated sequences is presented. The proposed low-leakage SCR and the second-order compensation scheme help achieve excellent temperature stability without needing opposite sign TC resistors. Using trimming at three temperature-insertion points, the high-frequency FLL-based temperature-compensated oscillator achieves a frequency inaccuracy of ±140 ppm from −40 °C to 95 °C (2.1 ppm/°C), 83-ppm/V voltage sensitivity, 1.3-ppm Allan deviation floor, and excellent power efficiency of 1 μW/MHz. When a single-point trim at room temperature is performed by leveraging a solid correlation between α_{OPT}s, frequency inaccuracy of ±587 ppm from −40 °C to 95 °C (8.7 ppm/°C) was achieved. The proposed TCO achieves excellent frequency accuracy at low power, making it suitable for micro-controller applications where the desired clock frequency is in the range of 100 MHz [24].

CHAPTER 3

TEMPERATURE- AND AGING-COMPENSATED RC OSCILLATOR

3.1 Introduction

Integrated RC oscillators are becoming increasingly popular as clock sources in various applications, replacing bulky crystal or MEMS oscillators due to their smaller physical footprint, lower power consumption, and lack of expensive off-chip components [7, 9–27, 35–37]. These oscillators achieve excellent short-term frequency stability through novel methods that compensate for the frequency inaccuracy caused by the temperature coefficient (TC) of resistors used in the reference RC networks [9–16]. Over the past decade, numerous papers have been published to improve the temperature stability of RC oscillators, resulting in a significant improvement in their frequency accuracy, which is now comparable to crystal oscillators [14]. Despite their exceptional performance, the lack of information on the aging behavior of RC oscillators and their inability to guarantee long-term performance limits their commercial deployment.

Resistor aging is the primary contributor to long-term frequency drift in RC oscillators, and p-poly resistors, commonly used as reference resistors in RC oscillators for their high sheet resistance, small area, and relatively low-temperature coefficient of resistance (TCR), are particularly prone to aging [38,39]. Accelerated aging tests on standalone p-poly resistors have shown that their resistivity can change by over 0.5% after 1000 hours at 150 °C [40]. To evaluate the effect of resistor aging on the oscillator's frequency, a temperature-compensated frequency-locked loop (FLL)-based RC oscillator prototype using a p-poly resistor was designed, and its long-term stability was measured by baking it at 125 °C. The results, plotted in Fig. 3.1, show that resistor aging significantly affects the oscillator's frequency, causing more than 5000-ppm drift after 1000 hours. To address this issue, this chapter presents circuit techniques to enhance the long-term stability of RC oscillators and compensate for frequency drift caused by aging without the need for external stable sources. A 100-MHz FLL-based RC oscillator prototype is fabricated in a 65-nm CMOS process, and it achieves an inaccuracy of ±1030 ppm from −40 °C to 85 °C after 500 hours of accelerated aging at

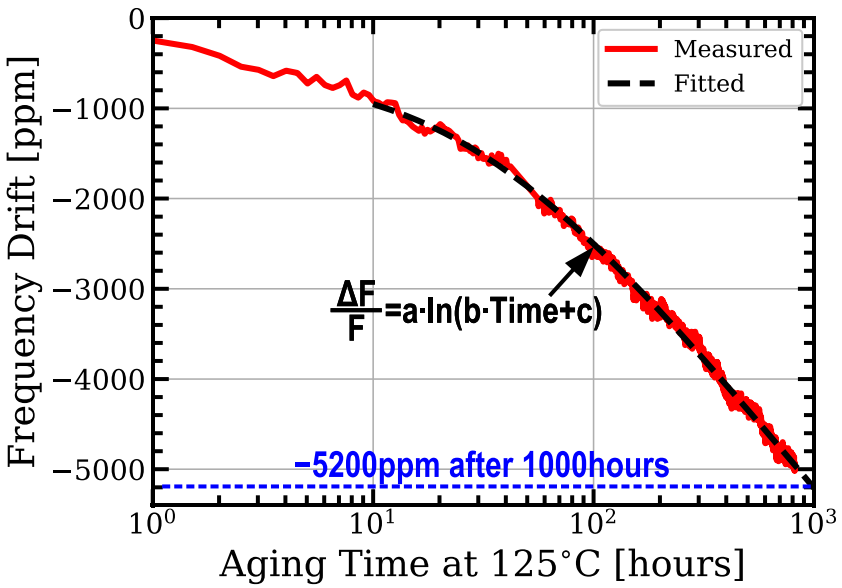


Figure 3.1: RC oscillator aging with a p-poly resistor.

125 °C, with 5.1-ps_{rms} period jitter and power efficiency of 1.4 μW/MHz.

The rest of the chapter is organized as follows: Section 3.2 presents the proposed architecture. Circuit implementation details of key building blocks are described in Section 3.3. Experimental results from the test chips are shown in Section 3.4. Key contributions of this chapter are summarized in Section 3.5.

3.2 Proposed Architecture

A simplified block diagram of the proposed temperature- and aging-compensated RC oscillator (TACO) is shown in Fig. 3.2. The TACO consists of a temperature-compensated oscillator (TCO), a reference TCO, and an aging compensation logic. The TCO operates continuously, while its long-term frequency drift due to aging is addressed by periodically synchronizing it with the less-aged reference oscillator. Both the main and reference TCOs use an FLL-based architecture, utilizing two reference resistors (R_0 and R_1) that are illustrated in Fig. 3.2. The reference oscillator, however, is heavily duty-cycled on time to prevent it from aging.

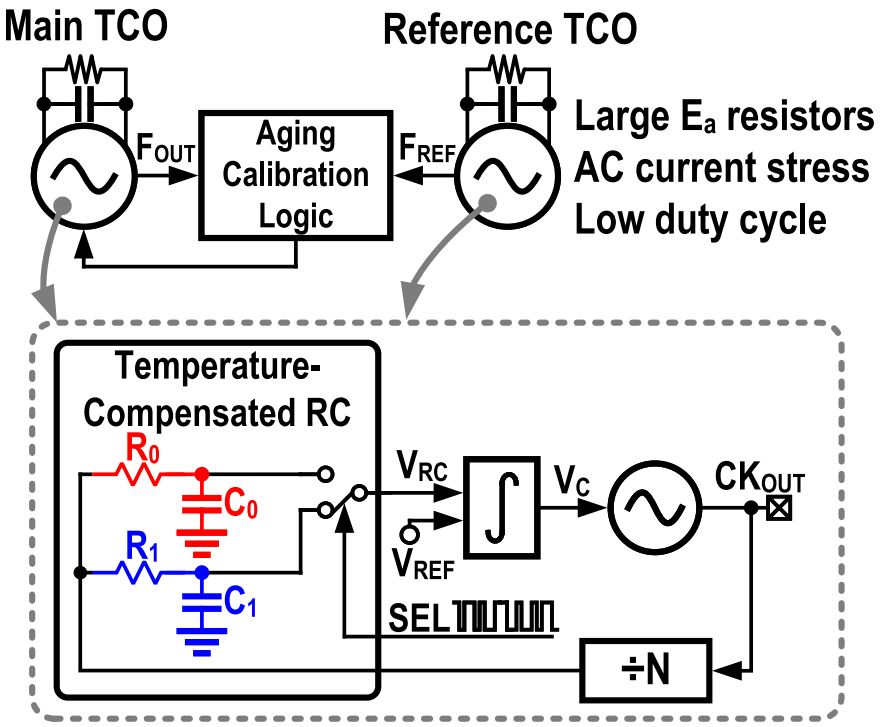


Figure 3.2: Proposed aging calibration scheme and FLL-based TCO architecture.

3.2.1 Techniques for Long-Term Stability Improvement

The TACO system uses various techniques to enhance its long-term stability. One such technique involves using reference resistors with higher activation energy (E_a) to increase their lifetime. The standard CMOS technology offers different types of resistors, such as poly, diffusion, and metal type resistors, whose estimated time to failure (TTF) can be modeled empirically using Black's (see Eq. (3.1)) [41,42] or a power law model (see Eq. (3.2)) [39,42] as

$$TTF = A \cdot J^{-n} \cdot exp\left(\frac{E_a}{kT}\right) \tag{3.1}$$

$$TTF = A \cdot exp\left(-nJ\right) \cdot exp\left(\frac{E_a}{kT}\right) \tag{3.2}$$

where A is an empirically determined constant, J is the current density (A/cm^2), n is the empirically determined current density factor, E_a is the activation energy (eV), k is Boltzmann constant, and T is the absolute junction temperature of the resistor during the aging stress (K). Equations (3.1) and (3.2) show that the TTF of a resistor increases exponentially with larger E_a. The p-poly resistors have a lower E_a of 0.477 eV and suffer from higher degradation caused by aging stress [39,40]. Compared to p-poly resistors, n-poly resistors have a higher E_a of 0.68 eV and longer TTF, making them more suitable for the

better long-term stability of the oscillators. Metal or back-end-of-line (BEOL) type resistors also have higher E_a and exhibit smaller resistivity shifts under electrical and temperature stress than poly resistors [42].

Another technique is to design the reference resistors to have the current direction alternate periodically to reduce the stress caused by electromigration (EM) induced by the DC current. The TTF of poly resistors increases monotonically with the frequency of AC current stress [43]. Electron wind induces the oscillation of dopant atoms by subjecting poly resistors to AC current stress. However, this oscillation does not result in the net movement of the dopant until it is trapped at a defect. The higher the frequency of the stress, the shorter the distance the dopant will travel, which reduces the probability of the dopant encountering a defect in the polysilicon, resulting in an improved TTF of the resistor [43]. Metal-type resistors also show better TTF with AC current stress than DC stress [44]. The circuit implementation for alternating current through reference resistors is described in detail in Section 3.2.2.

The third technique involves using on-time duty cycling to slow down the aging rate of the reference oscillator used to calibrate the main oscillator. The aging rate of poly and metal resistors in a standard CMOS process depends on the duty cycle. Lower duty cycles tend to lead to slower-aging rates of the resistors [44, 45]. By reducing the on-time of the reference oscillator, the amount of time that a current flows through the active devices and interconnects decreases, which can slow down the rate at which specific aging mechanisms, such as hot carrier injection (HCI) and EM, can occur.

3.2.2 Detailed TCO Architecture

It comprises two RC branches (R_0C_0 and R_1C_1), a $G_M - C$ integrator, a voltage-controlled ring oscillator (VCRO), a divider, differential voltage $\Delta\Sigma$-DACs (VDACs), a phase generator, and a $\Delta\Sigma$ modulator. The VCRO clock is divided by N (= 25) and fed to the phase generator, which generates clocks, Φ_{CHG}, Φ_{RST}, Φ_{BUF}, and Φ_{INT}. These clock phases are used to control the switching sequence in the RC branch such that the difference between the track-and-held voltage V_{RC} generated from the RC branch and V_{REF} provided by VDAC represents the error between the desired frequency and VCRO (F_{OUT}) frequency. The error voltage, V_{ERR} (= $V_{RC} - V_{REF}$), is integrated by the integrator and used to adjust the VCRO toward the frequency lock. To perform temperature compensation, the $\Delta\Sigma$ modulator generates mux select signal SEL, which enables either Path_0 consisting of R_0C_0 branch and VDAC_0 when SEL = 0 or Path_1 consisting of R_1C_1 branch and VDAC_1 when SEL = 1, as

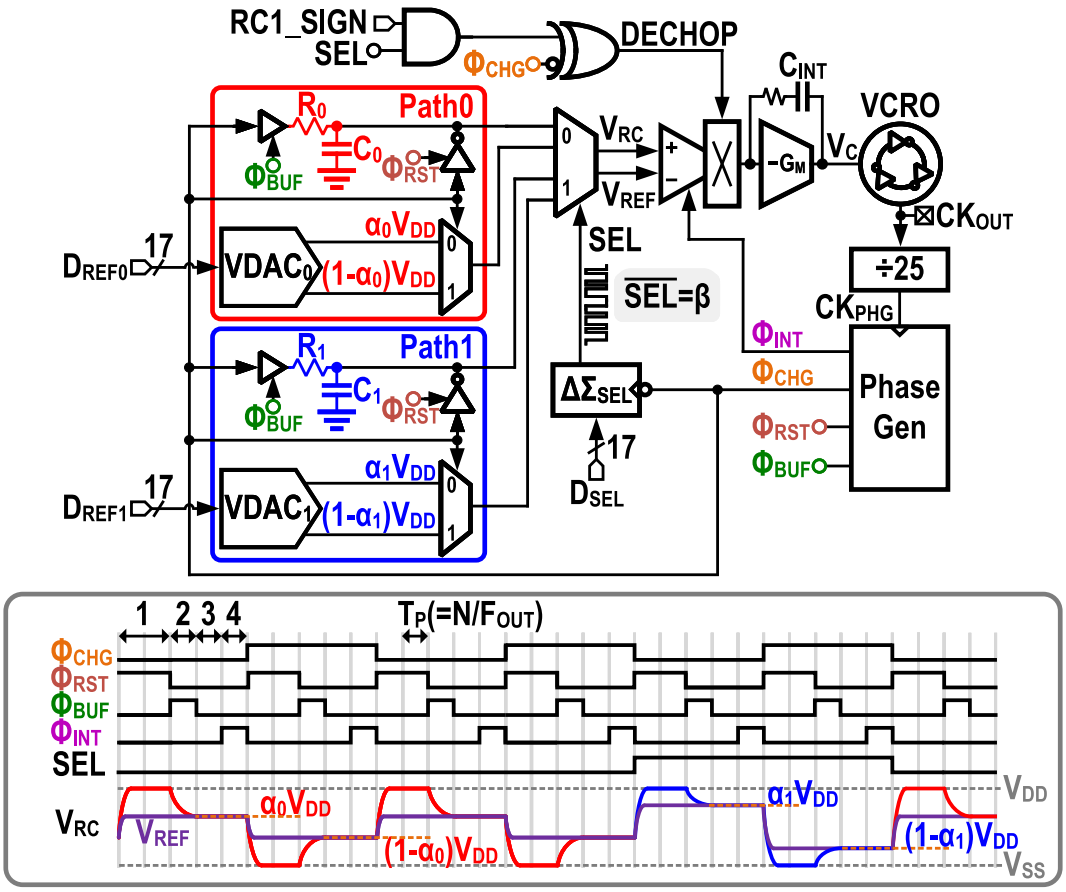


Figure 3.3: Detailed TCO architecture.

described later.

The TCO operates in four phases, as illustrated in the timing waveforms in Fig. 3.3. The first phase commences with SEL = 0 and $\Phi_{\mathrm{CHG}} = 0$, during which the inverter of Path_0 resets C_0 to V_{DD} when $\Phi_{\mathrm{RST}} = 1$ (reset phase). In the second phase when $\Phi_{\mathrm{BUF}} = 1$, the buffer of Path_0 is activated and discharges C_0 via R_0 for T_P duration to $V_{RC0,DCHG} = exp(-T_P/R_0C_0)V_{DD}$, where $T_P = N/F_{OUT}$. The value of V_{RC} $(= V_{RC0,DCHG})$ exceeds V_{REF} $(= \alpha_0 V_{DD})$ if F_{OUT} is greater than the target output frequency, and vice versa. The third phase occurs when Φ_{RST}, Φ_{BUF}, and Φ_{INT} are all zero, providing sufficient time for the redistribution of the charge stored in the parasitic capacitor of the resistor and for V_{RC} to stabilize. In the final phase, Φ_{INT}= 1 and the integrator is enabled (integration phase), V_{ERR} $(= V_{RC0,DCHG} - \alpha_0 V_{DD})$ is integrated for T_P duration, generating the control voltage V_C of the VCRO. In the subsequent cycle with $\Phi_{\mathrm{CHG}} = 1$, C_0 is reset to V_{SS} and charged for a duration of T_P, resulting in $V_{RC0,CHG} = (1 - exp(-T_P/R_0C_0))V_{DD}$, and then V_{ERR} $(= V_{RC0,CHG} - (1 - \alpha_0)V_{DD})$ is integrated for T_P duration. At Φ_{CHG}, the R_0C_0 branch is chopped, and the first-stage output of the integrator is de-chopped via the DECHOP

signal. By reversing the current flow direction in resistor R_0 during periodic discharge and charge operations, the EM-induced stress is significantly minimized, and long-term stability is enhanced compared to unidirectional current flow. Furthermore, the discharge and charge operation occurs with an inherent on-time duty cycle of 20% only when $\Phi_{\mathrm{BUF}} = 1$, which can decrease the aging rate of the resistor.

Assuming that SEL = 0 and Path_0 is selected, the output frequency, F_{OUT0}, of the TCO circuit is given by

$$F_{OUT0} = \frac{N}{R_0 C_0 ln(1/\alpha_0)}. \tag{3.3}$$

In the steady-state with SEL = 0, where $V_{RC0,DCHG}$ and $V_{RC0,CHG}$ are equal to $\alpha_0 V_{DD}$ and $(1-\alpha_0)V_{DD}$, respectively, due to feedback loop operation. Neglecting the TC and aging of C_0 and α_0, the output frequency TC is determined by the TC and aging properties of R_0 alone. To compensate for the TC of R_0, Path_1, consisting of an $\mathrm{R_1C_1}$ branch and a $\mathrm{VDAC_1}$, is added. In the steady-state with SEL = 1 and Path_1 selected, the TCO output frequency, F_{OUT1}, can be expressed as

$$F_{OUT1} = \frac{N}{R_1 C_1 ln(1/\alpha_1)} \tag{3.4}$$

where the $\mathrm{R_1C_1}$ branch is designed to have the same time product but exhibit a different TC from that of $\mathrm{R_0C_0}$ branch.

The first-order temperature compensation is achieved by modulating the SEL signal with the first-order $\Delta\Sigma$ modulator. If R_0C_0 and R_1C_1 have opposite-sign TCs, the averaged V_{ERR} is forced to zero in steady-state due to the high loop gain of the FLL, and can be expressed as

$$\overline{V_{ERR}} = (1-\beta)V_{ERR0} + \beta V_{ERR1} = 0 \tag{3.5}$$

where V_{ERR0} and V_{ERR1} represent the error between the TCO output frequency and F_{OUT0} and F_{OUT1}, respectively, and β is the average of the pulse-density modulated SEL sequence. This equation can be rewritten as

$$(1-\beta)(F_{OUT} - F_{OUT0}) + \beta(F_{OUT} - F_{OUT1}) \cong 0 \tag{3.6}$$

$$F_{OUT} \cong (1-\beta)F_{OUT0} + \beta F_{OUT1} \tag{3.7}$$

assuming that R_0C_0 and R_1C_1 have similar time constants. There exists an optimum β (β_{OPT}) at which F_{OUT} is insensitive to temperature changes to the first order.

However, if R_0C_0 and R_1C_1 have different positive TCs, the temperature dependency of F_{OUT} cannot be compensated for by varying the average SEL sequence. To overcome this issue, the RC1_SIGN is added to the DECHOP signal logic, and by setting RC1_SIGN to

one, the sign of integrator G_M is reversed when SEL = 1, producing a negative sign in the second term of the averaged V_{ERR} equation, given by

$$\overline{V_{ERR}} = (1-\beta)V_{ERR0} - \beta V_{ERR1} = 0. \tag{3.8}$$

This equation can also be expressed as

$$(1-\beta)(F_{OUT} - F_{OUT0}) - \beta(F_{OUT} - F_{OUT1}) \cong 0 \tag{3.9}$$

$$F_{OUT} \cong \frac{(1-\beta)F_{OUT0} - \beta F_{OUT1}}{1-2\beta}, \tag{3.10}$$

assuming that $R_0C_0 \cong R_1C_1$. If SEL = 1, flipping the sign of integrator G_M reduces the loop gain of the FLL. However, in Section 3.4, it was found through simulation and measurement that the first-order TC compensation's optimal β (β_{OPT}) is a small value of approximately 0.02, due to the large TC ratio of R_1C_1 to R_0C_0. As a result, the degradation of the loop gain is negligible.

3.2.3 Trimming Procedure

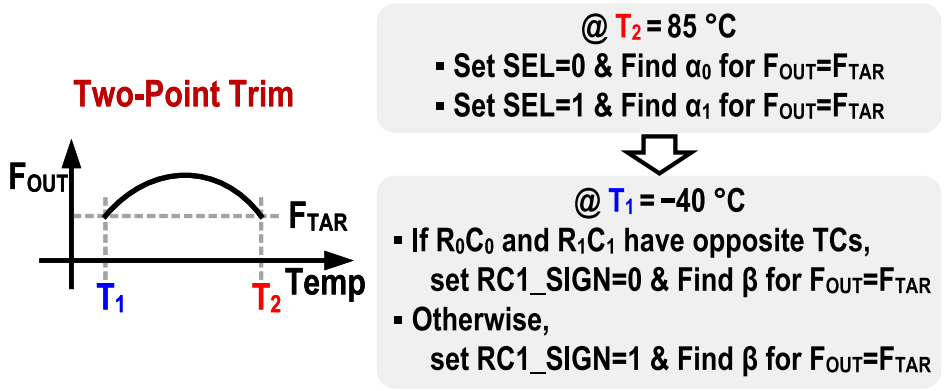


Figure 3.4: Two-point trimming logic.

Figure 3.4 illustrates the two-point trimming process. Initially, Path_0 is chosen by setting the SEL signal to zero. Then, a binary search is conducted for α_0 of VDAC_0 to attain the target frequency F_{TAR} with $F_{OUT} = F_{OUT0} = F_{TAR}$ at a temperature of 85 °C. Subsequently, Path_1 is selected by setting the SEL signal to one, and a similar search is performed for α_1 of VDAC_1 to achieve $F_{OUT} = F_{OUT1} = F_{TAR}$. The process is completed by setting the temperature to −40 °C. If R_0C_0 and R_1C_1 have opposite sign TCs, then RC1_SIGN is set to zero, otherwise to one. A binary search is then conducted for β that causes $F_{OUT} = F_{TAR}$.

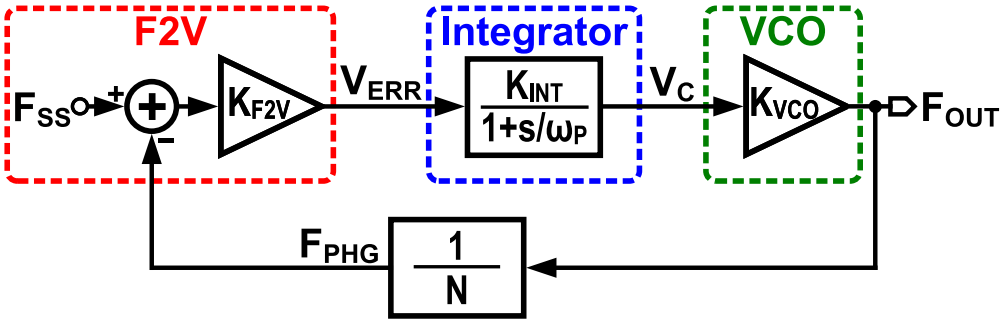


Figure 3.5: Linearized FLL model.

These steps provide alpha and beta value estimates, fine-tuned for optimal values. Finally, α_0, α_1, and β are truncated to 17-bit digital words D_{REF0}, D_{REF1}, and D_{SEL}, respectively. This trimming process is performed for both the main and reference TCOs.

3.2.4 FLL Design

The TCO's discrete-time operation can be represented as a linearized FLL, illustrated in Fig. 3.5, comprising a frequency-to-voltage converter (F2V), an integrator, and a VCO. This model is utilized to determine loop parameters and ensure stable closed-loop operation of the TCO. The two RC branches, modulated by signal SEL with an average density of β_{OPT}, act as a temperature-compensated RC branch that serves as F2V with the divided VCO clock F_{PHG} ($= F_{OUT}/\mathrm{N} = 1/T_P$) as input and the error voltage V_{ERR} ($= V_{RC} - V_{REF}$) as output during integration phase ($\Phi_{\mathrm{INT}} = 1$). F_{SS} is equivalent to F_{PHG} in the steady state. Since $R_0C_0 \cong R_1C_1$ and $\beta_{OPT} \sim 0.02$, the temperature-compensated RC branch's time constant is roughly equal to R_0C_0. When $\Phi_{\mathrm{CHG}} = 0$, V_{ERR} of F2V can be expressed as:

$$V_{ERR} = V_{RC0,DCHG} - V_{REF} = V_{DD}e^{-1/(R_0C_0F_{PHG})} - V_{REF}. \tag{3.11}$$

The transfer function of F2V can be derived as a gain of K_{F2V} where

$$K_{F2V} = \frac{dV_{ERR}}{dF_{PHG}} = \frac{V_{DD}}{R_0C_0F_{PHG}^2}e^{-1/(R_0C_0F_{PHG})} \tag{3.12}$$

$$= \frac{V_{DD}N^2}{R_0C_0F_{OUT}^2}e^{-N/(R_0C_0F_{OUT})}. \tag{3.13}$$

When $\Phi_{\mathrm{CHG}} = 1$, the V_{ERR} and K_{F2V} of F2V can be written as

$$V_{ERR} = V_{RC0,CHG} - V_{REF} = V_{DD}\left(1 - e^{-1/(R_0C_0F_{PHG})}\right) - V_{REF} \tag{3.14}$$

$$K_{F2V} = -\frac{V_{DD}N^2}{R_0 C_0 F_{OUT}^2} e^{-N/(R_0 C_0 F_{OUT})} \tag{3.15}$$

where K_{F2V} has the same magnitude of Eq. (3.15) but a negative sign.

The Miller effect, caused by C_{INT} and the second-stage voltage gain (refer to Fig. 3.3), results in the integrator having a dominant pole at its first-stage output. This can be represented as a simple one-pole system, as shown in Fig. 3.5, with K_{INT} and ω_P denoting the voltage gain and the dominant pole of the integrator, respectively. As the integrator operates exclusively during the integration phase, and its first-stage output is de-chopped by the DECHOP signal (see Fig. 3.3), the effective transconductance of its first stage $G_{M1,EFF}$ is equivalent to $0.2G_{M1}$ when $\Phi_{\text{CHG}} = 0$ and $-0.2G_{M1}$ when $\Phi_{\text{CHG}} = 1$, where G_{M1} is the transconductance of its first stage. The K_{INT} and ω_P are given as

$$K_{INT} = G_{M1,EFF} R_{O1} A_2 \tag{3.16}$$

$$\omega_P \approx \frac{1}{(A_2 + 1) R_{O1} C_{INT}} \tag{3.17}$$

where R_{O1} is the output impedance of the integrator's first stage, and A_2 is the voltage gain of its second stage.

From Fig. 3.5, the loop gain, $LG(s)$, is given by

$$LG(s) = K_{F2V} \frac{G_{M1,EFF} R_{O1} A_2}{1 + s(A_2 + 1) R_{O1} C_{INT}} \frac{K_{VCO}}{N} \tag{3.18}$$

where K_{VCO} is the voltage-to-frequency gain of the VCO. Due to the chopping/de-chopping operation, K_{F2V} and $G_{M1,EFF}$ have the same sign, irrespective of Φ_{CHG}, resulting in the loop maintaining negative feedback. The closed-loop bandwidth of the loop can be approximated by its unity gain frequency, denoted as ω_{UGF}, which is equal to

$$\omega_{UGF} \approx \frac{G_{M1,EFF} K_{F2V} K_{VCO}}{C_{INT} N}. \tag{3.19}$$

To achieve FLL stability and minimize $\Delta\Sigma$ quantization error, the ω_{UGF} value is typically set to approximately 1 kHz.

3.3 Circuit Implementation

The diagram of the R_1C_1 branch is illustrated in Fig. 3.6. It comprises a controllable resistor R_1, a capacitor C_1, a buffer for discharging/charging C_1, and an inverter for resetting C_1.

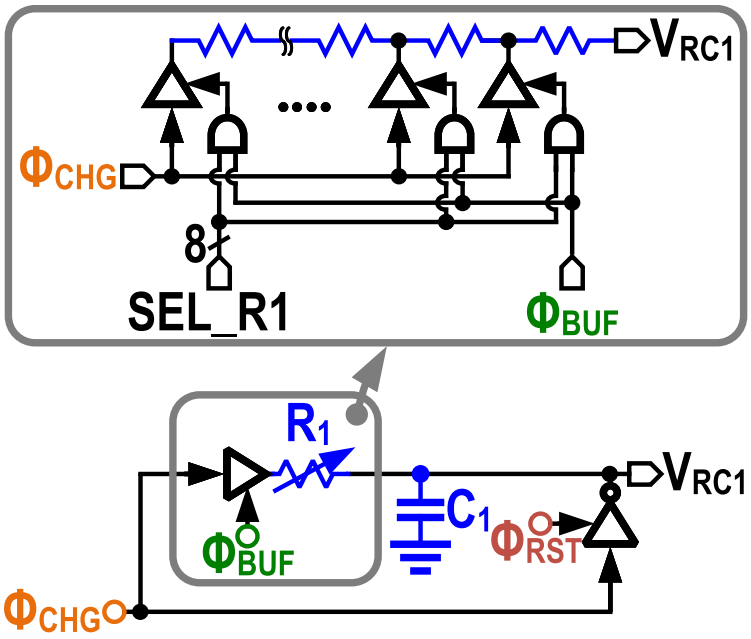


Figure 3.6: Schematic of the R_1C_1 branch.

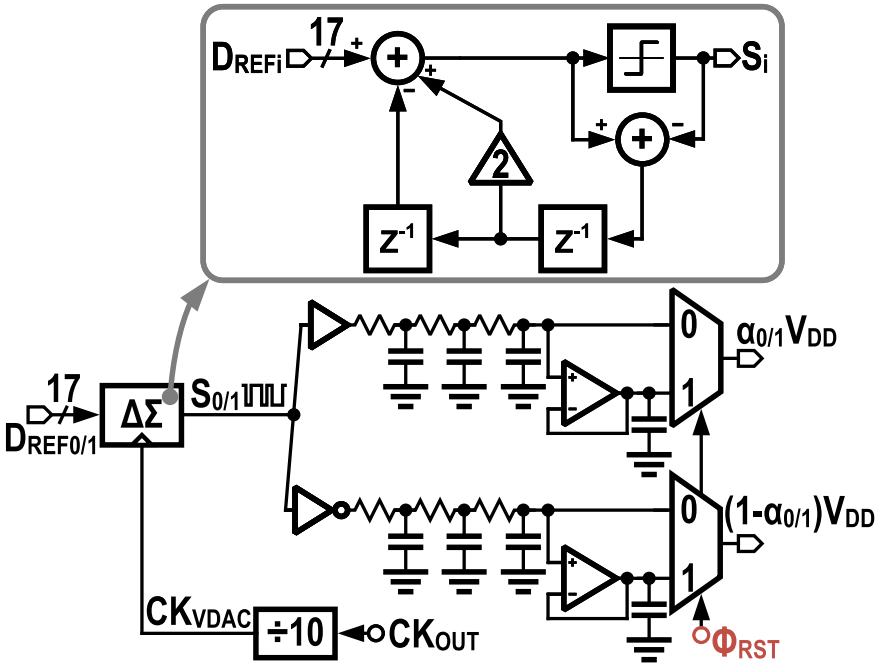


Figure 3.7: Schematic of the VDAC.

To cope with process variation of the resistor R_1, eight buffers are connected to eight taps of the segmented resistor R_1, and one of the buffers is chosen by 8-bit select signal SEL_R1. This programmability allows R_1C_1 to have comparable time constant to that of R_0C_0.

The reference voltage (V_{REF}) in Fig. 3.3 is produced through differential $\Delta\Sigma$-DACs illus-

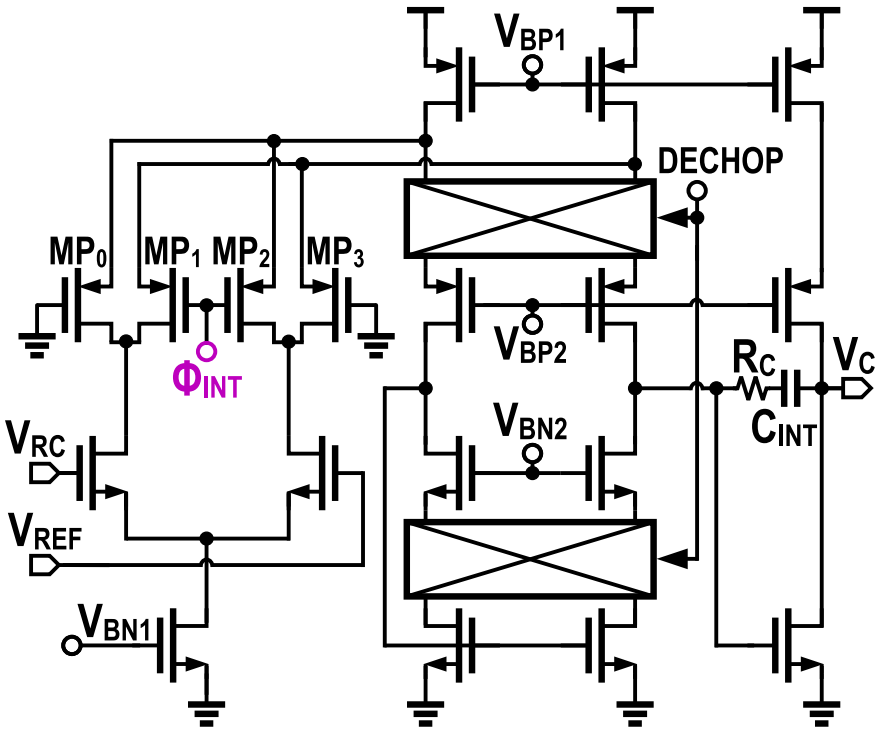


Figure 3.8: Schematic of the $G_M - C$ integrator.

trated in Fig. 3.7. The 17-bit digital input ($D_{REF0/1}$) is first truncated to 1-bit via a second-order $\Delta\Sigma$ modulator that operates at a switching frequency of $F_{OUT}/10$ (= 10 MHz). Using a buffer and an inverter, it is then transformed into a pulse-density modulated sequence $S_{0/1}$. This process provides superior reference voltage accuracy (better than eight ppm) and output frequency tuning resolution (22.5 ppm). To avoid potential aging effects caused by additional aging-susceptible components for other analog voltage level generation, the supply and ground voltage levels (V_{DD} and V_{SS}) are used for the 1-bit sequence conversion. The $\Delta\Sigma$ modulator employs the error feedback architecture shown in Fig. 3.7 and generates second-order shaped quantization error, which is suppressed by third-order RC low-pass filters (LPFs). The differential VDAC outputs can be expressed as $\alpha_{0/1}V_{DD}$ and $(1-\alpha_{0/1})V_{DD}$, where $\alpha_{0/1}$ denotes the average of sequence $S_{0/1}$. To avoid charge sharing between the parasitic capacitor at the integrator input and the LPF capacitors, the unity gain buffers are connected to V_{REF} in Fig. 3.3 during $\Phi_{RST} = 1$.

The integrator utilizes a two-stage $G_M - C$ topology as shown in Fig. 3.8. The RC branches are chopped at Φ_{CHG}, and the first-stage output of the integrator is de-chopped by the DECHOP signal to remove offset and flicker noise, thus improving the temperature stability and Allan deviation of the TCO. The PMOS switches (MP_0, MP_1, MP_2, and MP_3) steer the tail current equally to the folding node when $\Phi_{INT} = 0$, preventing integration of

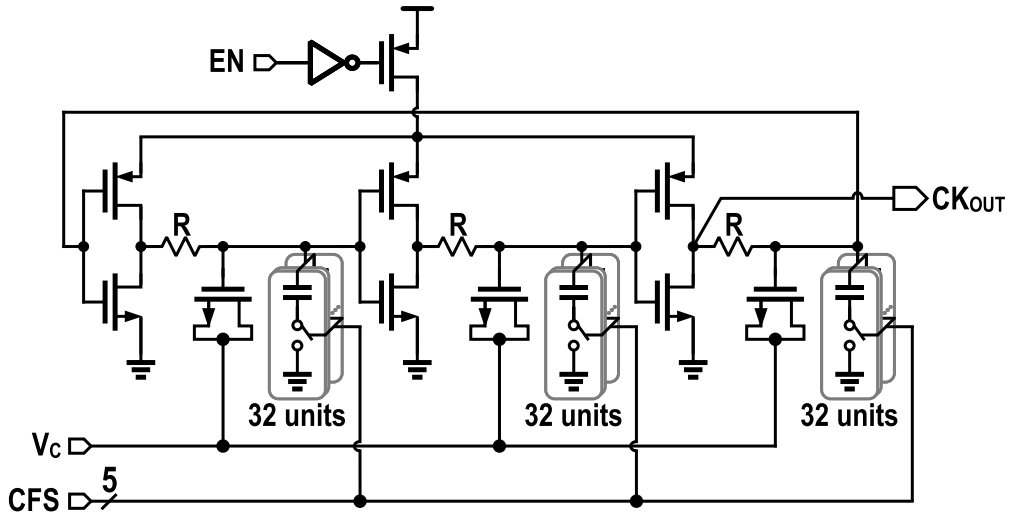


Figure 3.9: Schematic of the voltage-controlled ring oscillator.

the input signal. Integration is enabled by turning off MP_1 and MP_2 when $\Phi_{INT} = 1$. The mismatch between MP_{0-3} introduces an additional input-referred integrator offset, which the chopping/de-chopping operation removes. The second stage of the integrator enhances the gain and establishes a large integrator time constant by using a capacitor $C_{INT} = 8.8$ pF. The Miller effect results in a dominant pole at the output of the first stage, stabilizing the loop and limiting the loop bandwidth to ∼1 kHz, which is necessary to suppress the shaped quantization error of ΔΣ modulators. To remove the RHP-zero caused by the Miller effect, a resistor R_C is used. The high gain of the integrator allows the DC loop gain to be more than 126 dB, sufficient to suppress the supply and temperature sensitivity of the VCRO effectively.

Figure 3.9 displays the VCO diagram, which consists of three delay elements implemented with an inverter, a poly resistor, and controllable capacitors, along with a power-gating PMOS switch. The resistor and capacitors' sensitivity primarily determines the delay element's temperature sensitivity. The VCO's nominal frequency is coarsely tuned to 100 MHz using 5-bit binary-weighted MOM capacitor arrays and finely tuned using MOS varactors. When the reference TCO is unused, the power-gating PMOS switch is turned off to reduce leakage current.

The schematic of the on-chip aging calibration logic is depicted in Fig. 3.10. A feedback loop is utilized to counteract the frequency drift caused by aging in the main oscillator, which locks the frequency of the main temperature-compensated oscillator (TCO) to a less-aged reference TCO. The frequency error is measured by counting the number of main oscillator cycles within 2^{16} periods of the reference clock CK_{PHG}. This clock is obtained by dividing

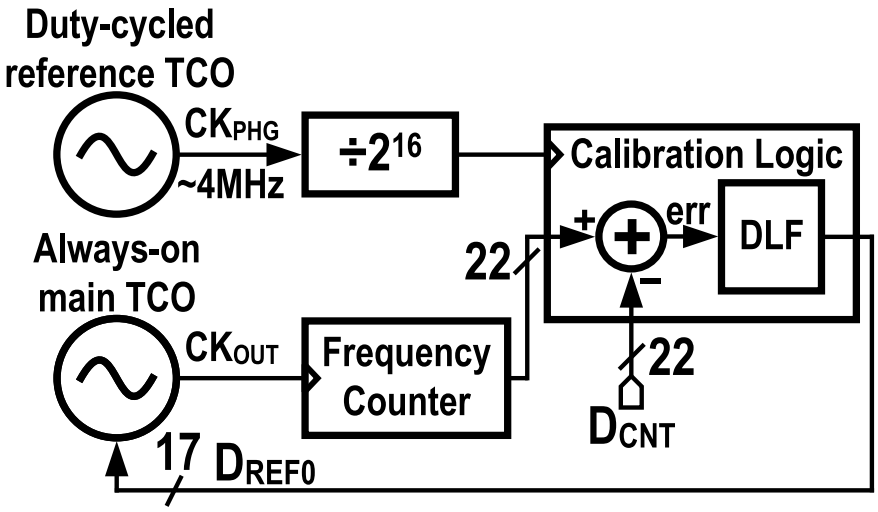


Figure 3.10: On-chip aging calibration logic.

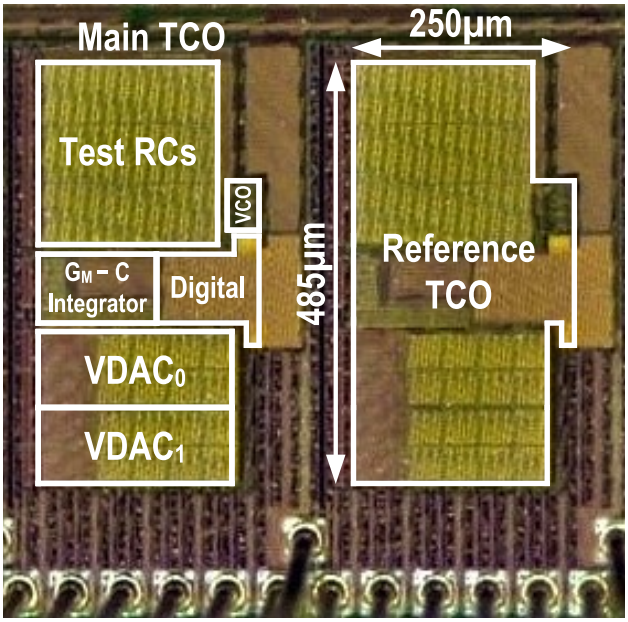


Figure 3.11: Die micrograph.

the reference TCO output clock by 25. Then, the ideal count represented by the 22-bit D_{CNT} is subtracted from the counter output. The resulting error is accumulated by the digital loop filter (DLF) and is used to adjust the 17-bit digital word D_{REF0}, which tunes the main oscillator's frequency.

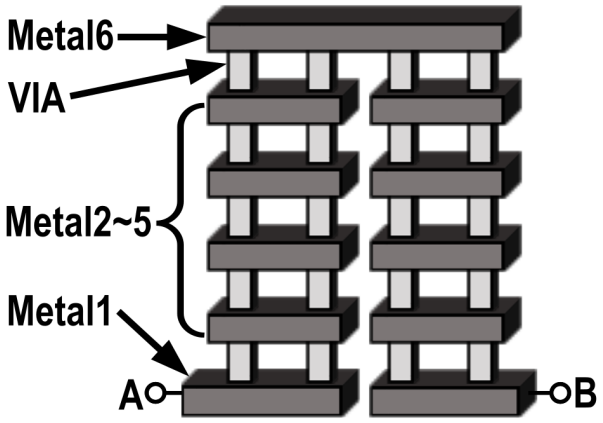


Figure 3.12: Unit segment of the VIA resistor.

3.4 Measurement Results

The TACO prototype was produced using a 65-nm CMOS process and packaged in a plastic QFN package. The die micrograph in Fig. 3.11 displays the prototype's active area, which measures 0.22 mm^2, and includes the main and reference TCOs. To fully characterize the impact of resistor aging on frequency drift, twelve RC branches with different resistors (two poly resistors, two diffusion resistors, four silicied poly/diffusion resistors, two composite resistors, a metal interconnect resistor, and a VIA resistor) were implemented in the prototype with the option of choosing any one or two RC branches out of them. Figure 3.11 illustrates the test RC branches with a combined area of 0.047 mm^2, including the twelve RC branches. Each RC branch comprises a 50-kΩ resistor and a 7.2-pF capacitor implemented with a MOM capacitor situated beneath a MIM capacitor. If we count only the two RC branches that use n-poly and VIA resistors utilized in the experiment, the total area is reduced to 0.15 mm^2. The VIA resistor comprises 7980 unit segments, each occupying an area of 3500 μm^2. Fig. 3.12 shows one such unit segment, which consists of VIA stacks and metal layers 1 to 6. Double VIAs connect the upper and lower routing metal layers instead of a single VIA to enhance reliability and minimize yield loss due to VIA failures.

To operate correctly, the prototype necessitates correspondingly three external power supplies with voltage levels of 1.15 V, 1 V, and 1 V for the analog, digital, and VCO blocks, respectively. The TCO's total power consumption is 121 μW, and its power allocation is illustrated in Fig. 3.13. Around 58.0 μW (approximately 48%) of the TCO power consumption is consumed by digital blocks like dividers, phase generators, and $\Delta\Sigma$ modulators (DSMs) from the 1-V supply. At the same time, the VCO accounts for 32% of the TCO power consumption. The RC branches, VDAC unity-gain buffers, and the integrator use

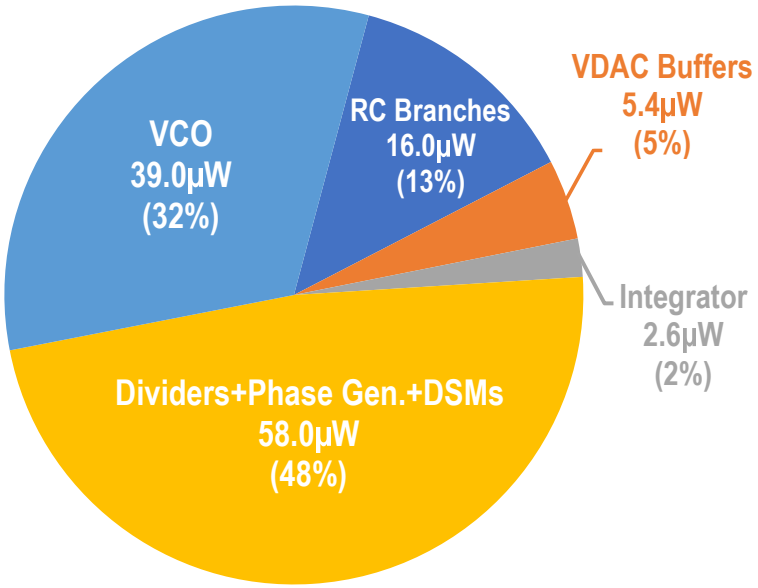


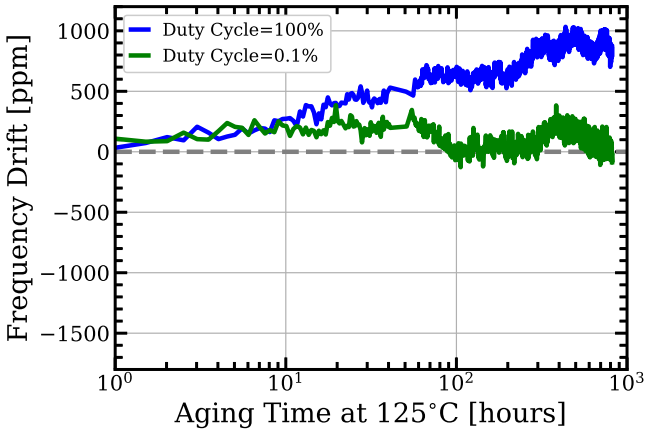
Figure 3.13: Power breakdown of the single TCO.

20% of the TCO power consumption from the 1.15-V supply. The average power consumption of the TACO (including main and reference TCOs) is 142 μW, with 21 μW of the power consumption coming from the leakage current of the disabled reference TCO biased by the external supplies. When aging compensation is activated, the TACO's power consumption rises to 263 μW. Still, the duty cycle for compensation in the experiment is only 0.1%, having an insignificant effect on the TACO's average power consumption.

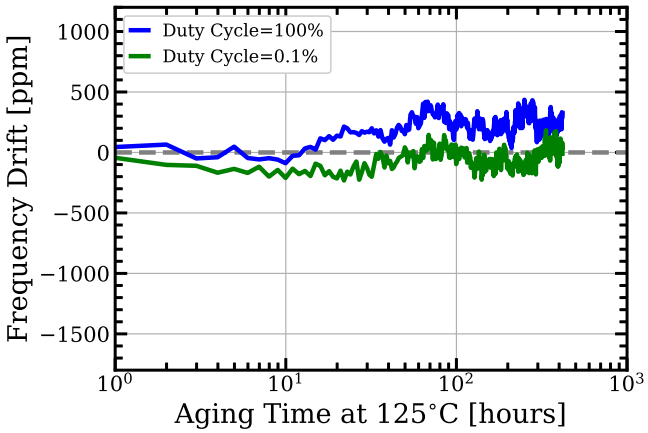
3.4.1 Aging Test using Standalone Resistor

An accelerated aging test was conducted on the TCO with different resistors to evaluate its aging behavior. During the test, only one resistor was enabled at a time. The long-term frequency drift of the always-on TCO with an n-poly resistor was within ±1030 ppm after 817 hours at 125 °C, as shown in Fig. 3.14(a). On the other hand, the TCO with a duty cycle of 0.1% exhibited a frequency drift of within ±390 ppm, indicating that duty cycling can reduce the aging effect. The TCOs using VIA resistors showed a long-term frequency drift of within ±440 ppm when always on and within ±230 ppm when duty-cycled at 0.1% after 418 hours of testing, as depicted in Fig. 3.14(b). These results suggest that duty cycling reduces the aging effect.

Based on the measurements of the aging behavior of TCOs with different types of resistors, TCOs with p-poly resistors exhibited the worst frequency drift of ±5200 ppm, as shown in Fig. 3.1. On the other hand, duty-cycled TCOs using VIA or n-poly resistors demonstrated



(a)



(b)

Figure 3.14: Measured frequency drift of TCOs when always-on and with 0.1% duty cycle using (a) n-poly resistors and (b) VIA resistors.

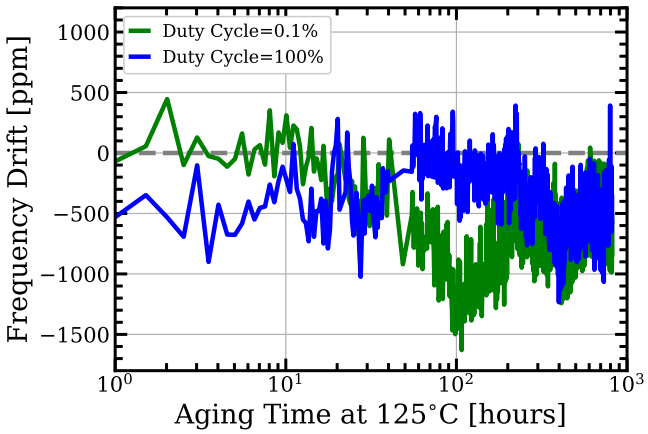


Figure 3.15: Measured frequency drift of TCOs using VIA resistors without chopping and without alternating current direction in RC branches.

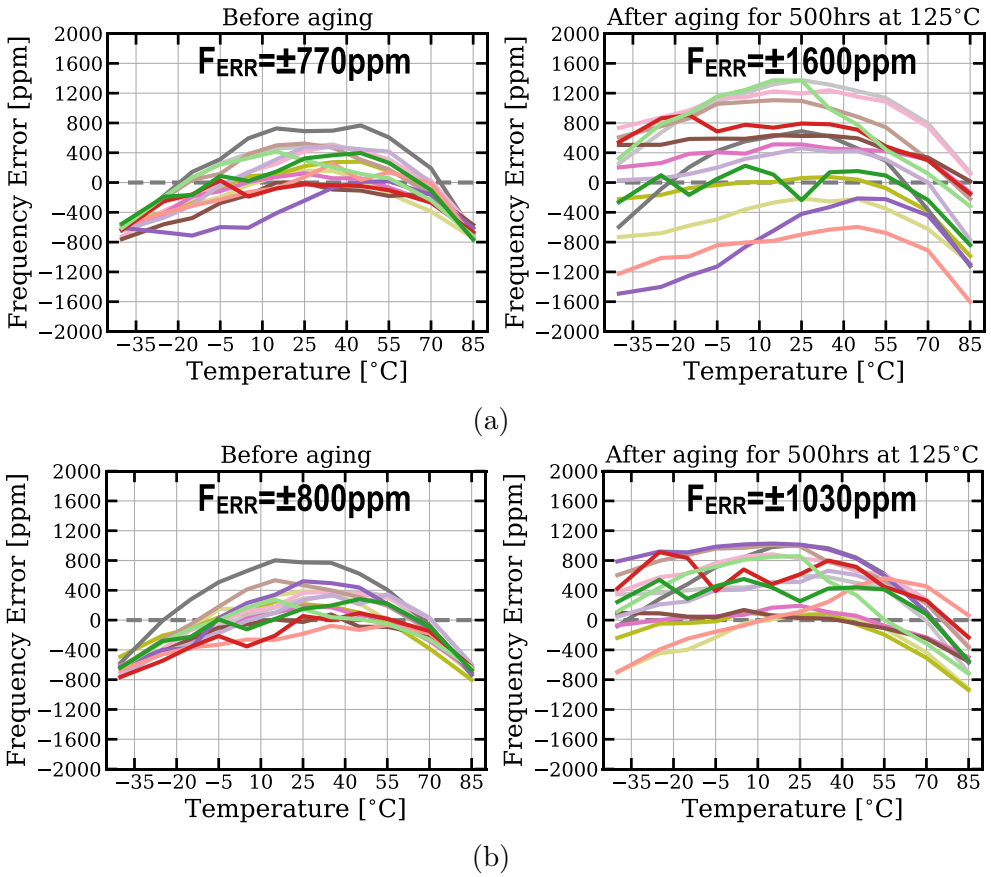


Figure 3.16: Measured frequency inaccuracy of main TCOs using n-poly and VIA resistors before and after aging (a) without the aging compensation and (b) with the compensation.

robustness in maintaining a stable frequency under aging conditions, as shown in Fig. 3.14.

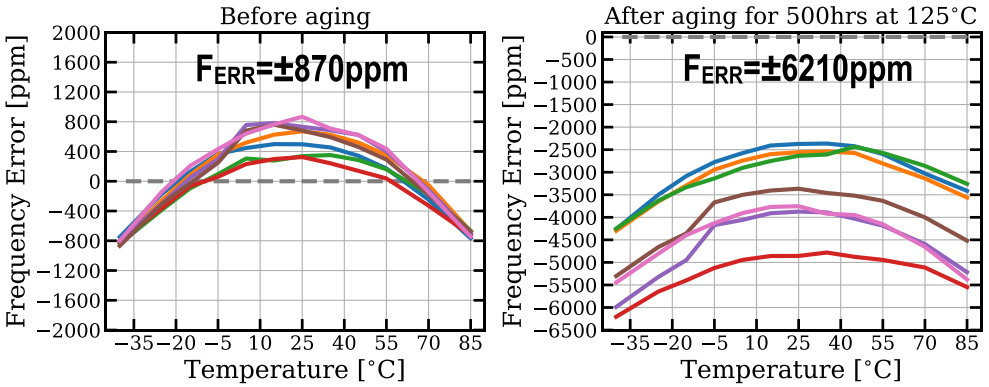
To investigate the impact of chopping/de-chopping operation and alternating current direction through the RC branches on the frequency, the frequency drift of TCOs using VIA resistors without these techniques was measured for 817 hours of aging at 125 °C, as illustrated in Fig. 3.15. The worst frequency drift was ±1630 ppm for the TCO with a duty-cycle of 0.1% and within ±1230 ppm for the 100% duty-cycled TCO. These results demonstrate a significant frequency drift compared to the measurements in Fig. 3.14(b), indicating that the chopping operation and alternating current direction through RC branches can reduce the aging effect caused by long-term instability of integrator offset and DC-current-induced EM.

3.4.2 Aging Test after Two-Point Trim

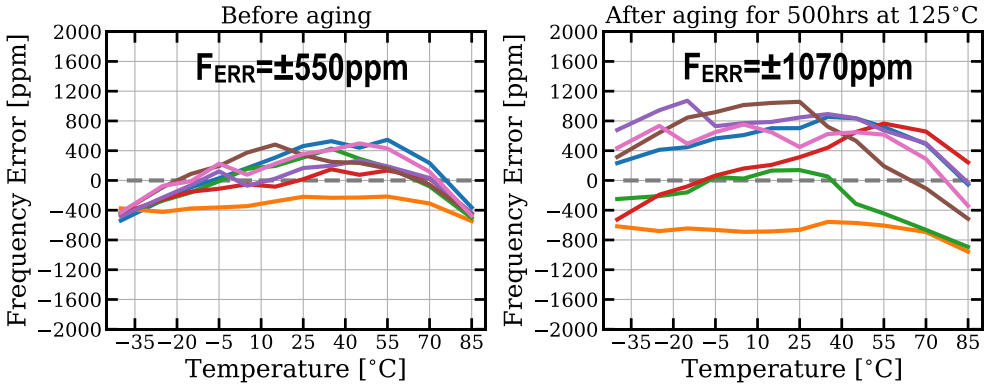
The selection of resistors for the main and reference TCOs was based on the aging behavior of the TCOs, as measured using a standalone resistor. N-poly and VIA resistors were chosen as R_0 and R_1, respectively. The digital control words D_{REF0}, D_{REF1}, and D_{SEL} were determined for each sample by trimming the TCOs at 85 °C and −40 °C for $F_{OUT} = F_{TAR} = 100$ MHz. The β_{OPT} value was calculated to be ∼0.02, as the ratio of R_1C_1 TC (1000 ppm/°C) to R_0C_0 product (20 ppm/°C) was found to be large. The accelerated aging test was performed on the two-point trimmed TCOs for 500 hours at 125 °C, and the results from 14 samples are shown in Fig. 3.16. Before aging, the frequency accuracy of the main TCOs was ±770 ppm, but it degraded to ±1600 ppm after aging, indicating an 830 ppm degradation due to aging (Fig. 3.16(a)). However, with the proposed aging compensation, which involves locking the frequency of the always-on main TCO to that of a 0.1% duty-cycled reference TCO at one-hour intervals, the frequency accuracy of the main TCOs was ±800 ppm before aging. It degraded to ±1030 ppm after aging, indicating degradation of only 230 ppm due to aging (Fig. 3.16(b)). Figure 3.17 shows the results of an aging test conducted over seven samples when a p-poly resistor replaces R_0 of the primary TCOs. This test provides a fair comparison to the state-of-the-art since most TCOs reported in the literature use p-poly resistors [10, 12, 14, 15, 28]. Before aging, the inaccuracy of uncompensated main TCOs is ±870 ppm, while after 500 hours of aging, it degrades to ±6210 ppm, as shown in Fig. 3.17(a). The degradation in accuracy appears to be mainly due to the aging of the p-poly resistor, as indicated by the comparison with the results shown in Fig. 3.16(a). However, with compensation, the main TCOs have a frequency accuracy of ±550 ppm before aging, which degrades to ±1070 ppm after the aging test. The compensation reduces the degradation to only 520 ppm (see Fig. 3.17(b)).

3.4.3 Supply Sensitivity and Output Clock Performance

Figure 3.18 shows that the supply sensitivity of 10 samples, measured using n-poly and VIA resistors, was 1440 ppm/V over a supply range of 1.1 to 1.3 V. The Allan deviation for a 1-second stride without chopping was found to be 40 ppm, but it was reduced to 8.1 ppm with chopping, as depicted in Figure 3.19. The measured output period jitter for the closed-loop TCO was 5.1 ps_{rms}, which is lower than the 5.8-ps_{rms} period jitter of the open-loop ring oscillator (refer to Figure 3.20). The dominant contributor to the period jitter was found to be the ring-based VCO.



(a)



(b)

Figure 3.17: Measured frequency inaccuracy of main TCOs using p-poly and VIA resistors before and after aging (a) without the aging compensation and (b) with the compensation.

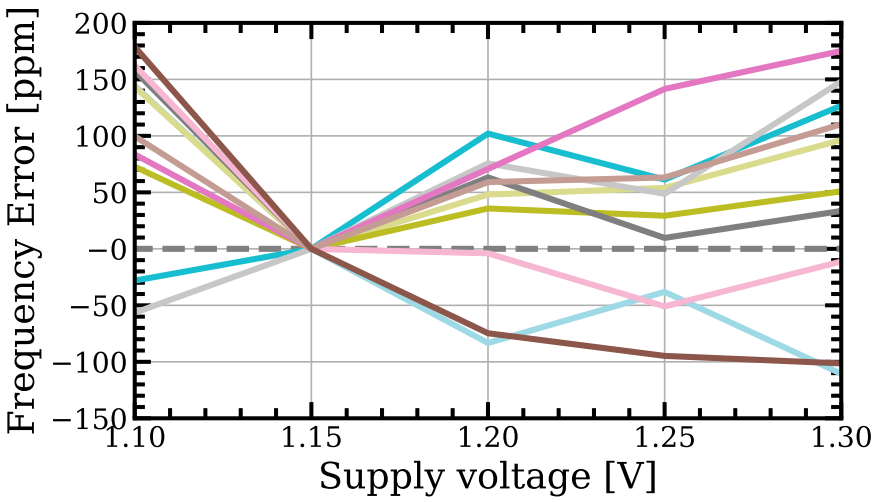


Figure 3.18: Measured supply sensitivity.

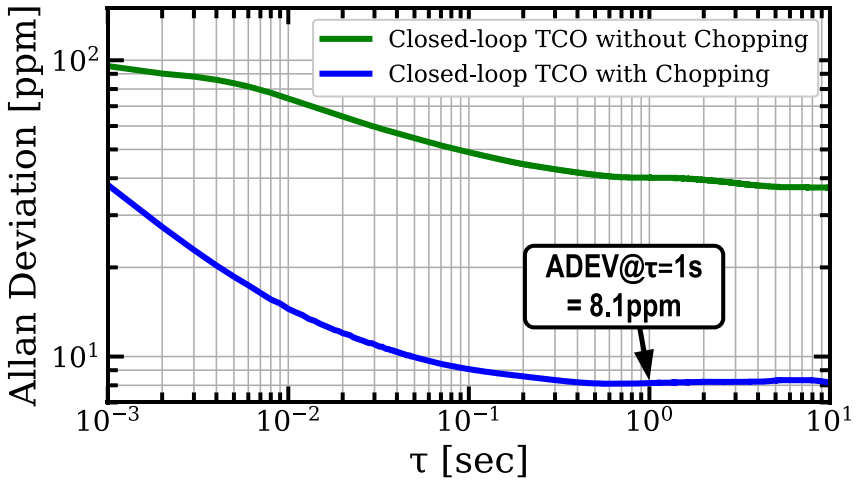
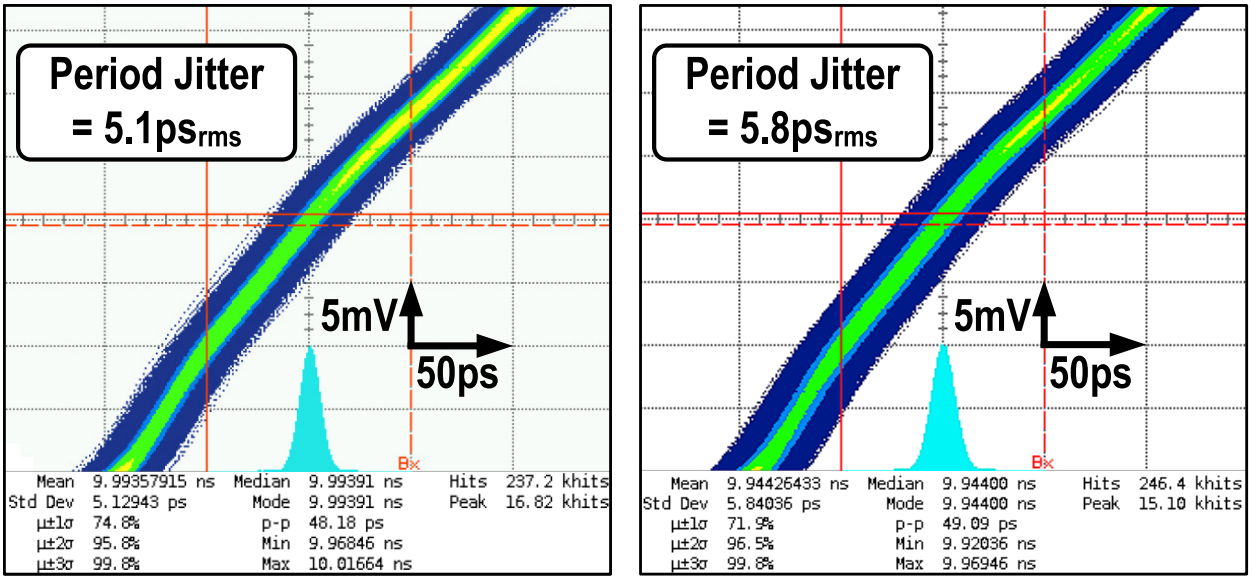


Figure 3.19: Allan deviation.



(a) (b)

Figure 3.20: Period jitter of (a) closed-loop TCO and (b) open-loop ring oscillator.

Table 3.1: Performance summary and comparison with state-of-the-art on-chip RC oscillators.

	This Work		Ji [28] ISSCC22	Gurleyuk [14] JSSC22	Khashaba [10] JSSC21	Jiang [12] ISSCC21	Choi [13] JSSC21	Park [15] CICC21
Process	65nm		180nm	180nm	65nm	180nm	65nm	65nm
Frequency [Hz]	100M		2.3M	16M	32M	16M	28M	100M
Power [W]	142μ		7.6μ	220μ	34μ	158μ	142μ	101μ
Power Efficiency [μW/MHz]	1.4		3.3	13.8	1.1	10	5	1.0
P-poly Resistor Used	No	Yes	Yes					
Aging Compensation	Yes		No					
Frequency Inaccuracy w/o Aging [ppm]	±770	±870	±1550†	±385	±530	±400	±200	±140
Frequency Inaccuracy w/ Aging [ppm] Uncompensated/ Compensated	±1600/ ±1030	±6210/ ±1070	-					
Trim Points	2		2	2	2	1+Batch	2+Batch	3
Temp. Range [°]	−40 to 85		−40 to 125	−45 to 85	−40 to 85	−45 to 85	−40 to 85	−40 to 95
Supply Sensitivity [%/V]	0.14		0.51	0.12	0.008*	0.2	0.29	0.0083*
Supply Range [V]	1.1 to 1.3		1.3 to 2.0	1.6 to 2.0	1.1 to 2.3	1.6 to 2.0	0.85 to 1.05	1.1 to 2.5
# of Samples	14	7	11	20	6	18	16	20
Period Jitter [ps_{rms}]	5.1		-	39.9	24	10.2	7	13.3
ADEV@τ=1s [ppm]	8.1		9	1	2.5	0.8	2	1.6
Area [mm^2]	0.15*		0.07	0.3	0.18**	0.14	0.06	0.19**

* 0.22 mm^2 including 12 RC branches ** With on-chip LDO † Worst case

The performance of the TACO is summarized in Table 3.1, where it is also compared to state-of-the-art RC oscillators. The proposed TACO exhibits a good power efficiency of 1.4 μW/MHz, and its frequency inaccuracy is comparable to that of state-of-the-art oscillators, even in the presence of aging.

3.5 Conclusion

The presented RC oscillator is a temperature- and aging-compensated design that mitigates the long-term drift of the main oscillator by periodically locking its frequency to that of a less-aged reference oscillator. To improve the long-term stability of the oscillator, several techniques are employed. The first technique involves using higher activation energy resistors because they exhibit smaller resistivity shifts under temperature stress. The second technique involves switching dual RC branches to mitigate the stress from DC-current-induced electromigration. Finally, the duty-cycling method is employed to slow down the reference oscillator's aging rate.

Thanks to these techniques, the proposed TACO achieves a frequency inaccuracy of $\pm$1030ppm from -40 °C to 85 °C, even after 500 hours of accelerated aging at 125 °C. The oscillator exhibits a period jitter of 5.1 $\mathrm{ps_{rms}}$ and a power efficiency of 1.4 μW/MHz. The two-point trimmed FLL-based oscillator is designed using n-poly and VIA resistors. Its performance is suitable for use in low-power micro-controller applications that require good frequency accuracy even when aging effects are present.

Overall, the proposed TACO design demonstrates the effectiveness of the presented techniques in achieving high stability and accuracy in RC oscillators, making it a promising candidate for low-power and low-cost applications.

CHAPTER 4

CONCLUSION

Fully-integrated RC-based frequency references have gained popularity as alternatives to bulky crystal or MEMS oscillators in many applications due to their low power consumption, small area, and lack of need for costly off-chip components [6]. However, their poor frequency accuracy resulting from their non-linear temperature sensitivity and aging has limited their usage to systems that can tolerate large frequency inaccuracy ($\sim$1%).

Several efforts are underway to improve the accuracy and extend their use to applications requiring medium to high stability clock sources. However, these efforts face challenges such as circuit-level imperfections [9], large uncompensated high-order temperature coefficients (TCs) [10], poor power efficiency [11–14], or the need for resistors with opposing TCs [10] that may not be available in all processes. Furthermore, even though some literature have demonstrated a good short-term inaccuracy of $<\pm$600 ppm [9–16], their commercial deployment is limited by the lack of information about their aging behavior and the inability to guarantee their performance over their lifetime.

In the first part of this work, we presented techniques to reduce the non-linear temperature sensitivity of fully-integrated CMOS RC oscillators and proposed methods for performing first- and second-order temperature compensation without the need for resistors with opposite TCs [15, 16]. Using the proposed three-point digital trim, a prototype 100-MHz FLL-based RC oscillator fabricated in a 65-nm CMOS process achieves an inaccuracy of $\pm$140 ppm over -40 °C to 95 °C, 83-ppm/V voltage sensitivity, 1.3-ppm Allan deviation floor, and 1-μW/MHz power efficiency. When only a single-point trim is performed using multiple linear regression model obtained from strong correlation between three switched resistors, the frequency inaccuracy is $\pm$587 ppm over -40 °C to 95 °C.

Second, in order to address the aging issue, we proposed a temperature- and aging-compensated RC oscillator (TACO) in which the long-term drift of the main oscillator is compensated by periodically locking its frequency to that of the less-aged reference oscillator. A prototype 100-MHz RC oscillator fabricated in a 65-nm CMOS process achieves an inaccuracy of $\pm$1030 ppm from from -40 °C to 85 °C after 500 hours of accelerated aging at 125 °C, with 5.1-ps_{rms} period jitter and a power efficiency of 1.4 μW/MHz.

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