GROWTH AND CHARACTERIZATION OF GALLIUM ARSENIDE PHOSPHIDE AND
GALLIUM PHOSPHIDE ON SILICON FOR III-V/SI MULTI-JUNCTION SOLAR CELLS

BY

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DISSERTATION

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ABSTRACT

Solar photovoltaic (PV) technologies offer the ability to provide a significant percent of the world's increasing energy demand while reducing overall greenhouse gas emissions. At the same time, PV technology is critical for the future of power generation in space. Silicon single-junction (1J) solar cells dominate the terrestrial solar market due to high production efficiencies and low material and processing costs from decades of investment. However efficiency is a key driver to further reduce the cost of PV technology and little room remains to improve the efficiency of Si toward its theoretical limit. Multi-junction (MJ) solar cells using a combination of III-V compound semiconductors achieve much higher efficiencies through tailoring bandgaps of sub-cells, leading to their utilization in space technology. Nevertheless, III-V solar cells are hindered by small-diameter, high-cost substrates, excluding their use in terrestrial power generation and placing a barrier to pursuing a greater variety of space missions. Through epitaxial integration of III-V semiconductors on Si, there is great potential to dramatically reduce the cost of III-V MJ cells and to realize competitive, high-efficiency solar cells for both space and terrestrial power.

While epitaxial III-V/Si MJ solar cells offer the possibility of a much-desired combination of high efficiency and low cost, the difficulty of growing high-quality III-V materials on Si substrates has left the potential of this PV technology unfilled. The combination of a ~1.7 eV III-V top cell and a ~1.1 eV Si bottom cell is close to the ideal double-junction (2J) bandgap pairing and has a > 25% (relative) higher theoretical maximum efficiency than for Si by itself. However, epitaxial III-V/Si MJ solar cells have yet to demonstrate efficiency higher than Si 1J solar cells. Extended defects resulting from crystal mismatches between III-V materials and Si hamper III-V sub-cell performance, and reducing the densities of these defects is critical to advancing epitaxial

III-V/Si technologies. The larger lattice constants for III-V materials than for Si inevitably cause threading dislocations to form that extend through III-V sub-cell(s). Gallium Arsenide Phosphide ($GaAs_yP_{1-y}$) is an ideal partner to Si due to possessing a tunable direct bandgap from $1.42 - 2.01$ eV and the smallest lattice mismatch to Si for ~1.7 eV III-V materials (~3.1%). Gallium Phosphide (GaP), with the closest lattice constant to Si for III-V materials, offers a convenient starting point for III-V epitaxial growth on Si before further expanding the lattice constant with compositional grading of $GaAs_yP_{1-y}$.

Obtaining low defect densities in ~1.7 eV $GaAs_{0.77}P_{0.23}$ (GaAsP) has remained challenging with threading dislocation densities (TDD) typically around an order of magnitude higher than desired for high performance (targeting $\leq 1 - 2 \times 10^6$ cm^{-2}). More troubling is that relaxed GaP on Si can result in TDD $> 10^7$ cm^{-2}, even though the lattice mismatch is less than an eighth of that for ~1.7 eV GaAsP. In this dissertation, I focus on defect management for relaxed GaP and GaAsP to improve material quality and advance GaAsP/Si 2J solar cell development. To this end, I investigated defects in GaP and determined growth strategies to reduce TDD to the lowest reported values I am aware of for both *p*- and *n*-type relaxed GaP on Si. I observed a strong dependence of TDD with doping and demonstrated methods to reach parity for relaxed *p*- and *n*-GaP on Si. For the GaAsP top cell I identified additional performance-damaging defects and strategies to mitigate them to realize high-current top cells. As a result, my collaborators and I realized the highest reported efficiencies for both GaAsP/Si 2J and ~1.7 eV GaAsP 1J solar cells on Si. Lastly, I studied radiation hardness and temperature-dependent device performance of ~1.7 eV GaAsP solar cells to broaden the space testing literature for this material.

ACKNOWLEDGMENTS

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Soli Deo Gloria

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CHAPTER 1

INTRODUCTION

Ever-increasing energy demands for human civilization and for technological advancement have made energy production one of the most important topics of the current era. However, it has become clear that the world's continued use of fossil fuels as the primary energy producer is not a viable long-term solution: the supply of fossil fuels is finite and, more importantly, the contribution of fossil fuels to climate change endangers the world population. To meet rising energy demand while limiting environmental damage, it is in our best interest to continue implementing new renewable energy generation capacity and to transition from reliance on fossil fuels to utilization of a variety of renewable energy sources. Due to the abundance of incident solar energy on the Earth, photovoltaic (PV) solar cells, which directly convert light into electricity, are an attractive option to supply an increasing market share. Indeed, solar cell deployment increased rapidly in recent years with the most new installed generation capacity among renewable technologies. This has amounted to installed capacity (total energy share) of 122.9 GW (4%) in the United States and 942 GW (5%) globally [1].

Decreasing solar cell cost per watt has driven this promising growth, making solar cells cost-competitive in comparison to fossil fuels. Among solar cell technologies, Si solar cells have dominated the terrestrial market for solar energy production on Earth. Si solar cells have benefitted from the well-established silicon microelectronics industry and years of solar cell production experience to decrease solar cell module costs. However, as module costs decrease, the role of non-module costs such as installation and support structures become an increasing fraction of the total cost, making further cost decreases more challenging. Instead, the cost per watt reduction

strategy shifts to increasing the module efficiency such that each module is producing more energy. Higher efficiency modules require less area for a given power, and thus these solar installations require less overall area and equipment for a given generation capacity. The lower area reduces both module costs (fewer modules) and non-module costs (less land use, support equipment, installation labor, etc.).

As shown in Fig. 1.1 for record solar cell efficiencies [2], the best 1-sun efficiency of Si solar cells (blue filled) hit a plateau near 25% over 20 years ago and the current record of 26.7% was set over 5 years ago [3], [4]. The highest efficiency of an ideal 1J solar cell is described by the Shockley-Queisser limit, which accounts for absorption and thermalization losses [5]. The choice of bandgap energy (E_G) for the 1J solar cell material determines the relative losses from absorption and thermalization. Under Shockley-Queisser assumptions, all photons with energy higher than E_G are absorbed while photons with energy lower than E_G are not absorbed. Therefore, materials with higher E_G suffer more from absorption loss resulting in lower current generation. Thermalization of generated carriers from higher energy states relaxing to band edge states leads
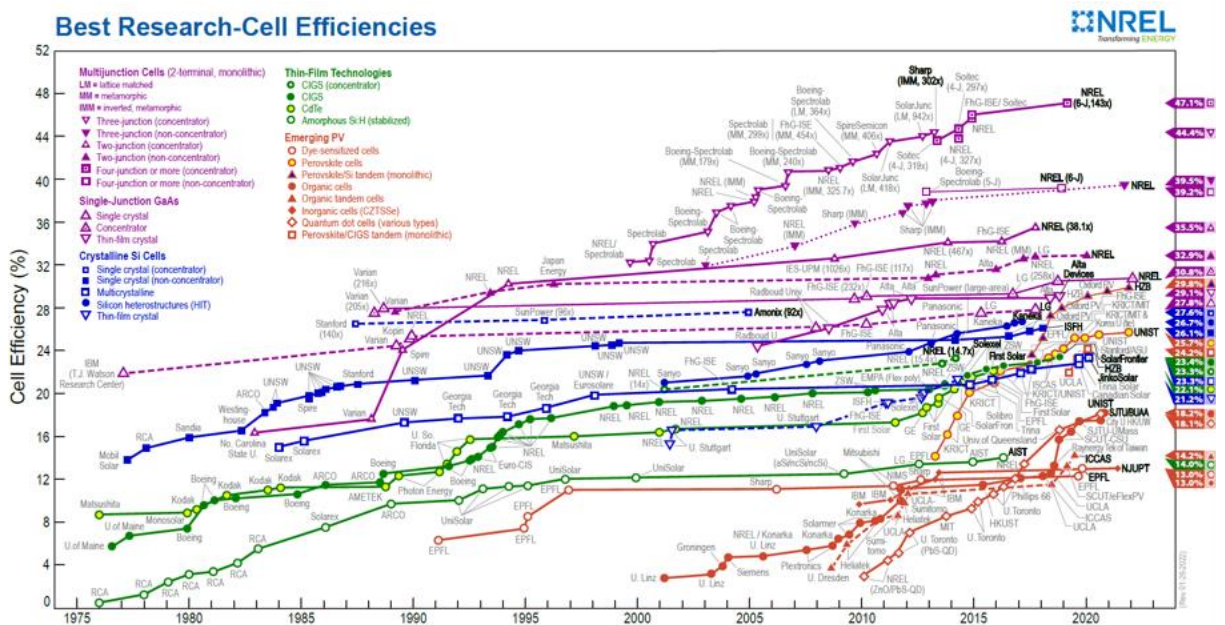
Fig. 1.1: Certified record solar cell efficiencies under the AM1.5G spectrum from 1976 to present. Si technologies are in blue while III-V technologies are in purple. From Ref. [2].

to lower voltage for collected carriers than for the original generated carriers. Therefore, materials with higher E_G suffer less from thermalization loss as the higher E_G translates to higher collected voltage. Balancing tradeoffs from absorption and thermalization losses results in a peak efficiency of ~31% for E_G of ~1.3 eV [6]. As such, little room remains for further improvement of Si single-junction (1J) solar cells toward the theoretical limit of 29.4% (calculation also includes losses from Auger recombination that are significant for Si) [7].

The Shockley-Queisser 1J limit can be surpassed by stacking materials with different E_G as a multi-junction (MJ) solar cell. MJ solar cells split the incident solar spectrum between sub-cells to reduce thermalization losses by better matching the incident photon energy with a sub-cell E_G. The highest E_G sub-cell (i.e. the top cell) faces the incident solar spectrum, absorbing the highest energy photons and allowing lower energy photons to pass through the top cell to the sub-cells underneath. In the same manner, each sub-cell observes a filtered solar spectrum without absorbed photons from the above sub-cells (see Fig. 1.2 for simple example). III-V solar cell efficiencies (purple in Fig. 1.1) far exceed that of other solar technologies due to the prominence of III-V MJ technologies with tailored sub-cell E_G combinations. III-V MJ solar cells have achieved AM1.5G efficiencies up to 39.5% (1-sun) [8] and 47.1% (with concentration) [9].
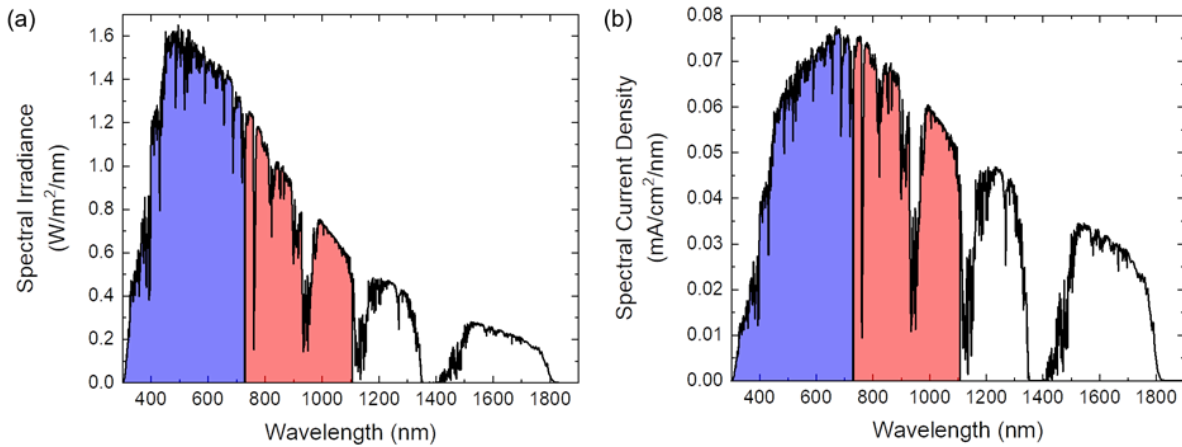
Fig. 1.2: Spectrum splitting for a dual-junction (2J) solar with a E_G combination of ~1.7 eV (blue region absorbed) and ~1.1 eV (red region absorbed). (a) Spectral irradiance and (b) spectral current density for the AM1.5G terrestrial spectrum. The standard reference spectra for AM1.5G is from ASTM G-173-03.

Due to their high efficiency and high specific power (power per weight), III-V MJ technologies have been the predominant solar cell choice for space applications. However, high substrate costs for III-V growth on GaAs or Ge wafers, around two orders of magnitude higher than for Si wafers, have prevented III-V technologies from utilization for terrestrial power generation. Cost requirements for space solar cell modules are less prohibitive since the total cost more strongly depends on launch costs. Launch costs scale with payload weight due to the fuel consumption used to move the payload into orbit, so high specific power is typically more important than low cost. High efficiency is also helpful to reduce the solar cell area required such that a smaller payload volume can be achieved. Besides lowering launch costs, the lifetime of the solar cell technology in the damaging space environment (described in Chapter 8.1) is also critical so that solar cells continue providing sufficient power to electronics throughout the mission duration. Recent advances in launch capabilities with reusable rockets have reduced launch costs and contributed to increased demand for space solar cells. Given the increased accessibility, the high cost of III-V technologies may become a barrier to scaling of production for mega-constellations of satellites or to the pursuit of a greater variety of space missions.

For both terrestrial and space applications there is a need for solar cell technologies with a combination of high efficiency and low cost to aid further technology penetration. With the remainder of this chapter, I discuss a potential solution to achieve this long sought pairing of traits by integrating both III-V and Si technologies into epitaxial III-V/Si MJ solar cells. I describe the advantages for direct growth of III-V sub-cells on a Si bottom cell/substrate as well as the challenges that have thus far prevented the success of this "holy grail" technology. Following, I detail prior development of $GaAs_yP_{1-y}$/Si dual-junction (2J) solar cells and my contributions in this work to the advancement of this technology.

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1.1 Epitaxial III-V/Si Multi-Junction (MJ) Solar Cells

III-V MJ solar cells offer high efficiency but are hindered by their reliance on small-diameter, high-cost substrates. In contrast, large-diameter, low-cost Si substrates are ubiquitous, but difficulties with integration of additional junctions have prevented the widespread use of Si substrates for MJ solar cells. Combination of a ~1.7 eV top cell with a ~1.1 eV Si bottom cell is near the ideal E_G pairing for a 2J solar cell (Fig. 1.3) [10]. This ~1.7 eV/~1.1 eV pairing has a theoretical max efficiency of 37% – 44% (34% – 40%) for 1-sun AM1.5G (AM0) illumination; the efficiency range is due to differences in modeling assumptions [10], [11]. Adding another sub-cell for a 3J with ~2.0 eV/~1.5 eV/~1.1 eV bandgaps could enable theoretical efficiencies up to 46% (44%) for 1-sun AM1.5G (AM0) illumination [11].

Recently, efficiencies for Si-based 2J (GaAs//Si) and 3J ($Ga_{0.51}In_{0.49}P$/GaAs//Si or $Ga_{0.51}In_{0.49}P$/$Ga_{0.93}In_{0.07}As_{0.87}P_{0.13}$//Si) solar cells up to 32.8% and 35.9% under 1-sun AM1.5G illumination have been achieved when combining III-V and Si sub-cells [12], [13]. Although impressive, these high-efficiency demonstrations utilized either mechanical stacking or wafer bonding, necessitating both a Si substrate and a III-V substrate. Such bonded or stacked cells are
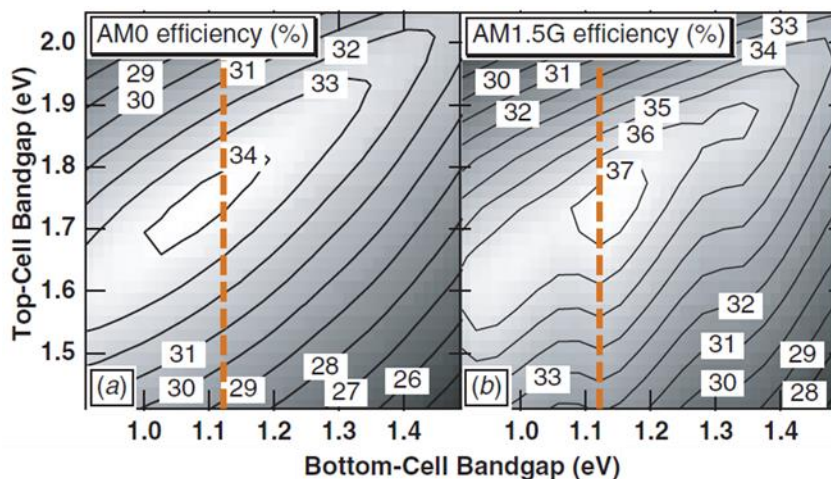
Fig. 1.3: Iso-efficiency contour plots for a two-terminal 2J solar cell as a function of top/bottom cell E_G for the (a) AM0 space and (b) AM1.5G terrestrial standard spectra. The dashed line in each marks the conditions with Si selected as the bottom cell. Adapted from Ref. [10].

commonly denoted in the research community as III-V//Si MJ solar cells – note the double-slash to indicate the III-V layers are not grown on Si but attached. While III-V//Si techniques allow the combination of high-quality sub-cells to reach high MJ efficiency, the high cost of a III-V substrate is not removed.

Mechanical stacking effectively "glues" the III-V solar cell stack on top of the Si solar cell. Most commonly, separate III-V and Si devices are fabricated prior to stacking such that the III-V//Si device is operated with four-terminals, with separate positive/negative contact for both the III-V and Si devices. Four-terminal operation removes the current matching requirement between III-V and Si sub-cells allowing non-optimal E_G combinations (for example 1.42 eV/1.12 eV for GaAs//Si) to reach closer to the efficiency of the optimal combination. In addition, mechanical stacking enables the free choice of Si architecture including front-side texturing, a luxury unavailable to wafer bonding and epitaxial approaches. However, fabrication and cell interconnection are complicated by the doubling of device contacts.

Direct wafer bonding presses two wafers with polished and activated surfaces together resulting in permanent covalent bonding between the two surfaces. Wafer bonding results in a single monolithic III-V//Si wafer that can be fabricated into two-terminal MJ solar cell devices as long as the wafer bond is electrically conductive. Resulting two-terminal devices from either wafer bonding or epitaxial approaches are simpler to integrate as modules than four-terminal devices from mechanical stacking. Major challenges for wafer bonding include required surface polishing for smooth surfaces and high bonding surface cleanliness as contaminants can cause voids or delamination.

Epitaxial integration can reduce cost and integration complexity by only using a single large-area Si wafer as both an active bottom cell and as a substrate for III-V growth. Epitaxial III-

V/Si MJ solar cells are monolithic and result in two-terminal devices, like wafer-bonded III-V//Si. Epitaxial III-V/Si devices do not utilize a III-V substrate and require fewer processing steps than either wafer bonding or mechanical stacking approaches. Although epitaxial III-V/Si MJ solar cells have great potential, device results significantly underperformed in comparison to III-V//Si solar cells with AM1.5G efficiencies in 2017 up to only 16.6% [14] and 19.7% [15] for GaAsP/Si 2J and GaInP/GaAs/Si 3J solar cells, respectively. Growth of high-quality III-V materials on Si substrates is challenging due to mismatched crystal lattice properties (see next Chapter 1.2) and causes more defective and therefore lower performance III-V sub-cells than in III-V//Si approaches. Epitaxial growth on Si degrades the Si lifetime from high temperature exposure [16]–[18] and also constrains the Si sub-cell architecture to an even greater extent than wafer bonding due to limited front-side passivation of Si by the defect-ridden interface between the III-V nucleation layer and Si [19] – wafer bonding can utilize a tunnel oxide (SiO_x) and poly-Si for the front-side of Si [20]. Additionally, epitaxial III-V/Si layer structures typically require III-V defect-reduction layers that are thicker than the thickness of III-V sub-cell(s), adding cost from extended growth time. Even so, recent work by my collaborators, by me, and by other research groups has enabled efficiency improvement in 2022 up to 23.4% – 25.0% for GaAsP/Si 2J [14], [21] and 25.9% for GaInP/GaAs/Si 3J [22].

1.2   Challenges of Epitaxial III-V on Si

Epitaxial growth of III-V semiconductors on Si substrates is challenging due to multiple differences in the crystal structure properties including crystal symmetry, lattice constant, and thermal expansion coefficient. These mismatches cause extended defects in the III-V epitaxy that often propagate in the growth direction and penetrate the active III-V absorber material(s). Due to missing or incorrect bonds (for example III-III bonds), extended defects typically form a

line/plane/surface of localized mid-gap defect levels that can recombine photo-excited charge carriers to hamper III-V solar cell device performance. Optimizing the layer design and growth process for reduction of extended defect densities is critical to achieving high-efficiency III-V sub-cells on Si.

Diamond cubic Si and zincblende III-V semiconductors both consist of atoms at the same crystallographic positions (face-centered cubic (FCC) lattice with two atom basis with site A at (0,0,0) and site B at (¼,¼,¼)). While diamond cubic Si has a Si atom at both basis sites, zincblende III-V semiconductors have group III atoms at site A and group V atoms at site B such that there are separate group III and group V FCC sub-lattices. The resulting zincblende III-V crystal structure has group III atoms tetrahedrally-bonded with four nearest-neighbor group V atoms, and vice versa. Due to the difference in basis, the zincblende structure has reduced crystal symmetry in comparison to the diamond cubic structure.

When nucleating III-V growth on Si substrates, two crystal domains of III-V – one with group III at site A and one with group V at site A – can form creating anti-phase domains (APDs). The boundary between adjacent APDs is called an anti-phase boundary (APB) and is a plane/surface of III-III and/or V-V bonds that will strongly recombine photo-generated carriers and reduce III-V sub-cell performance if APBs propagate through the III-V epilayers. Additional nucleation-related defects include stacking faults (SFs) and microtwins (MTs) from the coalescence of islands. Suppression of these nucleation-related defects is critical to enabling III-V sub-cells with anything above poor performance. Extensive research has focused on addressing the challenge of III-V nucleation on Si, primarily for GaP on Si (see Chapter 4.1 for detailed references). In short, careful optimization of substrate preparation and the growth process enabled nucleation of Ga near-selectively on site A such that nucleation-related defects are either self-

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terminated within a thin GaP layer or eliminated [23]–[27]. Commercial templates of thin, high-quality GaP on Si free of propagating nucleation-related defects were used in this work [24], [28], so APBs, SFs, and MTs were not a focus of my dissertation research.

Instead, I focused my research efforts on investigating the challenge of lattice mismatch between III-V semiconductors and Si. Conventional zincblende III-V semiconductors (AlGaInPAsSb compounds) all have larger lattice constants than Si (see Fig. 1.4).[1] Lattice mismatch, or lattice constant (a) difference, for an epilayer film on a substrate is described by the misfit strain ($f = (a_{Substrate} - a_{Film})/a_{Film}$) which is the sum of elastic strain (ε) and plastic strain (δ); $f < 0$ is for a compressive film and $f > 0$ is for a tensile film [30]. Films with thickness (h) less than the critical thickness (h_c) have misfit accommodated by only elastic strain ($f = \varepsilon$, fully-strained called pseudomorphic) resulting in tetragonal distortion of the film lattice constants. For thicker films (h $> h_c$) misfit dislocations are introduced to relieve elastic strain energy through plastic strain and
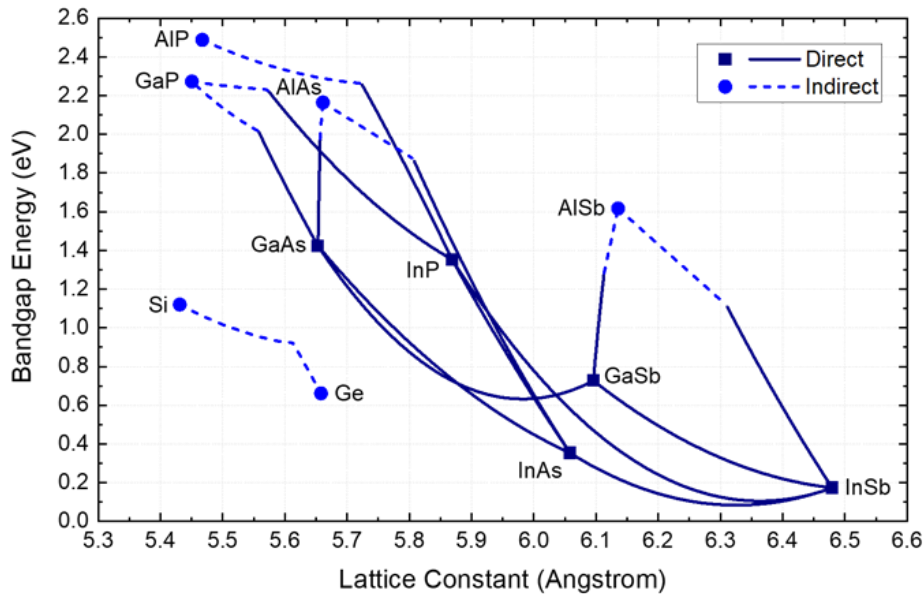
Fig. 1.4: Minimum bandgap energy vs lattice constant plot for conventional zincblende III-V binary and ternary semiconductors. Also includes group IV Si and Ge.

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[1] Dilute nitride III-N-V alloys can lattice match to Si. However, III-N-V materials typically have poor minority carrier properties and thus poor device performance [10]. Similarly, dilute boride B-III-V alloys can lattice match to Si but are not well studied [29].

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relax the film lattice constants back toward the unstrained lattice constant. GaP with the smallest lattice mismatch to Si, misfit of -0.36% at room temperature (RT), has an experimental h_c of ~90 nm [31], [32]. Increasing the lattice constant further for direct-E_G III-V of interest such as GaAs$_{0.77}$P$_{0.23}$ (~1.7 eV), GaAs, and Ga$_{0.51}$In$_{0.49}$P results in misfit of -3.1% – -3.9% necessitating dense networks of misfit dislocations to relax the thick absorber layer(s).

Dislocations are linear crystalline defects marking the boundary between slipped and un-slipped regions of the crystal film. Due to geometric considerations dislocations need to form a loop enclosing the slipped crystal, either having dislocation segments form a closed loop within the crystal or having two dislocation segment endpoints at the crystal surface (closing the loop by a virtual segment). Dislocations commonly form half-loops with a strain-relieving misfit dislocation (MD) segment at the mismatched interface and threading dislocation (TD) segments extending roughly vertically to exit the film at the growth surface. Dislocations with sufficiently-long MD segments may exit the film via the wafer edge such that the TD segment is not required, but this is typically a very small percent of dislocation loops due to the massively different length scales for film thickness vs. wafer dimensions.

The predominant type of dislocation in III-V growth on Si (001) substrates are so-called 60° dislocations [30]. 60° dislocations lie on {111} slip planes with the strain-relieving MD segment at the mismatched interface with either [110] or [1$\bar{1}$0] line direction and a TD segment for each end of the MD segment extending to the surface on the associated {111} slip plane. Following nucleation of dislocation half loops, glide of TD segments lengthens MD segments for added strain relief proportional to the total MD length. A set misfit strain can be accommodated by either a large density of dislocations with short MD segments or a small density with long MD segments. Since almost all dislocation loops have two TD segments, the threading dislocation

density (TDD) exiting the growth surface of a relaxed film depends proportionally on misfit strain relief and inversely on average MD length.

Growth of lattice-mismatched III-V materials typically uses metamorphic buffer layers to relieve misfit strain such that device layers can be grown lattice-matched on the resulting virtual substrate having the desired relaxed lattice constant. Metamorphic buffer layers concentrate MD segments within layers utilized at most for electrical conduction. Instead only TD segments hamper solar cell performance by introducing lines of defects extending through the absorber thickness. Minimizing the TDD is critical to limit degradation of minority carrier properties. Longer MD segments provide more strain relief than shorter MD segments, necessitating fewer dislocation loops and therefore lower TDD. Therefore, growth conditions should maximize the glide of dislocations while minimizing nucleation of new loops.

Compositionally-graded buffer (CGB) layers are employed to control the nucleation and glide of misfit dislocations with a small fraction of the target misfit strain introduced in each successive layer [33]. Growing a layer directly with larger misfit causes uncontrolled dislocation nucleation limiting the ability for misfit relief by extending MD length. Also, direct growth concentrates the network of MD segments on a single mismatched interface increasing dislocation interactions that may impede dislocation glide. Instead, growing layers with small misfit can enable reduced dislocation nucleation rates such that strain relief proceeds by glide of a lower number of dislocations. In addition, CGB layers separate MD segments between the multiple low-misfit interfaces, helping to reduce dislocation pinning. CGB growth conditions also influence the obtained TDD. When TDD is glide-limited, the TDD is expected to be proportional to growth rate (thickness per time) and strain grading rate (misfit per thickness), and exponentially decreases with growth temperature (T_{growth}) due to the Arrhenius dependence of dislocation glide velocity [33].

However, dislocation nucleation rates also depend on T_{growth} by Arrhenius relations, so increased T_{growth} may result in increased TDD [34].

While thicker buffer layers (lower strain grading rate) can enable reduced TDD, thermal expansion coefficient mismatch limits the total III-V thickness that can be grown on Si without cracking. Due to larger thermal expansion coefficients for III-V than Si, III-V layers on Si are more lattice-mismatched at T_{growth}; GaP on Si for example has misfit of -0.36% at RT that increases to -0.47% at 600 °C. When cooling down from T_{growth} the III-V lattice shrinks faster than that of Si and changes the III-V material from relaxed to tensile strained. Quick cooling rates reduce the time for as-grown dislocations to adjust to the change in strain before dislocation motion freezes out at lower temperature. Cooling down may build too much tensile strain energy and crack the III-V film to relieve strain. Mechanical handing at RT following these growths increases the probability of crack formation as heterogeneous forces applied to the sample may stimulate strain relief through cracking. Limiting total III-V thickness on Si can eliminate cracking by lessening the stored tensile strain energy. T_{growth} and material choice influence the achievable thickness without cracking. My colleagues in the Lee group and I typically avoid cracking when growing 5 – 6 μm of III-V (~1.7 eV GaAsP or GaAs) on Si.

1.3   Prior Development of GaAsP/Si Dual-Junction (2J) Solar Cells

$GaAs_yP_{1-y}$ is the top cell choice for epitaxial III-V/Si 2J solar cells as $GaAs_{0.77}P_{0.23}$ has the smallest lattice mismatch to Si of conventional III-V alloys with ~1.7 eV bandgap (Fig. 1.4). $GaAs_yP_{1-y}$ offers a tunable direct E_G from 1.42 eV – 2.01 eV along with multiple options for higher E_G barrier materials at the same lattice constant (AlGaAsP and AlGaInP alloys). GaP, with the smallest lattice mismatch to Si, serves as a convenient starting point for III-V growth on Si, first

addressing the challenge of polar III-V nucleation on non-polar Si before further expanding the lattice constant.

However, even with nucleation-related defects controlled and moderate -0.36% misfit strain, growing thicker GaP layers to relax strain can cause high TDD $> 10^7$ cm^{-2} [25], [35]–[37]. This high starting TDD is unacceptable since high TDD is generally expected to persist in subsequent III-V growth, where larger misfit strains need to be relaxed. High TDD in device layers hampers performance, necessitating TDD reduction to $1 - 2 \times 10^6$ cm^{-2} to reach III-V/Si 2J solar cell efficiencies exceeding 30% [38]–[41]. Previous work in the Lee group by Nay Yaung *et al.* investigated the TDD of relaxed *p*-type GaP on GaP/Si templates as a function of growth temperature [34]. Nay Yaung observed TDD decreased exponentially with increased T_{growth} (< 500 °C), in agreement with the expected dislocation dynamics model when dislocation glide limits the achievable TDD [30]. While further TDD reduction was expected at higher T_{growth}, Nay Yaung found an exponential increase in TDD with increased T_{growth} (> 550 °C) indicating strong dislocation introduction limits TDD in this T_{growth} regime. Optimized T_{growth} enabled relaxed *p*-GaP TDD on Si as low as 1.7×10^6 cm^{-2} [34]. However, *n*-type GaP on Si is needed for epitaxial III-V/Si MJ solar cells and, while not known at the time, obtaining low TDD for relaxed *n*-GaP on Si is more challenging.

For epitaxial III-V/Si MJ solar cells, GaAs$_y$P$_{1-y}$ is the primary grading pathway with buffer layers stepping y_{As} to the final ~1.7 eV GaAsP composition [14], [22], [34]. Since GaAs$_y$P$_{1-y}$ E$_G$ decreases monotonically as y_{As} increases, compositionally-graded buffers using GaAs$_y$P$_{1-y}$ have E$_G > 1.7$ eV and allow photons not absorbed by the ~1.7 eV GaAsP top cell to pass through to the Si sub-cell. (Al)GaInP with graded x_{In} is another CGB option, but high surface roughness and phase separation defects impede glide in (Al)GaInP CGBs resulting in higher TDD when

compared against GaAs$_y$P$_{1-y}$ CGBs [42]. Si$_x$Ge$_{1-x}$ CGBs on Si have enabled ~1.7 eV GaAsP with lower TDD than on GaAs$_y$P$_{1-y}$ CGBs [43]. However, Si$_{1-x}$Ge$_x$ CGBs absorb photons for Si due to lower E$_G$ for Si$_{1-x}$Ge$_x$ than for Si. As a result, the highest x$_{Ge}$ composition Si$_{1-x}$Ge$_x$ needs to be utilized as the bottom cell instead of the Si substrate. Si$_{1-x}$Ge$_x$ solar cells are not well-developed lacking backside passivation technologies like that of Si and require thick epitaxial layers due to the indirect E$_G$.

GaAsP/Si 2J solar cells rely on the wider-E$_G$ GaAsP top cell to provide most of the power; a ~20%-efficient GaAsP top cell combined with a ~10%-efficient Si bottom cell (with GaAsP-filtered spectrum) is expected to be needed to attain a 30%-efficient 2J cell under AM1.5G. Due to the expectation that TDD reduction to $1 - 2 \times 10^6$ cm^{-2} is needed to reach this performance, TDD has consistently been a primary concern. High TDD causes short minority carrier diffusion length resulting in poor carrier collection (reduced current) and high dark current (reduced voltage) [39].

Research on GaAs$_y$P$_{1-y}$ CGB growth and design took ~1.7 eV GaAsP TDD on Si from > 10^8 cm^{-2} to < 10^7 cm^{-2}. Similar to as done for GaP buffers, Nay Yaung and Vaisman optimized T$_{growth}$ for the Lee group's *p*-type GaAs$_y$P$_{1-y}$ CGB demonstrating TDD for ~1.7 eV GaAsP as low as 4.0×10^6 cm^{-2} on GaP/Si and 1.4×10^6 cm^{-2} on GaP [34], [44]. These results indicated that the TDD of relaxed *p*-GaP on Si (1.7×10^6 cm^{-2}) contributed significantly to the TDD of GaAsP on Si, as TDD reduction to $1 - 2 \times 10^6$ cm^{-2} was already feasible on GaP substrates. The large TDD contribution from GaP is concerning as the misfit for GaP on Si is a fraction of that for ~1.7 eV GaAsP. Additionally, it should be noted that obtaining low-TDD *n*-type buffer layers, as needed for GaAsP/Si 2J solar cells, was not yet known to be even more challenging.
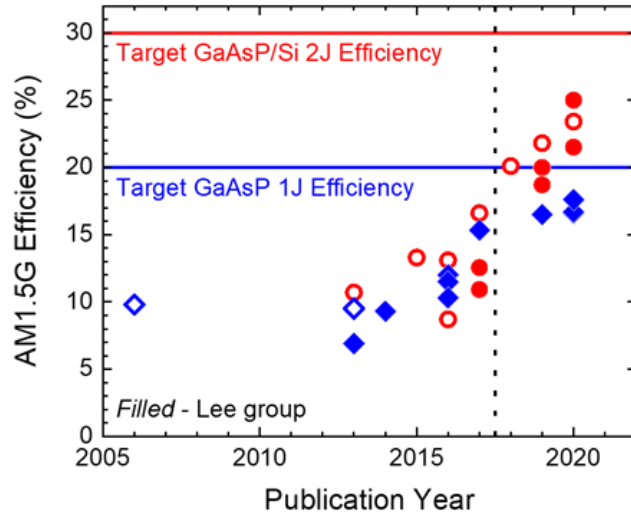
Fig. 1.5: AM1.5G efficiency of ~1.7 eV GaAsP 1J (blue) and GaAsP/Si 2J (red) solar cells with GaAs$_y$P$_{1-y}$/GaP buffers on Si [14], [21], [34], [45]–[56]. Filled points show data from the Lee group. Horizontal lines show target GaAsP 1J and GaAsP/Si 2J efficiencies. Data left of the dotted line was performed before I joined the Lee group.

Many factors such as defect densities, junction design, light management, and contact/barrier layer choices interact in a complex manner to affect GaAsP top cell performance. While TDD does limit device performance, much of the efficiency improvement during development of ~1.7 eV GaAsP 1J and GaAsP/Si 2J solar cells relates to device design improvements (Fig. 1.5) [14], [21], [34], [45]–[56]. Before I joined the Lee group, the group's GaAsP 1J design had grown in complexity from a barrier-less homojunction with 6.9% AM1.5G efficiency [57] to including InAlP window layer, InGaP back surface field (BSF), and anti-reflection coating with 15.3% efficiency [50]. Design changes during this period beside CGB changes to reduce TDD [34], [48] included adding InGaP window and back surface field (BSF) barrier layers [47], [48], improving the *n*-contact layer doping [48], switching to an InAlP window layer [34], and adding an anti-reflection coating (ARC) [50]. At this time the Lee group (University of Illinois, UIUC) had not yet developed GaAsP/Si 2J devices, while the Grassman group (Ohio State University, OSU) advanced their GaAsP/Si 2J efficiency without ARC from 13.3% up to 16.6% with changes to both sub-cell designs [54].

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Early during my time in the Lee group, Fan led the development of GaAsP/Si 2J devices in the Lee group. Following the installation of CBr_4 and GaTe sources for high C and Te doping stable to thermal annealing, Fan *et al.* designed an (Al)GaAsP-based tunnel junction design [52]. In addition, Fan developed 2J device processing for the Lee group including isolated front-side/back-side III-V/Si etching capabilities and an improved in-house ARC demonstrating GaAsP/Si 2J solar cell AM1.5G efficiency up to 20.0% [52]. During a similar timeframe, Grassman *et al.* utilized improved processing capabilities and added an ARC to increase GaAsP/Si 2J efficiency from 20.1% to 21.8% [51], [54]. Additionally, Fan improved current collection for both GaAsP and Si sub-cells with higher T_{growth} for GaAsP active region (GaAsP 1J to 16.5% efficiency) and random pyramid texturing for the backside of Si [52], [53]. However, Fan and I noticed early indications Nay Yaung's thick *p*-type CGB design with GaAsP TDD on Si as low as $4.0 \times 10^6 \, cm^{-2}$ needed modification for both the higher T_{growth} of the GaAsP sub-cell and the switch to *n*-type buffer layers required for the GaAsP/Si 2J design.

Although epitaxial III-V/Si MJ solar cells have primarily targeted terrestrial applications, the potential combination of low cost and high efficiency could enable cost-constrained space missions and meet increased demand for PV in space. However, GaAsP is nearly untested for environmental conditions in space, such as bombardment from electron/proton irradiation and thermal challenges from high/low temperatures and temperature swings/cycling. Common III-V solar materials are already well-studied under particle irradiation showing good radiation hardness [58]; more radiation-hard solar cells suffer less degradation under a given fluence of particle irradiation. In fact, dislocated GaAs 1J solar cells on Si are more radiation-hard than equivalent cells on GaAs [59]–[62], potentially out-performing efficiencies on GaAs at high particle fluence [59], [60]. Prior to my work, promising but limited space testing studies were performed on GaAsP

solar cells including proton irradiation [63], initial electron irradiation tests on GaAsP 1J cells in the Lee group by Vaisman [44], and thermal tests including temperature-dependent lighted current-voltage curves and thermal cycling of GaAsP/Si 2J cells [64].

1.4   Dissertation Contents

1.4.1 Research Objectives

While metamorphic GaAsP/Si 2J solar cells offer great promise, many challenges remain to enable high efficiency. In this dissertation, I focus on investigation and reduction of defects for relaxed GaP and ~1.7 eV GaAsP on Si to improve material quality and advance GaAsP/Si 2J solar cell development. Initially, I set out to work on decreasing TDD from our previously achieved 1.7 $\times 10^6$ cm^{-2} and 4.0×10^6 cm^{-2} for *p*-type GaP and GaAsP on GaP/Si, respectively, to improve GaAsP 1J performance. With the introduction of GaAsP/Si 2J devices in the Lee group, new challenges arising from the GaAsP/Si 2J architecture became apparent. As a result, I aimed to understand and mitigate these new challenges, in particular the higher TDD from *n*-type buffers, to improve GaAsP/Si 2J performance. Additionally, I set out to provide detailed space testing studies for metamorphic GaAsP on Si broadening the current literature.

1.4.2 Research Contributions

In the course of this dissertation research, I made the following original research contributions:

- Enhanced capabilities of defect selective etching (DSE) for GaP to investigate larger TDD ranges and TDD inhomogeneity by etch pit size control and surveys with multiple microscopy tools.

- Investigated morphological defects for relaxed *p*-type GaP on GaP/Si templates and studied a two-step growth strategy to reduce TDD.

- Studied effects of doping for relaxed GaP on GaP/Si, revealed TDD escalation and inhomogeneity with *n*-type doping, and determined strategies to reduce *n*-GaP TDD.

- Showed TDD of ~1.7 eV GaAsP 1J solar cells on Si was higher using *n*-doped $GaAs_yP_{1-y}$/GaP buffers than using unintentionally-doped (UID) or *p*-type buffers and later demonstrated similar TDD between UID buffers and improved *n*-doped buffers.

- Advanced capabilities of electron beam-induced current (EBIC) imaging to investigate electrically-active defects dependent on depth within a solar cell by varied accelerating voltage choice.

- Identified dark line defects (DLDs) in EBIC affecting GaAsP top cells at either the front or back surface of the active region and showed an AlGaAsP BSF design reduced DLDs at the back surface.

- Aided design, growth, and characterization of GaAsP 1J and GaAsP/Si 2J solar cells with improved carrier collection and efficiency.

- Studied radiation hardness of ~1.7 eV GaAsP 1J solar cell device designs demonstrating superior radiation hardness for n^+/p front junction design.

- Developed temperature-dependent solar cell device characterization capabilities and measured temperature-dependent external quantum efficiency (EQE) and lighted/dark current-voltage (LIV/DIV) for GaAsP 1J.

With this dissertation work (**bold**), I contributed the following advances to the state of the art:

- I decreased the lowest TDD for relaxed *p*-type GaP on Si from 1.7×10^6 cm^{-2} [34] to **$1.0 - 1.1 \times 10^6$ cm^{-2}** [36].

- I decreased the lowest TDD for relaxed *n*-type GaP on Si from $3 - 4 \times 10^7$ cm^{-2} [37], [65] to **1.54 ($\pm$0.20) $\times$ 10^6 cm^{-2}** [65]. TDD for relaxed *n*-type GaP on Si was decreased by Boyer *et al.* to 2.4 ($\pm$0.4) $\times 10^6$ cm^{-2} [37] during my dissertation timeline.

- I aided improvement of record 1-sun AM1.5G efficiencies for ~1.7 eV GaAsP 1J solar cells on Si from 15.3% [50] to **17.6%** [21].

- I aided improvement of record 1-sun AM1.5G efficiencies for epitaxial GaAsP/Si 2J solar cells from 16.6% [54] to **25.0%** [21]. During my dissertation timeline, the record also was set by the Grassman group at 20.1% [51], 21.8% [54], and 23.4% [14].

1.4.3 Dissertation Organization

Chapter 1 describes the motivation and challenges for epitaxial III-V/Si MJ solar cell technologies, prior development of GaP and ~1.7 eV GaAsP on Si, and briefly on the dissertation contents. Chapter 2 details material growth by molecular beam epitaxy including specifics on mixed arsenide-phosphide growth. In addition, Chapter 2 details techniques used for material characterization and solar cell characterization. Chapter 3 discusses extended defect characterization techniques primarily for TDD estimation. I also include additional experiments investigating the application of each technique. Chapters 4 through 8 describe experimental results for this dissertation, and I begin each results chapter by providing additional background information relevant to the presented work.

Chapter 4, 5, and 6 discuss results from investigation of relaxed GaP on Si. Chapter 4 investigates morphological defects and TDD reduction for *p*-type GaP on Si with a two-step growth design. Chapter 5 studies the effects of doping for relaxed GaP on Si, showing unexpected TDD escalation for *n*-doped GaP while UID and *p*-doped GaP did not change. Additional material

quality challenges for *n*-type GaP on Si are also discussed. Chapter 6 directly follows the studies from Chapter 5 and implements strategies to reduce TDD for relaxed *n*-type GaP on Si.

Chapters 7 and 8, as well as the last section of Chapter 6, discuss results from investigations of ~1.7 eV GaAsP solar cells. The last section of Chapter 6 compares the TDD and device performance of GaAsP 1J solar cells on Si grown on either UID buffers or *n*-doped buffers using improvements from the prior sections in Chapter 6. Chapter 7 first details previous Lee group development of GaAsP 1J and GaAsP/Si 2J solar cells before investigating improved designs and the resulting effects on defects and on device performance. Chapter 8 changes discussion to solar cell characterization for the space environment. I detail experiments on ~1.7 eV GaAsP 1J solar cells testing either the radiation hardness or temperature-dependent device performance.

This dissertation concludes with Chapter 9 summarizing the results and discussing areas for potential future work.

CHAPTER 2

MATERIAL GROWTH AND CHARACTERIZATION

This chapter reviews the material growth, material characterization, and solar cell characterization techniques utilized throughout this dissertation. The experimental work in this dissertation relied on a feedback loop of growth and characterization to understand and to develop high-quality processes and components for GaAsP/Si double-junction (2J) solar cells. First, I detail molecular beam epitaxy (MBE) growth, describe the Lee group MBE system, and provide additional explanation for mixed arsenide-phosphide growth using valved crackers in solid source MBE. Following, I explain material characterization techniques used in this work to assist growth calibration and to investigate material quality. Lastly, I discuss solar cell characterization techniques used in this work to evaluate the device performance resulting from design changes to the growth and device structure. Extended defect characterization techniques, as described in Chapter 3, were also utilized as important feedback for growth design.

2.1 Molecular Beam Epitaxy (MBE) Growth

2.1.1 MBE Basics

Molecular beam epitaxy is a carefully controlled physical vapor deposition process using evaporation or sublimation to grow epitaxial films on a substrate. The precise control of atomic layer thicknesses, composition, and intentional doping as well as the ability to achieve low unintentional impurity concentrations make MBE an excellent tool for III-V compound semiconductor growth [66]. Ultra-high vacuum (UHV) environment, having base pressure typically on the order of 10^{-10} Torr or less, is a critical enabler to both of these capabilities. The low pressure of the UHV environment causes gas atoms or molecules to have mean free paths ($\lambda \propto P^{-1}$) much longer than the chamber dimensions such that an atom/molecule would collide with the chamber walls many times before colliding with another atom/molecule [67]. The long mean free path translates into beams of atoms or molecules travelling ballistically from elemental sources to the substrate target. Sources are commonly heated to elevated temperatures to vaporize atoms/molecules in the cell pocket, and once a mechanical shutter or needle valve is opened, an atomic or molecular beam emanates from the opening to cover the substrate somewhat akin to spray painting. Choice of the sequencing of source temperatures and shutter/valve positions can be utilized to precisely control layer properties.

Both the UHV environment and high-purity sources (typically higher than 99.9999% (6N)) ensure the growth environment is nearly free of contaminants. Rigorous care needs to be taken to maintain the UHV environment and avoid contamination of the growth chamber and source materials. This is often achieved with a combination of stainless steel chambers with low-leak ConFlat (CF) flange connections, vacuum pumps (such as turbomolecular pumps, cryogenic pumps/shrouds, and ion pumps), load-lock chamber separated by gate valve, and thorough

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cleanliness procedures during chamber maintenance, material sourcing, and substrate loading/unloading. Fast pumping is needed to remove residual atoms/molecules not incorporating into growth on the substrate and is commonly realized with liquid nitrogen (LN2) cooling of the inner chamber walls (cryo shroud). Gas species colliding with the cryo shroud lose kinetic energy and become trapped on the cryo shroud wall and buried by later arriving species. Cryo pumps operate similarly but use compressed He to reach much lower temperatures down to ~10 K. Ion pumps also are gas entrapment pumps but instead ionize gas species and use the ions to sputter a chemically-active material that getters gas species inside the pump. Turbo pumps work instead by imparting momentum to gas species by collisions with rotating blades to direct species to the pump exhaust.

With a growth temperature range primarily from 400 °C to 700 °C, surface kinetics control the epitaxy of III-V semiconductors in MBE. MBE growth occurs by incident atoms/molecules adsorbing on the growth surface, dissociating from molecules (such as As_2 or P_4) into atoms, migrating on the surface by hopping between adjacent atomic sites, and nucleating islands of adjacent atoms or extending a layer step edge. In addition, atoms/molecules can escape back into the gas state when having sufficient kinetic energy to desorb from the surface. Desorption rates vary depending on the species as well as following an Arrhenius dependence on temperature. Sticking coefficients refer to the probability for a species to stay adsorbed and ultimately become part of the film [67].[2] In MBE, group III elements (Al, Ga, In) are reasonably assumed to have unity sticking coefficient; unity sticking coefficient for In only applies for growth temperatures roughly < 500 °C, as higher temperatures lead to problematic In desorption [68]. On the other

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[2] The sticking coefficient may not always be equivalent to the incorporation coefficient since an impurity may form a surface layer that does not incorporate with as high concentration. During surface layer accumulation the sticking coefficient would be larger than the incorporation coefficient [67].

hand, sticking coefficients for group V elements (P, As, Sb) are much less than unity because of high vapor pressure. Due to the difference in group III and group V sticking coefficients, MBE growth is often performed with large V/III flux ratios to supply enough group V overpressure at the surface to maintain stoichiometry. In addition, the group III flux(es) conveniently limits/controls the growth rate and group III alloying. However, the non-unity sticking coefficients of group V species make control of group V alloying much more challenging as group V composition may depend on temperature, V/III ratio, growth rate, and group III composition (see Chapter 2.1.3).

Epitaxy occurs in one of five growth modes – Frank-van der Merwe, step-flow, Volmer-Weber, Stranski-Krastanov, or column – and depends on the combination of misfit strain, adhesion, and adatom mobility as influenced by the growth temperature and incident fluxes [69]. For high adatom mobility and high bonding strength with the substrate, a full monolayer is completed before a second layer starts forming, resulting in layer-by-layer growth, Frank-van der Merwe mode (Fig. 2.1(a)). High bonding strength leads to adatoms attaching to the side of 2D islands as opposed to climbing on top to become 3D islands. In addition, when surface steps are present and adatom mobility is sufficiently high, adatoms become more likely to encounter and
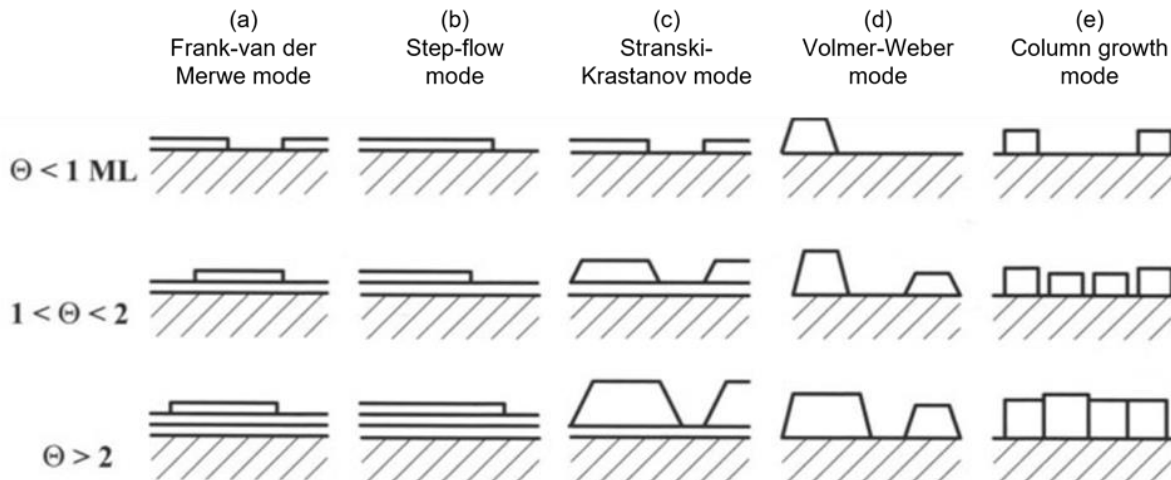
Fig. 2.1: Schematics of different growth modes in MBE for three cases of monolayer (ML) coverage (Θ) during growth Adapted from [69].

attach to step edges than other adatoms, resulting in step-flow mode (Fig. 2.1(b)) where growth proceeds by the advancement of surface steps. Increasing adatom mobility with higher temperature, lower V/III ratio, or lower growth rate can transition growth from Frank-van der Merwe mode to step-flow mode. For low adatom mobility and low bonding strength with the substrate (stronger bonding between surface atoms), clusters of surface atoms nucleate 3D islands that grow and coalesce into a film, called island growth or Volmer-Weber mode (Fig. 2.1(d)). With stronger bonding to the substrate, a 2D wetting layer can cover the substrate surface before 3D islands form, resulting in layer-plus-island growth called Stranski-Krastanov mode (Fig. 2.1(c)). Volmer-Weber and Stranski-Krastanov modes are often influenced by high misfit strain as 3D islands reduce strain energy in comparison to 2D growth. For extremely low adatom mobility and preferential growth direction, the 3D islands continue growth as whisker-like columns in column growth mode (Fig. 2.1(e)). If the columns coalesce into a film the boundaries between columns will be highly defective.

2.1.2 *Lee Group's Veeco Mod GEN-II MBE System*

The Lee group utilizes an Applied EPI (now Veeco) Mod GEN-II MBE system for epitaxy of III-AsP samples. This system is a horizontal-style MBE with the growth direction perpendicular to the floor (see Fig. 2.2 [70]). GEN-II MBE systems are designed for 3" wafers, however the Mod GEN-II system has a modified design to enable the use of up to 4" wafers with a 4" substrate heater and continual azimuthal rotation (CAR) assembly. Since the Mod GEN-II has a 4" CAR in a 3" growth chamber, flux uniformity decreases for the last ~1" outer ring. Nevertheless, the ability to perform growth with up to 4" wafers is beneficial for research purposes. The CAR assembly facilitates both substrate rotation to improve flux uniformity and flips the substrate between facing the source flange with effusion cells for growth (growth position) and the buffer chamber having
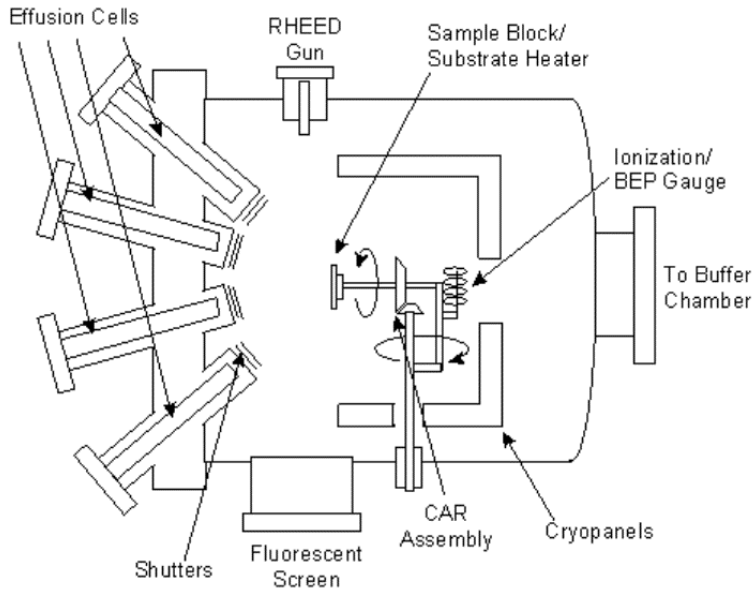
Fig. 2.2: Overhead-view schematic of a typical horizontal-style MBE growth chamber. Abbreviations used: reflection high energy electron diffraction (RHEED), continual azimuthal rotation (CAR), and beam equivalent pressure (BEP) gauge also referred to as beam flux monitor (BFM). From [70].

a transfer arm effector to load/remove substrates into/from the growth chamber (load position). A beam flux monitor (BFM) is attached to the opposite side of the CAR than the substrate heater. When in load position the BFM, which is a specially-designed ionization gauge for pressure measurement, faces the effusion cells and can be used to calibrate fluxes prior to growth.

In-situ monitoring of growth and the growth environment enables precise control of epitaxy. Reflection high energy electron diffraction (RHEED) can monitor in-situ atomic-scale surface morphology through a glancing incidence electron beam from a high voltage electron gun and a glancing exit diffracted beam projected onto a fluorescent phosphorous screen that can be captured on camera. The low incidence angle of the electron beam results in penetration depths of only a few atomic layers such that 3D island (2D layer) growth can be observed as a spotty (streaky) RHEED pattern with a pattern dependent on the surface reconstruction periodicity [71]. A resistive substrate heater (tantalum covered by pyrolytic BN (PBN)) heats the substrate primarily by radiative heat transfer. Substrate temperature is measured both by a thermocouple in close

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proximity to the backside of the substrate and a pyrometer at normal incidence to the frontside of the substrate. Growth pressure is monitored by an ionization gauge while additional specially-designed ionization gauges within the As and P cell pockets called "sniffers" allow in-situ monitoring of approximate As and P fluxes during growth. The sniffers enable a grower to adjust group V fluxes during growth to improve composition accuracy during mixed As-P growth (see Chapter 2.1.3). In addition, a residual gas analyzer (RGA) can monitor gas species present in the chamber. However, the RGA is primarily used during UHV maintenance including leak detection.

The Lee group MBE utilizes multiple pumps to maintain high pumping rates and low pressure. Pumps on the growth chamber include the LN2 filled cryo shroud, a cryo pump, and an ion pump. Since this is a phosphide MBE system, an additional pumping route is included to safely remove pyrophoric white phosphorous that builds up on the cryo shroud walls. Exposure of white phosphorous to oxygen around room temperature causes spontaneous combustion also forming toxic fumes; maintenance on a growth chamber with white P on the chamber walls would be very hazardous. Instead a phosphorous removal system is installed onto the growth chamber including a removable LN2 cooled cryo shroud called a "P trap" that is backed by a turbo pump backed by a scroll pump. The growth chamber cryo shroud is heated by LN2 removal and subsequent growth chamber baking to transfer white P to the P trap. Following white P transfer the following simplified procedure is followed: isolate P removal system from growth chamber by gate valve, remove LN2 lines from P trap while still keeping LN2 slowly boiling off within the P trap, vent P removal system, remove P trap from flange and submerge P trap in abatement solution ($NH_4OH:H_2O_2:H_2O$ solution) to convert white P into primarily neutralized phosphoric acid. Often the P trap is not installed in the P removal system such that its turbo pump can be used to aid pumping during maintenance periods.

Two additional chambers, the buffer and intro chambers, enable substrate transfer from the room to the UHV growth chamber while avoiding exposure of the growth chamber to atmospheric contaminants. The buffer chamber directly connects to the growth chamber by gate valve while the intro chamber directly connects to the buffer chamber by gate valve. An ion pump pumps the buffer chamber often keeping a baseline UHV environment, while a turbo pump backed by scroll (or diaphragm) pump pumps the intro chamber. During periods of growth, the intro chamber serves as a load-lock typically being vented to atmosphere, pumped down, and baked to 200 °C daily to load/remove substrates from the MBE system. As such, the intro door has an o-ring seal instead of a CF flange for easy everyday opening/closing leading to higher baseline pressures. The buffer chamber is placed between the growth and intro chambers to allow substrate transfer from the intro chamber to the cleaner buffer chamber and substrate baking (typically to 300 °C on a buffer baking station) before loading the substrate into the growth chamber for sample growth.

The source flange has eight cell positions arranged with two steep upward ports, two shallow upward ports, two shallow downward ports, and two steep downward ports. "Shallow" ports are around 12° with respect to the floor, while "steep" ports are around 30°. Two additional "deep" upward ports are on the growth chamber and are at much steeper angles, almost 80°. Group III dual-filament SUMO effusion cells have occupied the steep and shallow upward ports for the Lee group currently with Ga and In in the steep upward ports and Al and another In in the shallow upward ports. Early in the Lee group, the shallow upward port for the second In was previously used for a second Ga cell, before changing to Ge, and most recently converted to In. Effusion cells control the temperature of a source charge in a PBN crucible to produce a vapor pressure that is directed through the crucible opening at the substrate when the shutter is actuated open or is stopped when the shutter is closed. Dual-filament SUMO effusion cells allow either heating of tip

(nearer crucible opening), base (nearer crucible bottom), or both to adjust the temperature profile of the crucible and reduce challenges such as spitting. The Al SUMO cell also has a specially-designed cold lip structure to stop Al from creeping out of the crucible and damaging the heating filaments.

Valved cracker cells for As and P occupy the steep downward ports. The source charge of a valved cracker is held at a constant temperature during growth as the large vapor pressure of As and white P makes tuning temperature for flux values challenging. Instead a mechanically-actuated needle valve controls the flux by how far the valve opens. A cracker zone separates the source charge from the needle valve. The cracker zone serves as a high temperature (~700 °C – 900 °C) baffled path to crack As_4 or P_4 molecules to As_2 or P_2, modifying how group V elements interact with the growth surface. In addition, cracking P_4 (white P) to P_2 reduces the hazard of white P condensing on pumps. While the As valved cracker has two zones (source and cracker), the P valved cracker has three zones (red P source, white P source, and cracker). A red P source charge is loaded into the "red zone" to reduce hazard both during resourcing and subsequent chamber maintenance. Later the red zone is heated to elevated temperature with the valve closed to evaporate P from the red P and then condense this as white P in the cooled "white zone". For growth, the red zone is cooler again and P_4 vaporizes from the white zone. This process reduces the amount of white P that needs to be removed from the growth chamber prior to maintenance. The sniffer for each cell is positioned between the valve and the shutter for both steep downward ports.

The Lee group's primary *n*-type (Si) and *p*-type (Be) dopants occupy the shallow downward ports with single-filament dopant effusion cells. These cells utilize smaller crucibles and require the source charge to be fused to the PBN crucible such that the charge does not fall out

of the crucible when facing downward. In addition, the source charge should remain solid and sublimate so that the liquid does not drip out of the crucible. During dopant fusing the effusion cell heats the source charge above cell operating temperatures so the charge nears its melting point and diffuses with the PBN crucible enough such that it stays in place during normal operation.

The Lee group's secondary n-type (Te) and p-type (C) dopants occupy the deep upward ports and were added to the chamber following the group's move from Yale University to the University of Illinois Urbana-Champaign. A single-filament dopant effusion cell with attached shutter was loaded with GaTe captive source charge to be used for Te doping as group VI elemental sources have high vapor pressure. A CBr_4 gas-source injector is situated in the other deep upward port and is connected to the CBr_4 gas delivery system. This system regulates CBr_4 flow to the injector using a combination of valves, orifices, and a pressure controller in addition to a turbo pump backed by a scroll pump. The choice of orifice(s) and pressure controls the dopant flux delivered to the substrate surface. However, the Lee group has limited investigation of how these choices affect doping concentration since C doping is primarily used for p-type doping concentrations in excess of 1×10^{20} cm^{-3} for tunnel junction or contact layers.

2.1.3 Mixed Arsenide-Phosphide Growth

MBE growth of $Al_xGa_{1-x}As_yP_{1-y}$ for GaAsP/Si 2J solar cells in this work requires control of both mixed cation and mixed anion composition. Calibration of group III fluxes for mixed cation composition and growth rate is simple in comparison to calibration for mixed anion composition. As mentioned above, Group III species have unity sticking coefficients and limit growth rate such that separately-calibrated atomic flux densities for each group III species determine the growth rate and cation composition regardless of growth conditions (within reason). Group V sticking coefficients are non-unity and vary with growth temperature and potentially with group III fluxes

(growth rate and cation composition). As a result, changing growth temperature – even when keeping constant As and P fluxes and all other growth conditions the same – will change the resulting anion composition. As shown in Fig. 2.3(a), keeping constant As and P fluxes (constant BFM ratio) and increasing growth temperature results in lower y_{As}. While both sticking coefficients for As and P decrease with increasing growth temperature, these results indicate the change in As sticking coefficient is more significant, possibly since the P sticking coefficient is already lower than that of As.
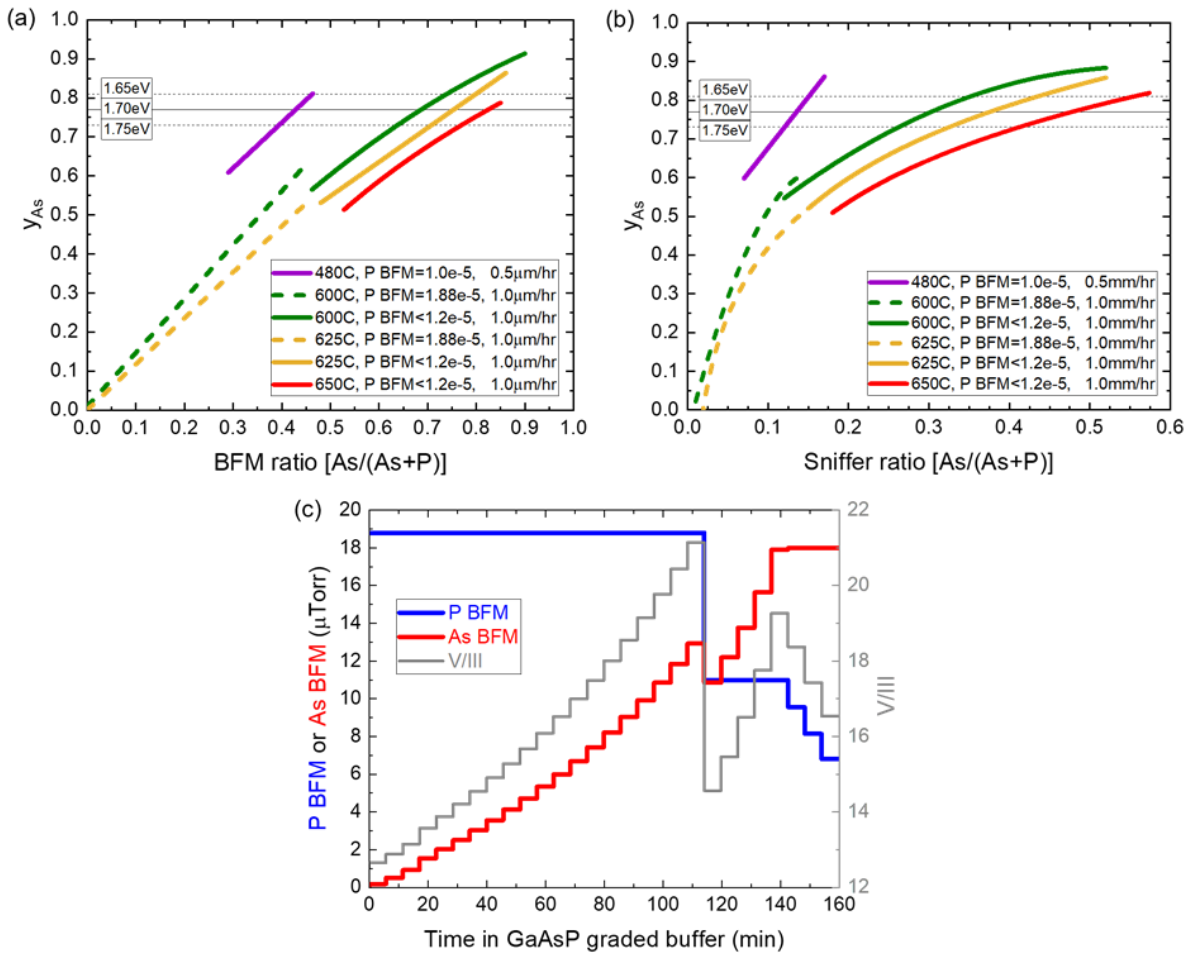
Fig. 2.3: Examples of GaAs$_y$P$_{1-y}$ calibration curves based on (a) BFM ratio and (b) sniffer ratio, primarily showing calibration curves for layers with different growth temperature or P BFM. Horizontal lines for the y_{As} of 1.75 eV, 1.70 eV, and 1.65 eV GaAsP are also shown for reference. (c) Example of BFM ratio control for GaAs$_y$P$_{1-y}$ 28-step step-graded buffer up to $y_{As} = 0.8$ at ~1.0 μm/hr. P BFM (blue, left axis) and As BFM (red, left axis) are shown using the P BFM = 1.88E-5 Torr calibration for $y_{As} < 0.6$ and the P BFM < 1.2E-5 Torr calibration for $y_{As} > 0.6$. Resulting V/III ratio (gray, right axis) also shown.

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$Al_xGa_{1-x}As_yP_{1-y}$ mixed anion calibrations need to be performed for each set of growth conditions of interest. In the Lee group, mixed anion calibrations typically are specified by the set of conditions including growth temperature, cation composition,[3] approximate growth rate, and P BFM. Calibration growths investigate the relation between y_{As} and the group V "BFM ratio" measured prior to growth and the "sniffer ratio" measured during growth to create fitting curves. Both BFM ratio and sniffer ratio for III-AsP growth are defined as $As/(As + P)$ such that y_{As} increases with increasing BFM and sniffer ratio. Typically, a grower chooses a constant P BFM and adjusts the As valve position to tune the As BFM and resulting BFM ratio or to tune the sniffer ratio. See Fig. 2.3 for an example of the BFM values utilized for a $GaAs_yP_{1-y}$ step-graded buffer as well as example $GaAs_yP_{1-y}$ calibration curves.[4]

BFM ratio control allows easier implementation, as both P BFM and As BFM values are measured during pre-growth flux measurements as done for group III species, but poorer flux stability for group V valve crackers can cause larger anion composition variation over time. Sniffer ratio control requires a grower's monitoring and input to adjust the As valve position during growth such that the sniffer ratio stays at the required value. I have observed tighter and more repeatable anion composition control during a layer and between separate growths when using sniffer control, similar to former Lee group graduate students and post-docs. Typically for ease, I use BFM ratio control for calibration layers while also noting sniffer ratio during these growths. Then for device growths, I perform sniffer ratio control to realize more accurate and repeatable anion compositions.

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[3] Effects of cation composition on anion composition calibration appear to be more prevalent at low growth temperature (~480 °C). I have observed differences in anion composition calibration at ~480 °C for high-y_{As} AlGaAsP and GaAsP though growth rate may factor into these growths. However, I have observed adding x_{Al} of ~0.3 to high-y_{As} GaAsP caused no change in the resulting y_{As} at high growth temperature (tested 600 °C – 650 °C) [21]. These results have not been tested for $y_{As} < 0.5$.

[4] For high y_{As} of $Al_xGa_{1-x}As_yP_{1-y}$ layers grown at higher temperatures (typically > 550 °C) I most often adjust the P BFM lower such that the As BFM is constant. For sniffer control of these layers, these reduced P BFM values are set and the As valve is adjusted for the targeted sniffer ratio. The P valve may be adjusted when the P sniffer is noticeably different from the expected P sniffer such that the As valve does not need to be over-adjusted.

2.2 Material Characterization

2.2.1 Nomarski Optical Microscopy

Nomarski microscopy (also known as differential interference microscopy (DIC)) is an optical microscopy technique that visualizes local gradients in optical path length [72]. Nomarski microscopy works by using beamsplitters (Wollaston prisms) to first separate polarized light into two mutually coherent wavefronts and to then recombine the wavefronts after interaction with the sample, leading to added contrast from interference dependent on the optical path difference. In this work, Nomarski microscopy was performed with a Zeiss AxioScope A1 using reflected light setup and DIC mode. Nomarski microscopy captured the as-grown surface morphology of samples after growth to check for growth flaws such as roughened morphology or pit defects. Lattice-mismatched growth commonly results in a crosshatch surface morphology that was compared between sample growths. More importantly for this work, Nomarski microscopy surveyed samples after defect selective etching to estimate threading dislocation density. Defect selective etching (DSE) leaves distinct pits shaped as rectangular pyramids and Nomarski microscopy enhances the image contrast for these etch pits to enable easier pit counting.

2.2.2 Atomic Force Microscopy (AFM)

AFM investigates the surface morphology of samples to provide a quantitative image of the surface topography at much smaller scales than Nomarski microscopy that can be used to quantify surface roughness and to investigate surface features and patterns. AFM operates by measuring the deflection of a cantilever with a sharp probe tip that closely tracks the specimen surface in z direction based on measurement of the force interaction between tip and specimen while the cantilever is scanned in x and y direction. A photodiode measures cantilever deflection by tracking position of a laser reflected from the cantilever backside near the probe tip. A

piezoelectric scanner controls movement of the cantilever in x, y, and z direction. Sampling of this force interaction varies depending on the selection of AFM mode and probe used for imaging, each having strengths, weaknesses, or additional data that can be measured beside topography.

In this work, I utilized a Digital Instruments (now Bruker) Multimode NanoScope IIIa with ScanAsyst-Air probe tips to perform PeakForce Tapping mode imaging. PeakForce Tapping periodically taps the specimen with the probe tip for force curves with piconewton sensitivity at every pixel. The peak force obtained from these curves is utilized for feedback control, and ScanAsyst can auto-optimize scanning parameters for rapid, high-quality images. Typically, I collected 10×10 μm^2 images of as-grown surface morphology to extract the root-mean-square (RMS) roughness and to compare the resulting topography between samples with varied growth conditions. In some cases, 1×1 μm^2 to 20×20 μm^2 images were collected to investigate features such as surface steps and morphological defects like pits or trenches or to quantify the dimensions of features such as etch pits from DSE.

2.2.3 Scanning Electron Microscopy (SEM)

The scanning electron microscope is a versatile tool for examination and analysis of samples at much greater resolution and depth of field than optical microscopes. SEM obtains images by raster scanning a focused electron beam over a sample surface and detecting a signal from the interaction of the electrons with sample atoms. An electron gun provides electrons with low energy spread by emitting electrons from a cathode material by thermionic emission and/or field emission and then accelerating these electrons through the anode opening. The accelerating voltage is the difference between the cathode and anode and determines energy of the resulting electron beam. Following, a set of apertures and electromagnetic lenses reduces and focuses the electron beam to be a small spot size on the sample surface, and pairs of deflection coils raster

scan the beam across the sample surface. Like AFM, user-input scan parameters determine the scan size and pixel count. The electron beam penetrates and interacts with sample atoms producing multiple different signals that can be detected as the beam is scanned to produce an image with contrast from relative signal strength. Adjusting the accelerating voltage modifies the electron-sample interaction volume, with higher accelerating voltage causing a broader and deeper interaction volume. Lowering accelerating voltage can improve resolution but decreases signal-to-noise ratio.

Various interactions from different scattering processes can be collected depending on the detectors available on a SEM system to obtain a mix of information about a sample. Scattering events between the incident electron beam (primary electrons) and atoms can eject lower-energy electrons from atoms (secondary electrons), return incident electrons back out of the sample (back-scattered electrons (BSE)), produce characteristic x-rays, or generate electron-hole pairs that could produce photons. Secondary electron imaging (SEI) is the most common mode and results in contrast related to surface topography. Elastic scattering causes BSE, so signal from BSE depends more strongly on atomic density, atomic number, and crystal structure (if any). As such BSE detection can enable contrast between adjacent materials or even mapping modes depending on electron diffraction. Additional detection tools can investigate variations in current generated for a diode sample, luminescence properties, or material composition from analysis of characteristic x-rays.

In this work, different SEM techniques were applied with different SEM systems. A Hitachi S-4800 was used with SEI/BSE and cleaved samples to image the growth cross-section to determine layer thicknesses and growth rates for MBE flux calibration. A JEOL JSM-7000F was used both for SEI surveys of pits formed after DSE and for electron channeling contrast imaging

(ECCI), a diffraction-based BSE technique. A JEOL JSM-6060LV was used with electrical feedthrough for electron beam-induced current (EBIC) mapping of solar cell devices on a custom probe stage. These defect investigation techniques will be discussed in detail in Chapter 3.

2.2.4 High-Resolution X-Ray Diffraction (HRXRD)

HRXRD is used for analysis of epitaxial semiconductor layers to determine in-plane and out-of-plane lattice constants to extract layer composition, strain, and relaxation. HRXRD measurements require a highly monochromatic x-ray beam for high resolution. An x-ray tube generates both Kα and Kβ lines that are then filtered by Ge monochromators to realize a Kα x-ray beam with minimal wavelength spread and low angular divergence. A goniometer precisely positions the x-ray source, detector, and sample holder to defined scan angles with respect to each other as well as to correct for sample mounting misalignment with sample rotation and tilts.

A strong diffracted signal is observed when the source, detector, and sample are aligned such that the Bragg condition is satisfied. For a set of crystallographic planes with indices (h k l) the Bragg condition is $\lambda = 2d_{hkl} \sin \theta_{hkl}$, where λ is the x-ray wavelength, d_{hkl} is the interplanar spacing, and θ_{hkl} is the Bragg angle. The interplanar spacing is related to the lattice constant $a = d_{hkl}\sqrt{h^2 + k^2 + l^2}$. Alternatively, the Bragg condition can be written based on reciprocal vectors as $\overrightarrow{G_{hkl}} = \overrightarrow{K_{dif}} - \overrightarrow{K_{inc}}$, where $\overrightarrow{G_{hkl}}$ is the reciprocal lattice vector for a set of planes and $\overrightarrow{K_{dif}}$ and $\overrightarrow{K_{inc}}$ are the wave vectors of the diffracted and incident beams, respectively. The reciprocal lattice vector is normal to the correlated plane with length determined by d_{hkl}, and the diffracted and incident beams have length determined by λ such that the first Bragg condition form discussed above can be derived.

Since metamorphic growth has materials with the same crystal structure and crystal registry but different lattice constants, the interplanar spacings appropriately scale such that the reciprocal

lattice scales inversely. In addition, biaxial strain modifies the out-of-plane and in-plane lattice constants in opposite directions dependent on Poisson's ratio, causing a stretching of the reciprocal lattice in one direction and squeezing in the other. To capture these changes to the reciprocal lattice of multiple stacked layers, reciprocal space mapping (RSM) measurements scan an area of reciprocal space and capture the diffraction peaks from each material for a specific (h k l). Typically RSM measurements include both (004) for a symmetric RSM to determine out-of-plane lattice constants and crystallographic tilts and either (115) or (224) for an asymmetric RSM to determine both in-plane and out-of-plane lattice constants after accounting for tilt. Following, relaxed lattice constant to determine material composition from Vegard's law as well as strain relaxation can be calculated using the strained lattice constants. More detailed explanation of HRXRD measurements for relaxed lattice constant and strain relaxation determination can be found in Chapter 3.4 of [73].

In this work, HRXRD measurements were performed with either a PANalytical Phillips X'Pert or a Bruker D8 ADVANCE system. RSM was performed for symmetric (004) and asymmetric (115) in glancing-exit geometry to determine composition and strain relaxation. RSM measurements were utilized extensively to determine composition for MBE calibrations. For GaP on Si, measurements were performed for both the A-direction and B-direction to investigate strain relaxation from α-dislocations and β-dislocations, respectively. Further explanation of geometry and correspondence to dislocation type can be found in Appendix A. For $GaAs_yP_{1-y}$/GaP compressively strained superlattice (CSS) samples on GaP, symmetric (004) line scans were fit in Bruker DIFFRAC.SUITE software to determine y_{As} and CSS period thickness.

2.2.5 Hall Effect Measurement

Resistivity and Hall effect measurements with the van der Pauw method enable determination of sheet resistance, doping type, sheet carrier density, and majority carrier mobility of semiconductor layers; knowing layer thickness allows calculation of conductivity and majority carrier concentration. The van der Pauw method utilizes four-point measurement with current sourced through one set of contacts and voltage measured through the other set to determine resistances in different orientations. A common geometry has thin, square samples with a contact at each corner. Resistivity measurements are determined from sourcing current and measuring voltage for the parallel contact sets. Hall effect measurements are determined by applying an external magnetic field orthogonal to the sample and then sourcing current and measuring voltage for the perpendicular contact sets. The sourced current under this magnetic field causes charge accumulation at one side of the layer due to the Lorentz force on electrons or holes. The accumulated charge results in an electric field perpendicular to current flow that can be measured as the Hall voltage.

In the Lee group, an Accent HL5500PC Hall Effect Measurement System is the primary tool for determining carrier concentration for MBE-grown doping calibration samples. In practice, a Hall sample is cleaved from the growth wafer into a roughly-square piece and an indium contact is soldered onto the surface at each of the four corners. Often a highly-doped contact layer is grown on top of the targeted calibration layer to make the metal-semiconductor contacts more likely to be Ohmic than Schottky. For these samples, the indium contacts are soldered on the contact layer, and then used as a hard mask for selective wet etching of the contact layer. Hall effect and resistivity measurements were performed at two different current values and current-voltage characteristics were observed to check if contacts affected the measurement values. For samples

with Schottky contacts such as indium on GaP, the rectifying behavior made Hall effect measurements inconsistent and inaccurate, though resistivity measurements were consistent.

2.2.6 Raman Spectroscopy

Raman spectroscopy is a light scattering technique that can probe phonon modes to provide information on molecular bonding in a sample. Most commonly Raman spectroscopy is used for chemical analysis to identify molecules by the structural "fingerprint" of peaks in the Raman spectrum. As used in this work, Raman spectroscopy can compare changes in phonon modes for a crystal under different strain states. Raman scattering is inelastic scattering of incident photons by phonons shifting the photon energy either up or down with an energy difference indicative of the phonon mode. A sample is typically illuminated with an incident laser beam at an unabsorbed wavelength. The resulting forward- or back-scattered light is collected through a monochromator at a detector, and then plotted by the resulting frequency shift in a Raman spectrum.

In this work, a Horiba LabRAM HR confocal Raman microscope was used with 532 nm laser in back-scattering geometry to investigate the local Raman spectrum of GaP on Si samples to compare strain. In addition, a rotatable half-wave plate rotated the laser polarization relative to the stationary sample. Polarized micro-Raman spectroscopy allows sampling of phonon modes from bonding in different crystalline direction and can reveal anisotropic strain.

2.3   Solar Cell Characterization

Solar cells are semiconductor devices that convert sunlight to electricity by absorbing photons from the incident solar spectrum to generate electron-hole pairs and then separating these carriers to produce a photocurrent and photovoltage. As a result, solar cell performance depends on how well incident light is absorbed and on how well generated carriers are collected. Both of these factors depend strongly on the optical and electronic properties of materials in the solar cell

architecture. Due to the combination of optical properties of the layer stack, photons incident upon the device will either be reflected away, absorbed in specific layers, or transmitted. Since electron-hole pairs only exist for a short time before recombining, the absorber layer is a *p-n* junction to assist current collection. The built-in electric field can sweep minority carriers through the depletion region into the oppositely-doped side of the junction such that these carriers become majority carriers. Electron-hole pairs that recombine in the absorber do not contribute to current. Refer to Chapter 4 of [73] for in-depth explanation of how solar cells operate.

Measuring the current-voltage characteristics of a solar cell device under illumination can easily demonstrate the efficiency of the device (efficiency = max power output / power input from illumination). However, detailed understanding of the solar cell device performance and how to modify the device architecture for higher efficiency requires additional device characterization and analysis. Refer to Chapter 5 of [73] for more in-depth technique explanation.

2.3.1 *Current-Voltage Measurements*

Current-voltage measurements are used to investigate diode characteristics and performance of solar cell devices. As *p-n* diodes in the dark, the current-voltage relation is well-established as the ideal diode equation: $J = J_{o,n} \left[\exp \left(\frac{qV}{nkT} \right) - 1 \right]$ where J is current density, $J_{o,n}$ is reverse saturation current density, q is electron charge, V is voltage, n is ideality factor, and k is the Boltzmann constant, and T is temperature. Ideality factor typically has a value between 1 and 2 depending on the dominant recombination mechanism in the device: oversimplified as 1 for recombination in quasi-neutral region and 2 for recombination in depletion region. Often solar cells can be described by the superposition of an n = 1 diode with an n = 2 diode. The right-hand-side (RHS) of the ideal diode equation is referred to as dark current density. Under light illumination, the photocurrent density J_L is subtracted from the dark current density such that the

current-voltage relation becomes $J = J_{o,1} \left[\exp\left(\frac{qV}{kT}\right) - 1\right] + J_{o,2} \left[\exp\left(\frac{qV}{2kT}\right) - 1\right] - J_L(V)$. J_L may be voltage-dependent because of field-assisted carrier collection where the shrinking depletion region thickness with increasing voltage decreases carrier collection due to insufficient minority carrier diffusion lengths.

For the practical case, a series resistance and a parallel shunt resistance should be added to this equation. Series resistance (R_S) drops increased voltage with increasing current such that this behavior dominates the diode characteristics at high current levels when diode resistances become small. Shunt resistances offer a parallel current pathway that can be dominant at low bias when diode resistances are large such that most current flows through the shunt path. Dark current-voltage (DIV) measurements set J_L to zero to enable extraction of reverse saturation current densities as well as series and shunt resistances.

Under illumination, the resulting lighted current-voltage (LIV) curve has a few special points, called figures of merit. Short-circuit current density J_{SC} is the name for $J_L(0\ V)$. J_{SC} is indicative of the carrier collection of a solar cell like quantum efficiency. Open-circuit voltage V_{OC} is the voltage where current is zero. At open-circuit condition current does not flow through the series resistance, so the V_{OC} is unaffected by R_S. Instead photogenerated current is recombined through the dark current diodes. For an ideal diode at open-circuit, $V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_{o,n}} + 1\right)$ such that the biggest contribution to changing V_{OC} is the dominant $J_{o,n}$ term(s) that can vary by orders of magnitude depending on solar cell design and material quality. Solar cells in this work are primarily dominated by $n = 2$ ideality due to high defect densities. Thus, V_{OC} is most strongly controlled by $J_{o,2}$ which can be described as $J_{o,2} = qWn_i/2\tau_o$ where W is the depletion width, n_i is the intrinsic carrier concentration, and τ_o is the minority carrier lifetime [74] Lastly, the max power point voltage V_{MPP}, current density J_{MPP}, and power density P_{MPP} are defined at the point

on the LIV curve with max power density that occurs near the transition from behavior dominated by J_L (and shunt resistance) to behavior dominated by dark diode characteristics (and series resistance). P_{MPP} is divided by the power density of the incident spectrum to determine the efficiency. The fill factor FF describes the "squareness" of the resulting LIV curve as $FF = \frac{P_{MPP}}{V_{OC} \times J_{SC}} = \frac{V_{MPP}}{V_{OC}} \frac{J_{MPP}}{J_{SC}} = V_{ratio} \times J_{ratio}$. Additionally, splitting the FF into V_{ratio} and J_{ratio} can be useful to isolate FF loss to the effects of series resistance or shunt resistance and field-assisted carrier collection.

An additional current-voltage measurement called Suns-V_{OC} can be utilized to analyze solar cell diode characteristics without the effect of series resistance. J_{SC} and V_{OC} pairs are measured as a function of illumination intensity often with a voltage-controlled LED. Then, each J_{SC}-V_{OC} pair is used as a J-V data point to describe a curve similar to a DIV curve without series resistance. Suns-V_{OC} can aid determination of $J_{o,1}$ since R_S often dominates the behavior of DIV prior to current levels where $J_{o,1}$ behavior would dominate over $J_{o,2}$. Also, Suns-V_{OC} curves can be shifted by J_L to form a pseudo-LIV curve with an ideal fill factor FF_o to further investigate FF losses in LIV.

In this work, current-voltage measurements were performed with a Keithley 2420 source meter unit (SMU). DIV was measured in a dark room. $J_{o,n}$ and n were extracted from semi-log fitting and R_S was extracted from linear fitting. LIV measured at the University of Illinois was under approximate 1-sun AM1.5G (Chapter 6.4 and 7) or AM0 (Chapter 8.3) illumination from an ABET 10500 single-source solar simulator. LIV measured at NASA Glenn Research Center was under calibrated 1-sun AM0 (Chapter 8.2) illumination from their custom triple source AM0 solar simulator [75]. LIV figures of merit were determined for multiple devices and the best device results are presented. Suns-V_{OC} measurements were performed by including a Keithley 2400 SMU

for controlling the voltage of a blue LED collimator source (470 nm, Mightex Systems LCS-0470-03-22) that was roughly focused onto the device with a focusing lens. Voltage to the LED was adjusted to control light intensity and the Keithley 2420 SMU determined J_{SC} and V_{OC} at the intensity before the LED voltage was stepped and another J_{SC}-V_{OC} pair measured. Neutral density filters were placed in the light path to increase the intensity range measured by orders of magnitude.

2.3.2 Quantum Efficiency Measurements

External quantum efficiency (EQE) describes the current collected by a solar cell per incident photon flux as a function of photon wavelength or energy, therefore quantifying the current loss per wavelength. This includes current losses from reflection, transmission, and recombination in the solar cell. Photon absorption in a semiconductor material is energy-dependent; photons with lower energy than the bandgap are unabsorbed, photons with energy greater than the bandgap are absorbed, and photons with higher energy are absorbed more strongly. Note, when discussing quantum efficiency measurements photon energies are typically described by photon wavelength instead. Short-wavelength (higher-energy) photons are absorbed more strongly within less material thickness than long-wavelength photons (still shorter than bandgap wavelength). As a result, short-wavelength photons generate electron-hole pairs only near the top of the solar cell facing the incident light and long-wavelength photons generate pairs that extend deeper into the device.

Quantum efficiency can distinguish carrier recombination losses occurring near the front/back of the device when probed with short/long-wavelength photons. Reflection losses can be measured and removed from EQE to give the internal quantum efficiency (IQE) to better compare short- vs long-wavelength carrier recombination losses. Alternatively, reflection losses

can be strongly reduced with anti-reflection coating layers to often give roughly similar comparison. Strong recombination loss at short/long-wavelength indicates that minority carriers generated far from the junction do not have sufficient diffusion length to reach the depletion region, recombine at the interfaces of adjacent interfaces, or transfer into adjacent materials and recombine there. Higher-bandgap barrier layers are often used on both the front and back side of the absorber junction to reduce interface recombination and block minority carriers from transferring into these barrier layers. For example. an ideal *p*-type barrier for minority electrons would have higher conduction band energy than the *p*-absorber to block minority electrons and the same valence band energy to allow conduction of majority electrons. However, a drawback for the front barrier (called the window layer) is that it absorbs a portion of the short-wavelength photons. Window layers are typically chosen with high bandgap and lower thickness to reduce this absorption loss. Barriers for the back side are called back surface field layers.

In this work, EQE and reflectance were measured with a PV Measurements Inc. QEX7 system. This system creates a monochromatic beam of light[5] and uses a beam splitter to direct half the beam at a monitor photodiode to measure the photon flux and half at the sample solar cell to measure the solar cell current at the chosen wavelength. Prior to measurement the sample solar cell is replaced with a calibrated photodiode to recalibrate the monitor photodiode signal as a function of incident wavelength. Then the EQE of the sample solar cell device[6] was measured by determining the current at each wavelength, dividing by the light beam area, and dividing by the incident photon flux with one minority carrier generated per photon. Solar cell J_{SC} for a specific solar spectrum can be calculated by integrating the EQE curve with the solar spectrum converted

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[5] Xenon arc lamp emission directed through chopper, monochromator, and filter wheel.
[6] Ideally the solar cell device does not have top metal grid fingers to shadow the incident light and is bigger than the light spot.

to proper units (photon flux per wavelength) and multiplying by electron charge. The EQE near the bandgap can also be used to determine the bandgap of a solar cell (see Chapter 5 of [73]). Additionally, the reflectance was measured by mounting the sample at slight angle and capturing the reflected light beam with the calibrated photodiode. Reflectance was calculated by dividing the resulting EQE curve for the calibrated photodiode with light reflected by the EQE with direct light.

CHAPTER 3

EXTENDED DEFECT CHARACTERIZATION

Minimizing performance-reducing extended defects, particularly threading dislocations, is important to advancing epitaxial III-V/Si multi-junction (MJ) solar cell technologies. Methods are needed to identify these defects and estimate defect densities at various stages of the growth structure to guide growth conditions and layer design for defect reduction. Different properties of extended defects can generate contrast when investigated by different techniques. The structural imperfection of extended defects can create strong diffraction-based contrast for techniques such as plan-view or cross-sectional transmission electron microscopy (PVTEM or XTEM) with "two-beam" conditions, electron channeling contrast imaging (ECCI), or x-ray topography (XRT). Strong non-radiative recombination at extended defects can be observed in cathodoluminescence (CL) or electron beam-induced current (EBIC) mapping from either reduced photon generation or carrier collection of generated electron-hole pairs. Also, altered chemical reactivity at the improper bonding of defects can enhance etch rates at the defects to give defect selective etching (DSE) resulting in morphology observable with microscopy. Comparison of advantages/disadvantages for most of these techniques is given in Chapter 6 and 7 of [76].

In this chapter I give a summary of the extended defect characterization techniques utilized throughout this dissertation primarily to estimate threading dislocation density (TDD) of GaP and ~1.7 eV GaAsP on Si. I discuss the use of DSE for GaP by hot phosphoric acid etching, ECCI, and EBIC of GaAsP single-junction (1J) solar cells. I also detail additional experiments in each section including controlled etch pit size and different microscopy surveys for DSE, dislocation multiplication/introduction from ECCI exposure, and accelerating voltage-dependent EBIC.

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3.1 Defect Selective Etching (DSE)

3.1.1 Technique Information

DSE can reveal dislocations as etch pits when etching is limited by the surface kinetics and dislocations offer reduced energy barriers to etching. Often the crystallographic orientation of the surface affects etching rates and can lead to anisotropic etching [77]. DSE nucleates removal of monolayers at dislocation cores more readily than the surface, and as etching continues deeper down the dislocation an etch pit forms with sidewalls that can reveal higher-angle planes. For zincblende III-V semiconductors, the polarity of crystallographic planes is important as group V {111}B planes are more reactive than group III {111}A planes due to higher electron density for the group V face (see Table A.1 in Appendix A for list of A and B planes). As a result, etch pits for III-V (001) wafers are most commonly anisotropic etch pits elongated in $[1\bar{1}0]$, such that commercial wafers have the orientation identified based on etch pit shape [77].

In this dissertation, DSE of GaP (001) was performed with hot phosphoric acid [36], [65], [78]–[80]. Uncut H_3PO_4 (85 wt.%, aq) in a Pyrex glass dish was heated on a hot plate to ~130 °C – 145 °C solution temperature as measured by immersed thermocouple and samples were etched on the order of minutes. DSE revealed rectangular pyramidal etch pits. The elongated direction was confirmed to be the $[1\bar{1}0]$ direction [79], [80]; the elongation of etch pits for cleaved pieces of GaP/Si (001) templates was used to determine crystallographic directions for other defects such as as-grown trenches (discussed in Chapter 4.2). GaP TDD can be estimated by the etch pit density from counting the distinctly-shaped etch pits. Previous comparisons of hot H_3PO_4 DSE of GaP (001) with other techniques for TDD estimation showed 1-to-1 correlation of etch pits with threading dislocations in PVTEM [81] and dark spots from dislocation in EBIC of a GaP *p-n* diode [80]. In addition, both Nay Yaung *et al.* [82] and I (Fig. 3.1) observed nearly 1-to-1 correlation
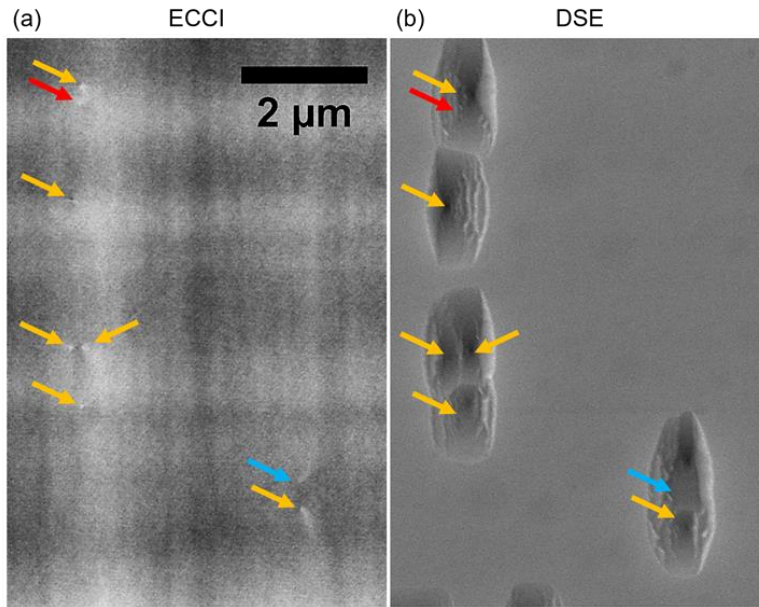
Fig. 3.1: Comparison of dislocations observed for GaP on Si (001) at the same location with (a) ECCI and (b) secondary electron imaging after hot H_3PO_4 DSE. DSE was performed following ECCI. Arrows indicating threading dislocation positions in (a) are exactly copied to (b). Orange arrows mark dislocations observed in both ECCI and DSE. Red arrow marks a dislocation observed in ECCI but not DSE. Blue arrow marks a dislocation that appears to have moved slightly upward for DSE. Note, etch pit shape was affected by short uncut HCl sonication and rinsing to remove carbon surface contamination from SEM during ECCI that prevented DSE.

with threading dislocations in ECCI, with DSE slightly undercounting due to tightly-bunched dislocations.

3.1.2 Microscopy Choice and Etch Pit Size Control

Different microscopy techniques can be utilized to determine etch pit density. Nomarski microscopy is most commonly used after DSE to rapidly survey and capture large areas (~10^{-3} cm^2 per image; 1×10^6 cm^{-2} TDD would result in ~1000 etch pits in this area). However, due to limited imaging resolution and large (~1 μm) unambiguous etch pits, Nomarski microscopy underestimates the TDD when dislocations are < 0.5 μm apart. TDD estimates from Nomarski microscopy become less accurate as the TDD increases, as the overlap problem becomes more severe [82], [83]. Secondary electron imaging (SEI) in a scanning electron microscope (SEM) greatly improves accuracy, though precision worsens due to the much smaller image areas (~2 – 9

48
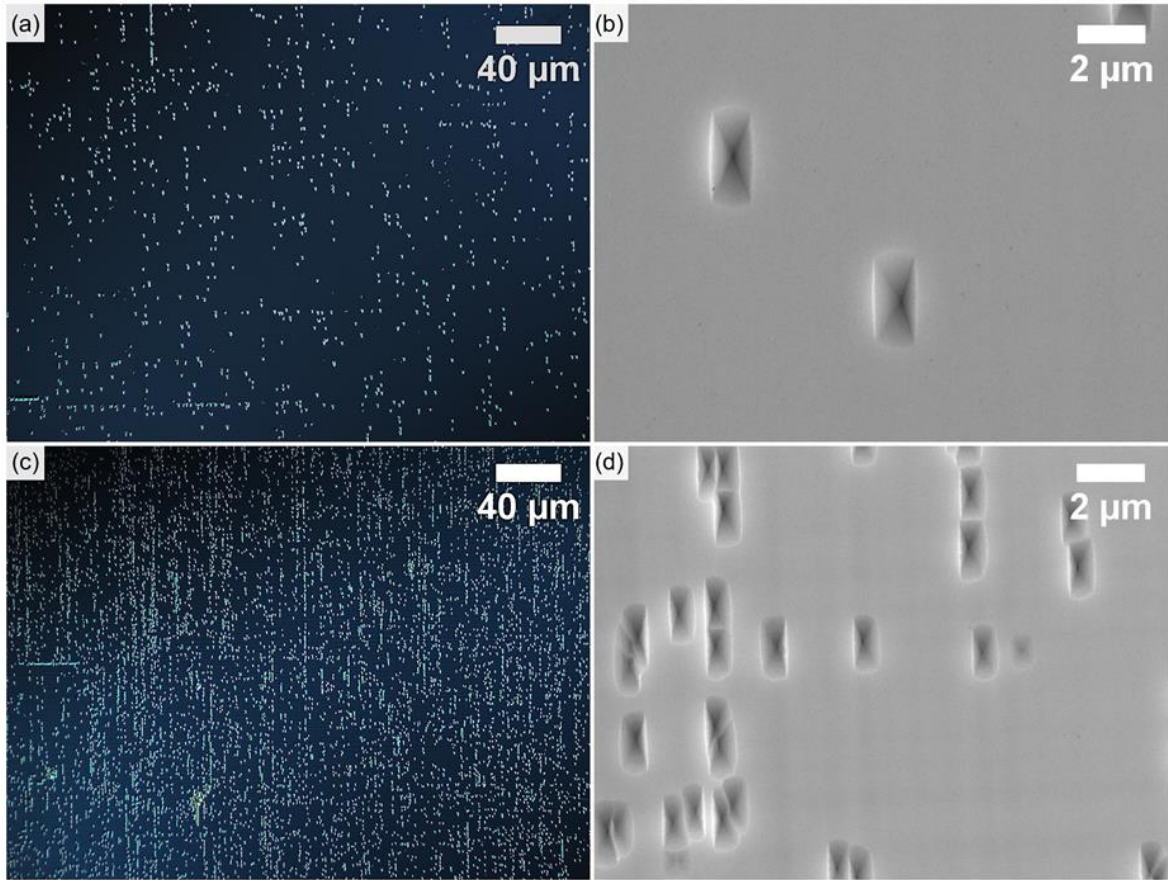
Fig. 3.2: Comparison of typical (a, c) Nomarski and (b, d) SEI micrographs after hot phosphoric acid DSE of GaP on Si (001) for (a, b) a low TDD sample ~1.1×10^6 cm^{-2} with longer etch time and for (c, d) a high TDD sample ~1.5×10^7 cm^{-2} with shorter etch time. Image area for (a, c) is ~9.6×10^{-4} cm^2 while for (b, d) is ~2.2×10^{-6} cm^2.

$\times$ 10^{-6} cm^2 per image is typical for my work) [36]. Fig. 3.2 displays the above advantages/challenges of both Nomarski and SEI micrographs. For high TDD samples, Nomarski for Fig. 3.2(c) was not able to accurately estimate TDD while SEI for Fig. 3.2(d) could easily distinguish overlapping etch pits based on the deepest point of etch pit relating to the dislocation core. However, counting a high number of etch pits was more time-consuming for SEI surveys. Typical Nomarski surveys included 5 images for ~5×10^{-3} cm^2 total area. On the other hand, SEI surveys included 5 sets of images (a set being a 3×3 grid of adjacent images) for 45 total images and ~$1 - 4 \times 10^{-4}$ cm^2 total area.
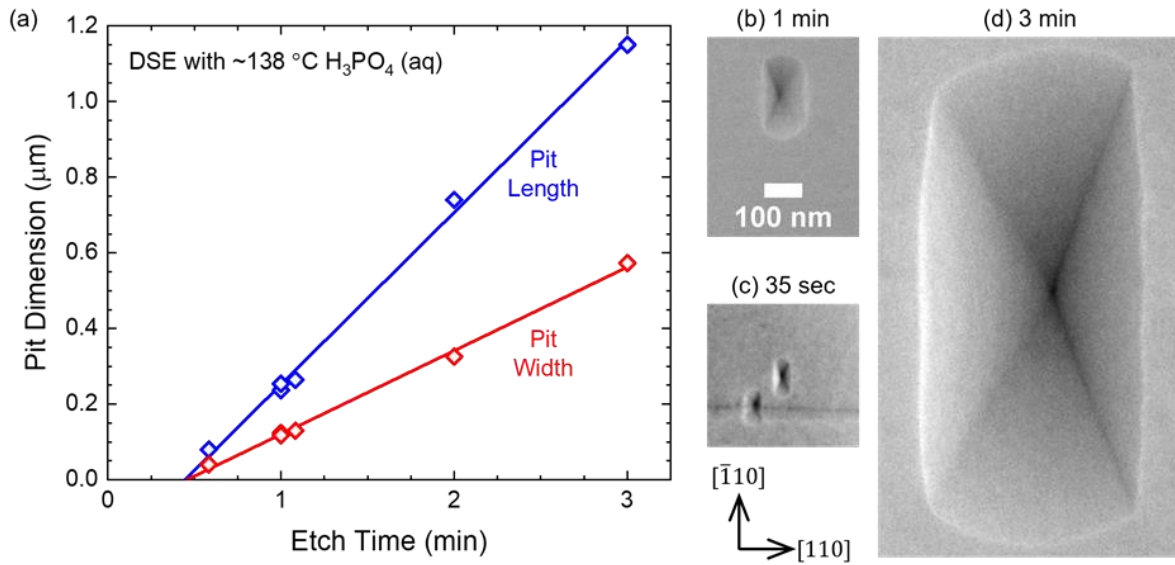
Fig. 3.3: Etch pit size control for hot phosphoric acid DSE of GaP on Si (001). (a) Pit length in $[\bar{1}10]$ (blue) and width in $[110]$ (red) of etch pits vs etch time with linear fits. (b – d) Example etch pit sizes for various etch times observed with SEI micrographs. All are at the same scale as shown in (b) and oriented similar to the axes below (c).

Improving over previous Lee group work having ~1 μm etch pit sizes, I demonstrated improved etch pit size control with consistent solution temperature and controlled etch timing (Fig. 3.3). I observed a consistent time delay for pit formation such that slightly exceeding the delay time enabled sub-100 nm pit dimensions with ~35 sec etching in ~138 °C H_3PO_4 (aq) achieving ~80 nm pit length and ~40 nm pit width. Additionally, atomic force microscopy (AFM) can quantify etch pit dimensions including pit depth. Full etch pit dimensions with ~1 min etching in ~138 °C H_3PO_4 (aq) were ~0.25 μm pit length, ~0.12 μm pit width, and ~24 nm pit depth. Small scan area and longer scan times limit the applicability of AFM for TDD estimation only to very high TDD samples. SEI after short DSE etch times is a better option for very high TDD >> 10^7 cm^{-2}.[7]

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[7] If threading dislocations occupied every adjacent 100 nm × 100 nm square, then the TDD would be 10^{10} cm^{-2}.

3.2 Electron Channeling Contrast Imaging (ECCI)

3.2.1 Technique Information

ECCI is an SEM-based technique capable of imaging structural defects with diffraction-based contrast when near specific electron channeling conditions. ECCI relies on crystal orientation-dependent back-scattered electron (BSE) signal, as some orientations align such that incident electrons can "channel" through parallel lattice planes and lessen BSE intensity. Variation of the BSE signal as a function of incident electron direction for a crystal viewed under low magnification in SEM creates an electron channeling pattern (ECP), analogous to Kikuchi lines in TEM [84], [85]. Kikuchi-like bands form in an ECP between a lattice plane and its opposite pair with highest electron channeling (darkest BSE signal) at the edges of a band where the beam aligns to the plane and highest back-scatter at the center of a band (brightest BSE signal). Since ECCI relies on changes in BSE signal, only defects close to the surface (typically < 50 nm) generate contrast.

Structural defects such as dislocations cause local changes in the lattice orientation that alter BSE yield dependent on the affected orientations. Defect contrast is typically optimized where the BSE signal slope is maximized, closer to the edges of bands, such that lattice perturbations from a defect either increases back-scattering or channeling [86], [87]. Due to the crystallographic nature of ECP bands, different bands can be chosen that correlate to different planes and generate contrast specific to a particular diffraction condition analogous to imaging in TEM with a "two-beam condition". Tilting and rotating the sample while viewing the ECP can enable alignment of the sample with respect to the electron beam. Then, imaging at high magnification views the sample with the selected alignment and resulting back-scattering and channeling. Defects imaged in ECCI may be identified based on the same invisibility criterion as
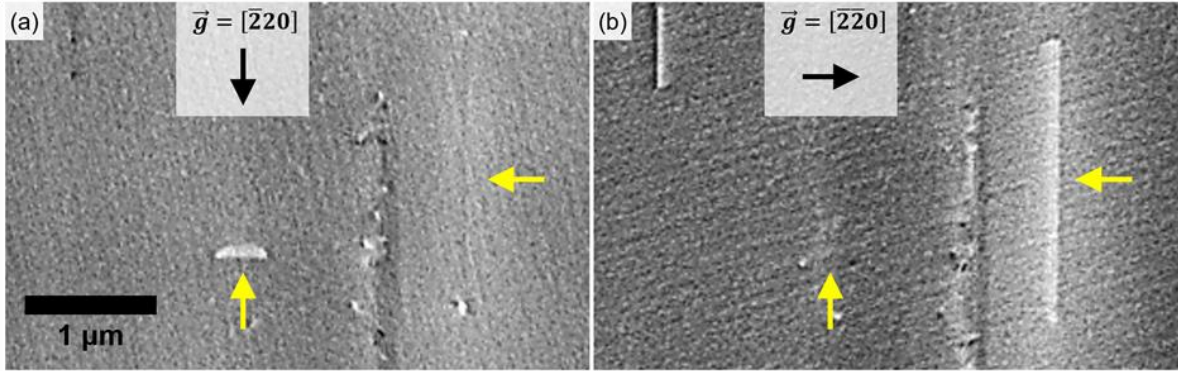
Fig. 3.4: Example of invisibility criterion for stacking faults. ECCI comparison for stacking faults and threading dislocations of GaP on Si using either (a) $\vec{g} = [\bar{2}20]$ or (b) $\vec{g} = [\bar{2}\bar{2}0]$ channeling condition. Yellow arrows indicate the location of stacking faults that are either visible or invisible depending on $\vec{g}$. Threading dislocations are also observed with white/black contrast which rotates based on $\vec{g}$.

TEM ($\vec{g} \cdot \overrightarrow{R(r)} = 0$, where $\vec{g}$ is the diffraction condition and $\overrightarrow{R(r)}$ is the defect translation vector; for a dislocation this is $\vec{g} \cdot \vec{b} = 0$ and $\vec{g} \cdot \vec{b} \times \vec{u} = 0$, where $\vec{b}$ is the dislocation's Burgers vector, and $\vec{u}$ is the dislocation's line direction) [85], [87], [88]. See Fig. 3.4 for an invisibility criterion example with ECCI for stacking faults in GaP on Si. Some defects like stacking faults have an invisibility criterion while others like threading dislocations do not.

In this work, ECCI was performed in a JEOL JSM-7000F system with Schottky field emission gun at 30 kV accelerating voltage to investigate trenches and dislocation pileups (see Chapter 4.2) due to ECCI's high resolution and ability to identify defects. Multiple diffraction conditions were imaged including different ⟨040⟩ or ⟨220⟩. Mixed conditions at the intersection of ⟨040⟩ and ⟨220⟩ were most commonly utilized to include contrast from both conditions on the same image. Samples were viewed with COMPO mode from an annular BSE detector. Typical ECCI images ranged from 7000 × (~220 μm^2) to 30,000 × (~13 μm^2) magnification (area).

3.2.2 Evidence of Dislocation Introduction for GaP on Si during ECCI

During the investigation showing nearly 1-to-1 correlation between DSE etch pits and ECCI threading dislocations for relaxed ~545 nm GaP on Si (see Chapter 3.1), I surprisingly

observed evidence of dislocation creation or multiplication occurring in some samples due to ECCI exposure. TDD from DSE etch pit density following ECCI exposure was $> 2 \times$ higher than for TDD from DSE of pieces of the same sample without ECCI exposure. In addition, the local TDD near the area with ECCI exposure was comparatively higher than far away on the same piece.

Fig. 3.5 shows results for a systematic investigation of local TDD relative to a region covered with ECCI exposure. A center region was exposed for ECCI images, DSE was performed, and then SEI images were captured in the ECCI exposed region and in a grid extending out in either the $[1\bar{1}0]$ or $[110]$ directions. To give statistical significance, a 4×4 grid of typical $7000 \times$ ECCI image exposures were taken to enable typical $3500 \times$ SEI images to be taken by twos in either direction. ECCI was performed at 30 kV with mixed $\langle 040 \rangle$ and $\langle 220 \rangle$ diffraction condition.[8]
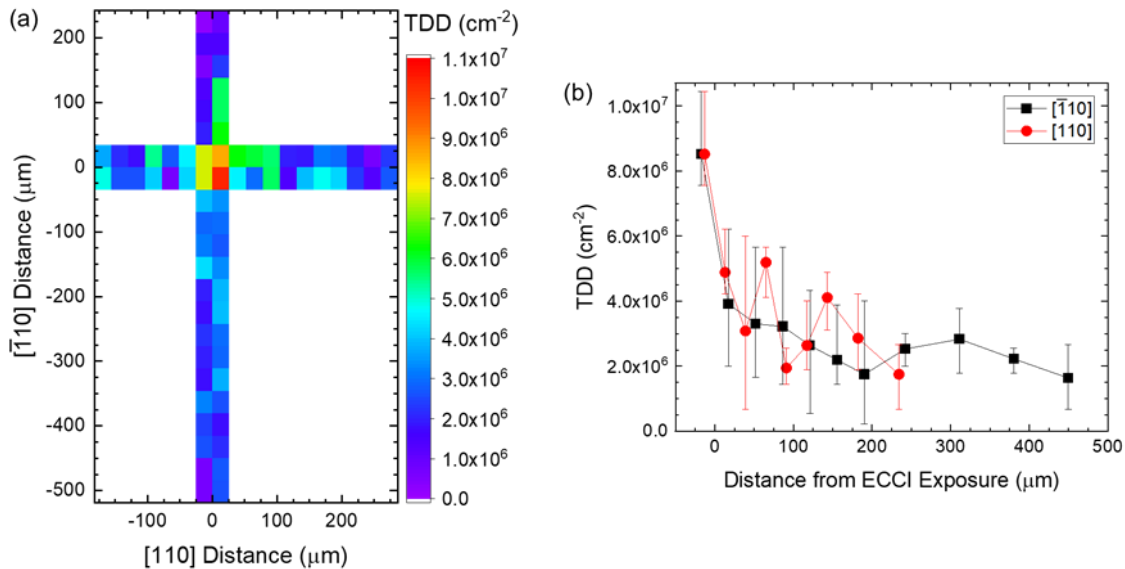
Fig. 3.5: Investigation of local TDD for relaxed GaP on Si as a function of distance from a region following ECCI exposure. (a) Colormap of TDD at sampled locations determined by counting of etch pits from SEI images after DSE. Each color "pixel" represents a single SEI image. ECCI exposures were performed to roughly cover the area of the 4 centermost image areas. No ECCI exposure was performed elsewhere on this sample piece. (b) TDD vs distance from ECCI exposure region for both $[\bar{1}10]$ and $[110]$ directions. "0" is relative to the edge of regions with and without ECCI exposure. Error bars represent standard deviation between images at the same distance.

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[8] SEI micrographs collected with 15 kV accelerating voltage in case SEI exposure would also move/create threading dislocations.

TDD was much higher within the ECCI-exposed region ($> 8 \times 10^6$ cm^{-2}) and decreased sharply outside this region back toward the expected bulk TDD value (~$1 - 2 \times 10^6$ cm^{-2}).

Fig. 3.6 displays SEI images obtained from an additional experiment to demonstrate that ECCI exposure both moves and creates new threading dislocations. DSE was performed on a relaxed ~545 nm GaP on Si sample and etch pits were noted with SEI images after this "1st DSE before ECCI exposure". Following, a single 7000 $\times$ ECCI image exposure was taken at some of the SEI image locations. DSE was performed again on this sample and repeat SEI images were taken after this "2nd DSE after ECCI exposure". Fig. 3.6(b) shows ECCI caused movement of some dislocations from their original etch pits (etch pit with flat bottom after 2nd DSE that was previously pyramidal after 1st DSE). In addition, ECCI led to the creation of many new threading dislocations (small etch pits not observed in Fig. 3.6(a)). Many times more small etch pits were observed than etch pits with flat bottoms, such that only a very small fraction of the new etch pits could be
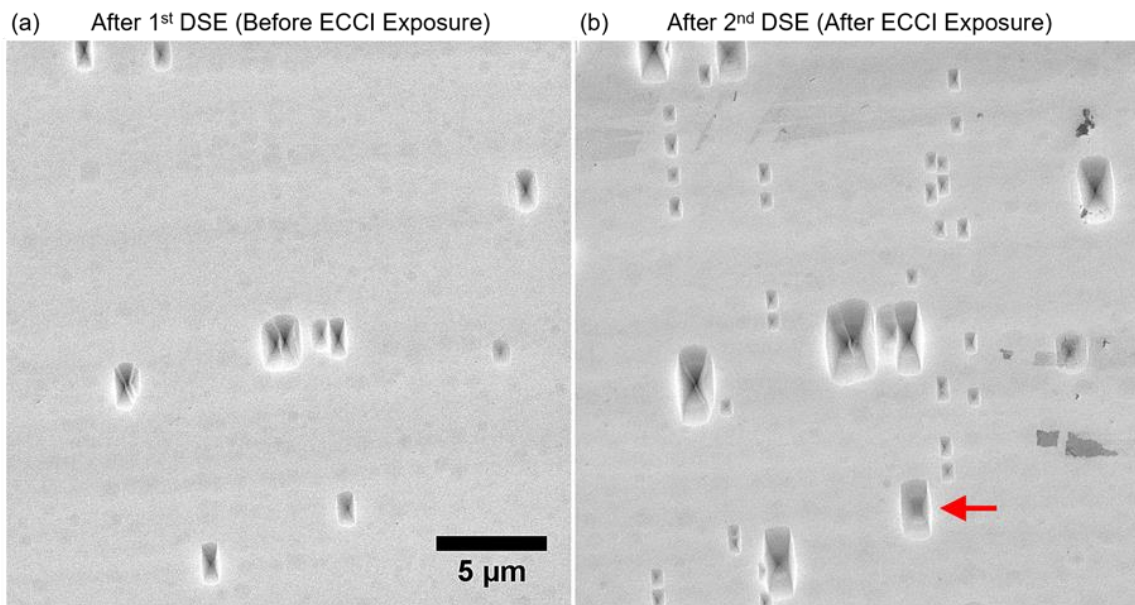
Fig. 3.6: SEI micrographs of relaxed GaP on Si after repeated DSE (a) before ECCI exposure and (b) after ECCI exposure to demonstrate ECCI can move threading dislocations and create new dislocations. Following ECCI exposure and performing DSE a 2nd time, three types of etch pits emerged. (1) Etch pit from 1st DSE just grew larger. (2) Etch pit from 1st DSE was etched to a flat bottom as the threading dislocation moved from within the etch pit during ECCI exposure. See red arrow. (3) New small etch pit from 2nd DSE as new dislocations were created by ECCI exposure.

accounted for by dislocations leaving their original etch pits. Callahan *et al.* previously showed ECCI can cause recombination-enhanced dislocation glide for GaAs on Si resulting in movement of dislocations and even annihilation of interacting threading dislocations [89]. Similar behavior may be occurring for GaP on Si, however, the cause of strong dislocation introduction or multiplication for my samples using this SEM tool is not known. ECCI is regularly utilized by Boyer for GaP on Si samples of varying GaP thickness without mention of additional dislocation introduction during ECCI measurements [86].

3.3   Electron Beam-Induced Current (EBIC) Mapping

3.3.1 Technique Information

EBIC mapping is a SEM-based technique to map local variations in current collection of a solar cell junction. Due to inelastic scattering events, the incident electron beam generates electron-hole pairs in the solar cell material. These carriers can be separated by the *p-n* junction and collected by the solar cell as the electron beam-induced current. Electrically-active defects such as threading dislocations cause increased local non-radiative recombination and therefore reduce the EBIC signal to give regions of dark contrast. Threading dislocations are observed as dark spots in EBIC images enabling TDD estimation of fabricated solar cells[9] from determining the density of dark spots. The solar cell device is electrically connected to a vacuum feedthrough such that the EBIC short-circuit current signal can be mapped by the SEM computer as the electron beam is raster scanning. The low current signal is first passed to a current preamplifier for conversion to a voltage signal that is read by the SEM computer and displayed as grayscale signal for the image.

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[9] "Quick and dirty" fabrication of solar cell devices for plan-view EBIC analysis may work for unfabricated solar cell materials if Ohmic contact can be made. This could be possible with soldered or painted metal contacts. Note that Schottky diodes can also be utilized for EBIC analysis of semiconductor materials [90].

In this dissertation, plan-view EBIC[10] was performed in a JEOL JSM-6060LV system with tungsten filament thermionic emission gun at accelerating voltages ranging from 2 kV to 16 kV; most commonly 6 kV to 12 kV was used. Hand-made probe assemblies were attached to a SEM stage to probe fabricated metal contact pads of the solar cell device to be measured. The probe for the bottom contact is grounded to the SEM stage while the probe for the top contact is wire-connected to a vacuum BNC feedthrough. This SEM system does not have a load-lock but instead has the specimen stage on a retractable drawer and vents/pumps the entire specimen chamber when unloading/loading samples. This feature enabled the probed electrical connection to be easily maintained as the sample is moved into position underneath the electron gun. Outside vacuum the electrical BNC feedthrough was connected as the input current signal of a Stanford Research Systems SR570 low-noise current preamplifier. The output voltage signal was connected to the auxiliary channel of the SEM system. Typical EBIC images ranged from $600 \times$ (~34,000 μm^2) to $2500 \times$ (~2200 μm^2) magnification (area).

Both the SR570 controls and SEM computer brightness control allowed signal processing to generate EBIC images with good contrast in grayscale. The SR570 gain mode was typically set to either high bandwidth or low noise modes. Both input offset (current added/subtracted prior to amplification) and sensitivity (amplification; current per output voltage) were adjusted to obtain a voltage signal range acceptable for the SEM computer to convert by a factor to grayscale values. A user-made control software allowed finer control of SR570 parameters than by the SR570 front panel alone. SEM brightness control finely shifted the grayscale values into 0 – 255 values (displayed black – white). Similar sensitivity values for a given accelerating voltage were often utilized between similar samples to give similar amplification of the original electron beam-

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[10] Cross-sectional EBIC can also be performed and used for diffusion length evaluation [91].

induced current. Different solar cell junction design or materials may affect optimal sensitivity values (see Fig. 3.9 in the next section).

3.3.2 Accelerating Voltage-dependent EBIC

Increasing the electron gun accelerating voltage inreases the interaction volume where the electron beam interacts with the sample. The shape of the interaction volume for SEM is commonly teardrop-like with smallest diameter at the sample surface and with a larger-diamter rounded shape deeper in the sample due to the accumulation of many random scattering events widening the paths of electrons [92]. With higher accelerating voltage all dimensions of the interaction volume increase. Due to this, lower accelerating voltages are more surface-sensitive and can achieve higher imaging resolution. However, this often leads to reduced signal-to-noise ratio. While the dependence of interaction volume on accelerating voltage for a material is often determined with Monte Carlo simulations, rough approximation can estimate the electron interaction depth (z) and width (w) in μm with $z \approx 0.1 \times E_0/\rho$ and $w \approx 0.077 \times E_0/\rho$ with accelerating voltage (E_0) in kV and density (ρ) in g/cm^3 [93].[11] For ~1.7 eV GaAs$_{0.77}$P$_{0.23}$, this would result in interaction depth (width) of 56 nm (43 nm) with 2 kV and 1.3 μm (1.0 μm) with 16 kV.[12]

For EBIC of a solar cell, varying the accelerating voltage alters the initial location of generated electron-hole pairs. Higher accelerating voltages cause more electron-hole pairs deeper in the material. Minority carriers generated in the junction depletion region are swept by the junction electric field into the oppositely-doped layer to be collected as current. Minority carriers generated outside the depletion region need to first diffuse to the depletion region; diffusion occurs by random walk so carriers have equal likelihood of going to the depletion region as to the opposite

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[11] Note [93] has the density unit in kg/m^3 which is in error based on calculation that follows in the reference. Density is g/cm^3 with a 3 g/cm^3 silicate mineral having ~2 μm interaction depth at 15 kV accelerating voltage.
[12] Calculating interaction depth (width) similarly for important accelerating voltages in this work: 0.29 μm (0.22 μm) at 6 kV, 0.45 μm (0.35 μm) at 8 kV, 0.82 μm (0.63 μm) at 12 kV, 1.27 μm (0.98 μm) at 16 kV.
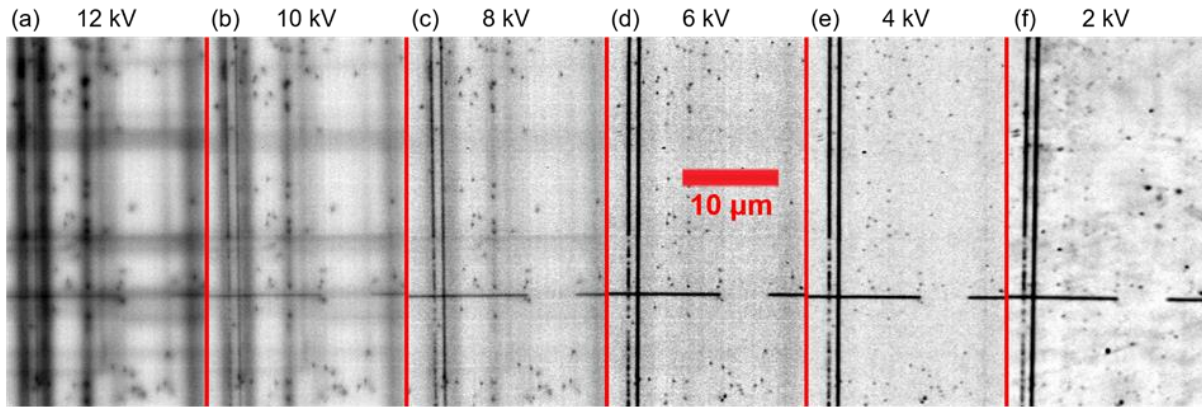
Fig. 3.7: Comparison of EBIC images at the same location for a ~1.7 eV GaAsP 1J solar cell with varying accelerating voltage of (a) 12 kV, (b) 10 kV, (c) 8 kV, (d) 6 kV, (e) 4 kV, (f) 2 kV. Thick dark line defects are observed at 12 kV and vanish by ~6 kV. Thin dark line defects are faintly observed at 12 kV and get stronger contrast with lower accelerating voltage.

direction. Due to this, defects at the front (back) side of the solar cell are more likely to affect EBIC at lower (higher) accelerating voltages. In addition, the junction depletion region depth will also affect the dependence on accelerating voltage.

I performed EBIC of a ~1.7 eV GaAsP 1J solar cell with varying accelerating voltage at the same location to compare defects at various depths in the thin n^+/p junction. The solar cell structure included 20 nm n^+-AlInP window layer, 50 nm n^+-GaAsP emitter (~1×10^{18} cm^{-3}), 1000 nm p-GaAsP base (~1×10^{17} cm^{-3}), and 25 nm p^+-GaInP back surface field (BSF) layer resulting in a depletion region extending from ~60 nm to ~210 nm depth from the sample surface. Fig. 3.7 shows that three types of defects were observed depending on the accelerating voltage chosen. Thick dark line defects (DLDs) were observed at higher accelerating voltages and lessened in contrast with lower accelerating voltage until these DLDs vanished at around 6 kV or 4 kV. Thin DLDs were observed sharper but less intense than thick DLDs at higher accelerating voltage and increased in contrast with lower accelerating voltage. Based on discussion in the previous paragraph, these results indicate two populations of DLDs, thick (thin) DLDs near the back (front) surface of the solar cell junction causing increased non-radiative recombination. The broadening
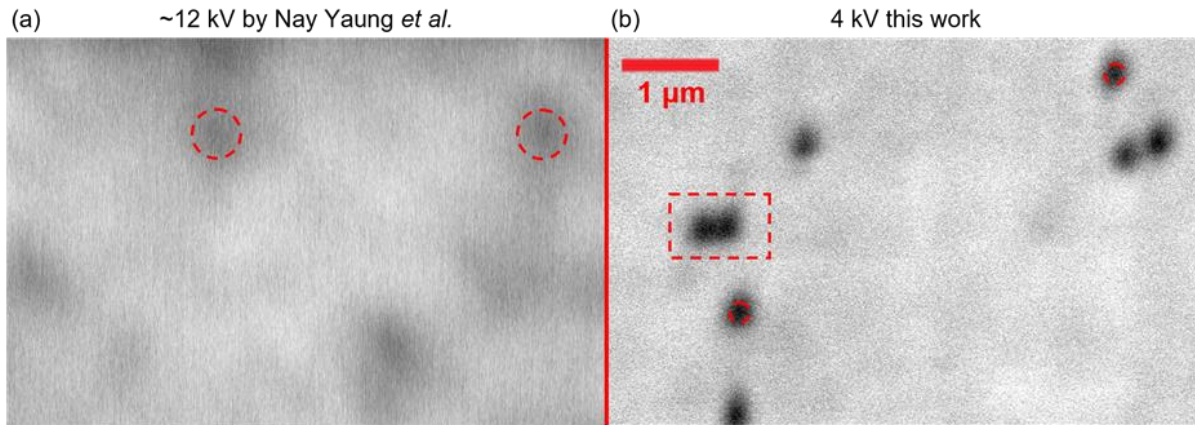
Fig. 3.8: Comparison of EBIC dark spot size from threading dislocation with accelerating voltage of either (a) ~12 kV or (b) 4 kV. Red dashed circles show the approximate dark spot diameter. The red dashed box for (b) shows two resolved dark spots with centers ~250 nm apart. (a) was adapted from [82].

electron interaction width likely caused some broadening of thick DLDs. See Chapter 7.2 for further discussion of DLDs in this work.

Thick DLDs vanishing at low accelerating voltage revealed additional threading dislocations (dark spots) that had been covered by thick DLDs. Lowering the accelerating voltage also enabled smaller dark spots from threading dislocations due to lower electron interaction width. This resulted in sharper dark spots and higher resolution of adjacent dark spots. Fig. 3.8 shows reduced dark spot diameter with lower accelerating voltage, decreasing diameter from ~500 nm at ~12 kV for prior Lee group work by Nay Yaung *et al.* [82] to ~200 nm at 4 kV in this work. In comparison, Nay Yaung observed threading dislocations with ECCI at similar magnification to have apparent diameters of ~50 nm – 100 nm [82]. Fig. 3.8 also demonstrates a pair of dark spots from threading dislocations resolved at ~250 nm apart. However, decreasing accelerating voltage further to 2 kV (Fig. 3.8(f)) appears to include contrast from the surface morphology possibly from surface contamination.

As shown in Fig. 3.9, I observed offset accelerating voltage dependence when the depletion region width was increased, as with an $n^+/i/p$ compared to n^+/p junction design. Both ~1.7 eV
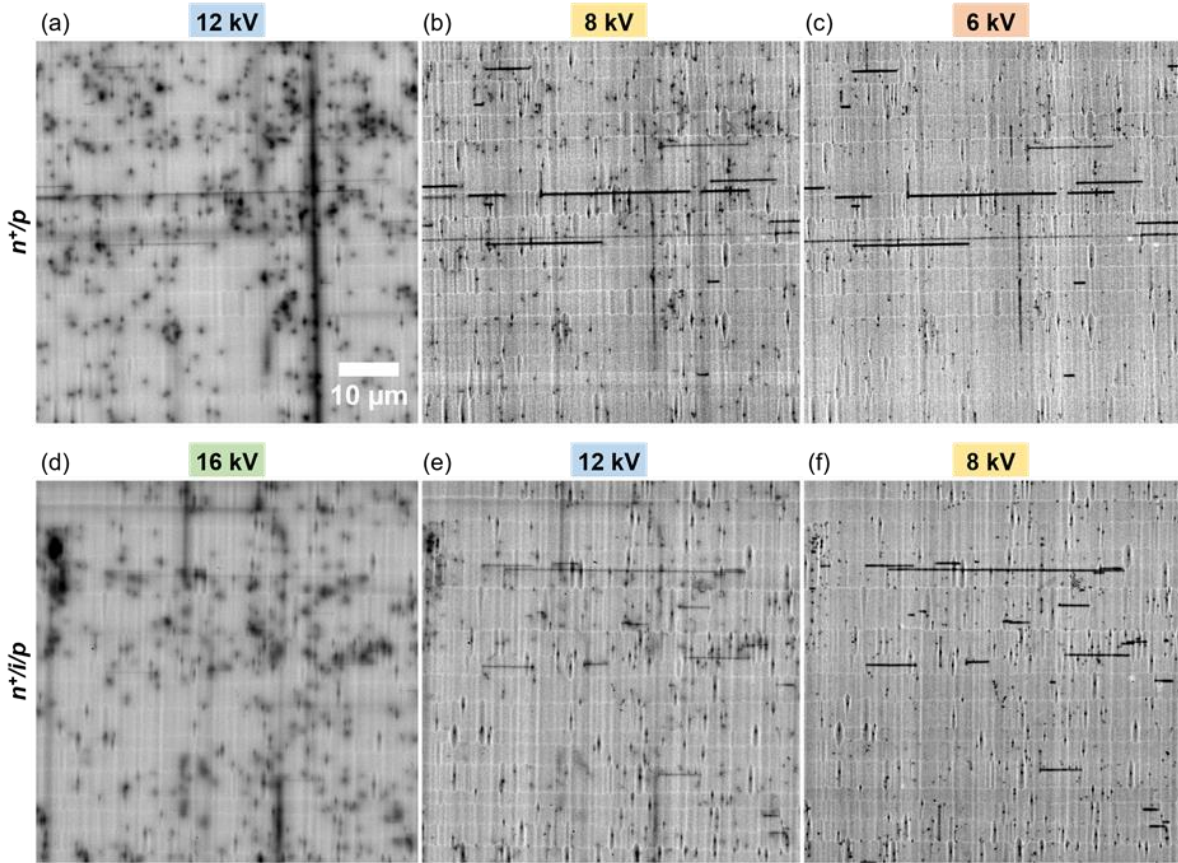
Fig. 3.9: Comparison of EBIC for ~1.7 eV GaAsP 1J solar cells with either (a – c) n^+/p or (d – e) $n^+/i/p$ junction design with varied accelerating voltage (d) 16 kV, (a, e) 12 kV, (b, f) 8 kV, or (c) 6 kV. Both solar cells have ~1.5 μm total absorber thickness, though the $n^+/i/p$ cell has ~325 nm of the p-type base replaced with an intrinsic layer. Note both solar cells have the "AlGaAsP BSF + spacer" design discussed in Chapter 7.2 reducing the density of thick DLDs at the highest accelerating voltages.

GaAsP 1J solar cells that were compared used ~1.5 μm of total GaAsP absorber, but the $n^+/i/p$ design replaced ~325 nm of the p-type base with an intrinsic layer to increase the depletion width similarly. Due to increased depth of the depletion region, higher accelerating voltages were needed to observe similar EBIC contrast (compare Fig. 3.9(a – c) vs (d – f)). By including the intrinsic layer to increase depletion width, minority electrons generated deep in p-type base were closer to the edge of the depletion region and therefore less likely to recombine at back surface DLDs. As a result, higher accelerating voltages were needed to observe similar effects from back surface DLDs by generating minority electrons at greater depth closer to the DLDs.

3.4   Chapter Findings

The main purpose of this chapter was to explain defect characterization techniques primarily for threading dislocation density (TDD) estimation. In addition, technique findings in this chapter are listed below:

- Nomarski microscopy allow easy large-area surveys for TDD estimation after defect selective etching (DSE), while secondary electron imaging (SEI) allows more accurate but less precise TDD estimates in particular for high TDD samples with DSE etch pits often overlap.

- Hot phosphoric DSE of GaP on Si (001) is controllable by etch time such that sub-100 nm etch pit dimensions can be achieved.

- Electron channeling contrast imaging (ECCI) exposure for our relaxed GaP on Si caused both movement and creation/multiplication of threading dislocations.

- Populations of electrically-active "dark line defects" (DLDs) as observed in electron beam-induced current imaging (EBIC) are present in our GaAsP top cells at both the front and back surface of the active region.

- Contrast from EBIC depends on the location of generated electron-hole pairs in comparison to the depletion region, such that the electron beam accelerating voltage choice depends on solar cell junction design.

CHAPTER 4

DEFECT REDUCTION OF RELAXED GAP ON SI

Reducing the density of performance-damaging threading dislocations penetrating the ~1.7 eV GaAsP top cell grown on Si is necessary to reach double-junction efficiencies exceeding those Si can achieve on its own. To reach lower threading dislocation density (TDD) for the GaAsP top cell, optimization of growth design and growth conditions is needed for the buffer layers used to manage dislocation introduction to relieve misfit strain and expand the lattice constant. In our group's previous work Nay Yaung *et al.* investigated growth temperature (T_{growth}) optimization for both relaxed *p*-GaP buffers and *p*-GaAs$_y$P$_{1-y}$ step-graded buffers [34]. Nay Yaung observed a tradeoff between TDD dominated by either insufficient dislocation glide velocity at low T_{growth} or rampant dislocation introduction at high T_{growth}, leading to a minimum TDD for relaxed *p*-GaP on Si of 1.7×10^6 cm^{-2} [34]. In this chapter, I describe investigations of relaxed *p*-GaP morphology and morphological defects performed in an effort to reduce dislocation nucleation sources. Two heterogeneous features, trenches and dislocation pileups, increased in density more strongly with T_{growth} than TDD and were shown to have very high local TDD. Later in this chapter, I describe a two-step GaP buffer designed to first suppress dislocation introduction and the formation of trenches and dislocation pileups with a thin low T_{growth} layer before changing to a high T_{growth} layer for higher dislocation glide velocity during strain relaxation. The two-step design enabled TDD as low as $1.0 - 1.1 \times 10^6$ cm^{-2} for relaxed *p*-GaP on Si [36].[13]

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[13] Parts of this chapter are reproduced from [R. D. Hool *et al.*, "Relaxed GaP on Si with low threading dislocation density," *Appl. Phys. Lett.*, vol. 116, no. 4, p. 042102, Jan. 2020, doi: 10.1063/1.5141122.], with the permission of AIP Publishing.

4.1 GaP on Si Background

GaP is convenient as a starting point for epitaxial III-V growth on Si (001) before further enlarging the lattice constant to grow direct-gap III-V layers with larger lattice constants such as 1.7 eV $GaAs_{0.77}P_{0.23}$ (GaAsP) or 1.4 eV GaAs. Among conventional zincblende III-V semiconductors (AlGaIn-PAsSb compounds), GaP has the smallest lattice mismatch to Si with a misfit strain of -0.36% at room temperature (RT); due to difference in thermal expansion coefficients the misfit strain increases to -0.45% – -0.48% at typical T_{growth} of 500 °C – 700 °C. In addition, GaP acts as a model system to understand defect formation for moderate-mismatch III-V nucleation and growth. Either fully-strained or partially-relaxed GaP layers – thin or thick relative to the experimental critical thickness of ~90 nm [31], [32] – can be grown to study the processes of III-V nucleation on Si or strain relaxation through dislocations, respectively.

Extensive research for GaP on Si has been performed with thin, pseudomorphic GaP layers below the critical thickness to address the challenge of zincblende III-V nucleation on diamond cubic Si before further expanding the lattice constant [23]–[27], [94]–[102]. Irregular initial GaP island formation and coalescence over the Si surface lead to nucleation-related defects such as anti-phase domains and stacking faults which often propagate through growth. Careful Si substrate preparation to produce a double-stepped surface [23]–[27], [95], [96], [98] and modulated Ga and P precursor dosing to cover the surface with a single element analogous to atomic layer deposition [24]–[26], [94], [97], [100]–[102] enabled preferential nucleation of domains with the same polarity. As a result, nucleation-related defects have either been eliminated for offcut Si or self-terminated within 10s of nm of GaP for on-axis Si, realizing commercial GaP/Si templates of ~45 nm GaP on 300 mm diameter Si on-axis substrates without propagating defects [24], [28].

However, even with nucleation-related defects controlled and moderate misfit strain, growing thicker GaP layers past the critical thickness can cause high TDD $> 10^7$ cm^{-2} [26], [35]–[37]. This high GaP TDD on Si is unacceptable since high TDD is generally expected to persist in subsequent III-V growth, where larger misfit strains need to be relaxed to reach direct-gap III-V compounds. Indications from our group's prior research by Nay Yaung *et al.* suggest that higher TDD in relaxed GaP/Si leads to higher final ~1.7 eV GaAsP TDD [76]. For example, Nay Yaung observed TDD increased from 0.2×10^6 cm^{-2} for GaP to $1.4 - 2.8 \times 10^6$ cm^{-2} for ~1.7 eV GaAsP when grown on bulk GaP substrates, and from 1.9×10^6 cm^{-2} to $4.0 - 4.5 \times 10^6$ cm^{-2} when grown on high-quality GaP/Si templates [34], [76].

Poor dislocation dynamics in GaP hamper misfit relaxation and can lead to high dislocation introduction rates. As shown in Fig. 4.1(a), Yonenaga and Sumino observed roughly two orders of magnitude slower dislocation glide velocities in GaP than in GaAs [103], [104]. When dislocation glide kinetics limit TDD, Fitzgerald's dislocation dynamics model predicts TDD should reduce with increasing T$_{growth}$ as the increased glide velocity leads to longer misfit line lengths [30]. However, the barrier for dislocation nucleation is easier to overcome with higher
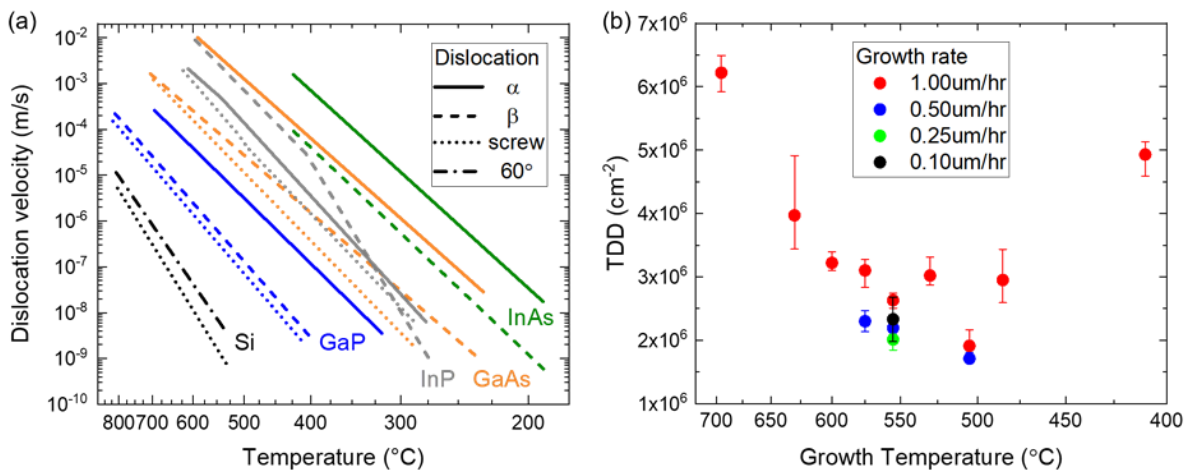
Fig. 4.1: (a) Arrhenius plot of dislocation glide velocities for different dislocation types (α, β, and screw for III-V compounds; 60° and screw for Si) in various common semiconductor single crystals. Adapted from Ref. [104]. (b) Relaxed *p*-GaP TDD on GaP/Si with varied growth temperature and growth rate. Temperature axes shown as inverse absolute temperature. Adapted from Ref. [34].

temperatures and may lead to a transition with increasing T_{growth} from a glide-dominated regime with exponentially decreasing TDD to a nucleation-dominated regime with exponentially increasing TDD, as observed by Isaacson *et al.* [105]. Previously in our group, Nay Yaung *et al.* studied the TDD of relaxed *p*-GaP (500 nm) on GaP/Si templates as a function of T_{growth} observing this transition between 500 °C and 550 °C [34]. With T_{growth} and growth rate optimization shown in Fig. 4.1(b), Nay Yaung demonstrated relaxed *p*-GaP TDD on Si down to 1.7×10^6 cm^{-2} with high dislocation nucleation at high T_{growth} limiting further TDD reduction [34].

4.2   Morphological Defect Study

p-GaP samples were co-grown by molecular beam epitaxy (MBE) on high-quality GaP/Si template pieces free of propagating nucleation-related defects (NAsP$_{III/V}$ GmbH, Germany). Growth conditions were 500 nm thick, 0.5 μm/hr growth rate, 15 V/III ratio, and ~4×10^{17} cm^{-3} Be nominal doping unless specified. GaP/Si template pieces were cleaved from a commercial GaP/Si wafer grown by metalorganic vapor phase epitaxy (MOVPE), similar to Ref. [24], on a 300 mm (001) Si substrate with a 200 nm homoepitaxial Si buffer followed by a 45 nm pseudomorphic GaP layer (see Fig. 4.7(a) for GaP/Si template layer structure). GaP/Si template pieces were precleaned with dilute *aqua regia* (freshly-prepared 1:3:3 HNO$_3$:HCl:H$_2$O for 5 sec) prior to loading into the MBE for growth unless specified. Regardless of growth conditions, 500 nm *p*-GaP films showed roughly symmetric strain relaxation of 80% − 100% at RT (65% − 80% at T_{growth}) as measured by reciprocal space mapping (RSM) measurements with high-resolution x-ray diffraction (HRXRD). Morphological defects were studied at varied length scales by a combination of Nomarski microscopy, secondary electron imaging (SEI) in scanning electron microscopy (SEM), and atomic force microscopy (AFM) in an attempt to guide growth conditions for TDD reduction.
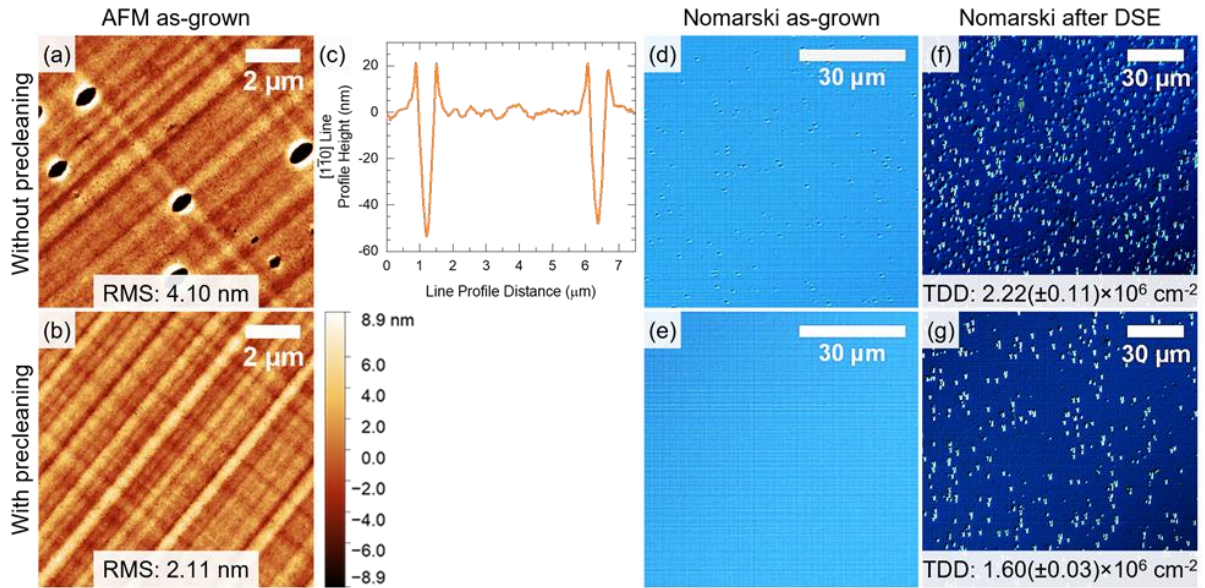
Fig. 4.2: Comparison of GaP co-grown at 530 °C on GaP/Si template pieces (a, d, f) without precleaning and (b, e, g) with dilute *aqua regia* precleaning. (a, b) AFM images of the as-grown surface morphology (z-range = 17.8 nm). (c) Line profile extracted from (a) in the $[1\bar{1}0]$ direction from top left to bottom right to show the pit morphology. Nomarski micrographs of (d, e) as-grown surface morphology and (f, g) after defect selective etching (DSE) revealing bright rectangular etch pits from threading dislocations and less bright rounded etch pits from as-grown pits. The $[1\bar{1}0]$ direction goes from top to bottom for (d – g). Modified from this work, Ref. [36].

Pit defects were observed as-grown for samples grown on GaP/Si templates without precleaning (Fig. 4.2(a, d)). As shown by AFM in Fig. 4.2(a, c), the pit defects appear like "cat eyes" such that the pit region, up to ~50 nm deep, elongates in [110] with ~20 nm tall protrusions above the baseline morphology perpendicular to the elongation. While the cat eye defects etch differently than threading dislocations during DSE – cat eye defects etch as elongated ovals and threading dislocations etch as rectangular pyramids – TDD estimation was more challenging with cat eye defects (Fig. 4.2(f)). Similar to Nay Yaung [76], performing dilute *aqua regia* precleaning of GaP/Si templates before growth eliminated these cat eye defects (Fig. 4.2(b, e)). Precleaning with dilute *aqua regia* with 1:3:3 or 1:2:2 HNO_3:HCl:H_2O for 5 – 10 sec produced similar results. In addition to making TDD estimation simpler, precleaning often lowered GaP TDD on Si by ~6 $\times 10^5$ cm^{-2}, suggesting cat eye defects may originate from contaminants on the template surface
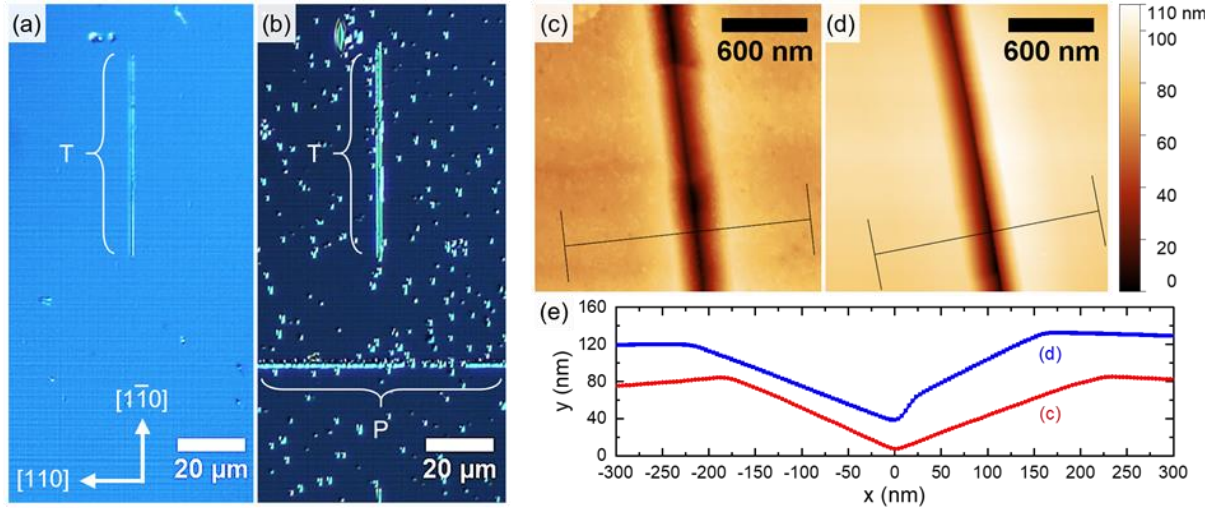
Fig. 4.3: Trench morphology for relaxed GaP on Si. Comparison of Nomarski micrographs of the same location (a) as-grown and (b) after DSE. Trenches (T, vertical, [1$\bar{1}$0]) are observed as-grown while dislocation pileups (P, horizontal, [110]) are typically not observed until after DSE. (c, d) AFM images of an example trench from separate samples. (e) Line profiles extracted as indicated from (c) and (d) in the [110] direction. Modified from this work, Ref. [36].

that act as heterogeneous dislocation nucleation sites [36]. AFM investigation of as-received GaP/Si templates without and with precleaning did not reveal any noticeable difference in surface morphology before growth.

Beside cat eye defects, trenches (T in Fig. 4.3(a)) running along [1$\bar{1}$0] had previously been observed in our group [76] as part of the as-grown morphology but not studied in detail. Surveying trenches for various 500 nm GaP samples by AFM showed trenches as valleys with depth ranging from 10 – 100 nm and wall angles ranging from ~15 – 60°, though {113}A and {114}A planes were most commonly observed; Fig. 4.3(c – e) shows two example trenches and extracted line profiles. Trenches etch in DSE as if a dislocation line, and often with dislocation etch pits nearby. As shown in Fig. 4.3(b), DSE reveals additional line features, here called dislocation pileups, running along [110]. These dislocation pileups (P in Fig. 4.3(b)) appear to have closely-spaced dislocations clustered in a line. Unlike trenches, dislocation pileups were typically not noticeable

from the as-grown surface morphology.[14] For ~500 nm GaP on Si samples, Boyer also observed

similar trench and pileup features after DSE but did not observe noticeable as-grown morphology

[86] like I found consistently for trenches running along $[1\bar{1}0]$. Based on these and below results,

trenches and pileups may both be dislocation pileups with as-grown morphology asymmetrically

influenced by the combined effects of growth conditions and strain.

Further investigation of trenches and dislocation pileups revealed both features have high

local TDD on the order of 10^8 cm^{-2} for a 1 μm-wide box centered along the feature [36]. Using

DSE with a short etch time (~1 min) reduced pit overlap enough to observe many dislocation etch

pits making a pileup and adjacent to trenches (Fig. 4.4(a)). Similarly as shown in Fig. 4.4(b, c),

electron channeling contrast imaging (ECCI) demonstrated an abundance of dislocations both

present as pileups and within/near trenches. A few short stacking faults were also observed within

trenches surveyed. Dislocations tended to be either in the center of the trench or on only one side

– for Fig. 4.4(b) dislocations in the trench sit on the centerline or to the left. This tendency is
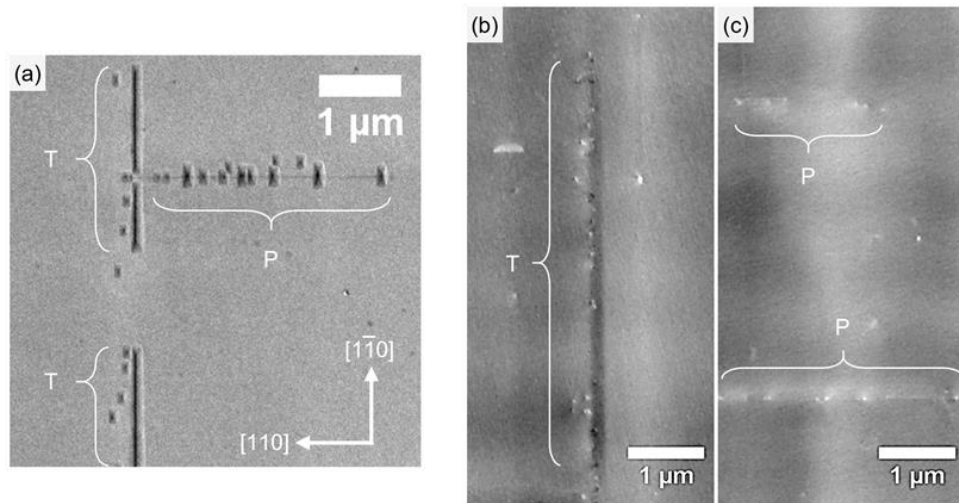
Fig. 4.4: High local TDD for trenches and dislocation pileups. (a) SEI closeup of trenches (T) and pileups (P) after DSE for a short time. Electron channeling contrast imaging (ECCI) of (c) a short trench and (d) portions of two pileups. Modified from this work, Ref. [36].

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[14] One GaP sample with very high TDD, $> 4 \times 10^7$ cm^{-2}, had trench-like as-grown morphology running along both $[1\bar{1}0]$ and [110].

similar to qualitative observations surveying greater numbers of trenches with Nomarski after DSE – see the dislocation etch pits next to the left side of the trench in Fig. 4.3(b) – and may indicate that trenches impede β-dislocations gliding in [110]. While insufficient evidence for trenches blocking β-dislocation glide has been observed, I observed strong evidence for pileups blocking α-dislocations gliding in [1$\bar{1}$0] as described later in Chapter 5.3 [65].

As shown in Fig. 4.5, trench and dislocation pileup densities both exponentially increased with increasing T_{growth} above ~500 °C. Nucleation of these dislocation-ridden features intensified much more strongly than for dislocations; trench and pileup densities increased by $> 140 \times$ and $> 50 \times$ for T_{growth} increasing from ~500 °C to ~700 °C. Since dislocations concentrated in the trenches and pileups are more challenging to include in etch pit counting for TDD estimation, and since trench/pileup densities escalate dramatically with T_{growth}, TDD estimates for samples at higher and higher T_{growth} are expected to be more and more underestimated. In addition samples at 1.0 µm/hr
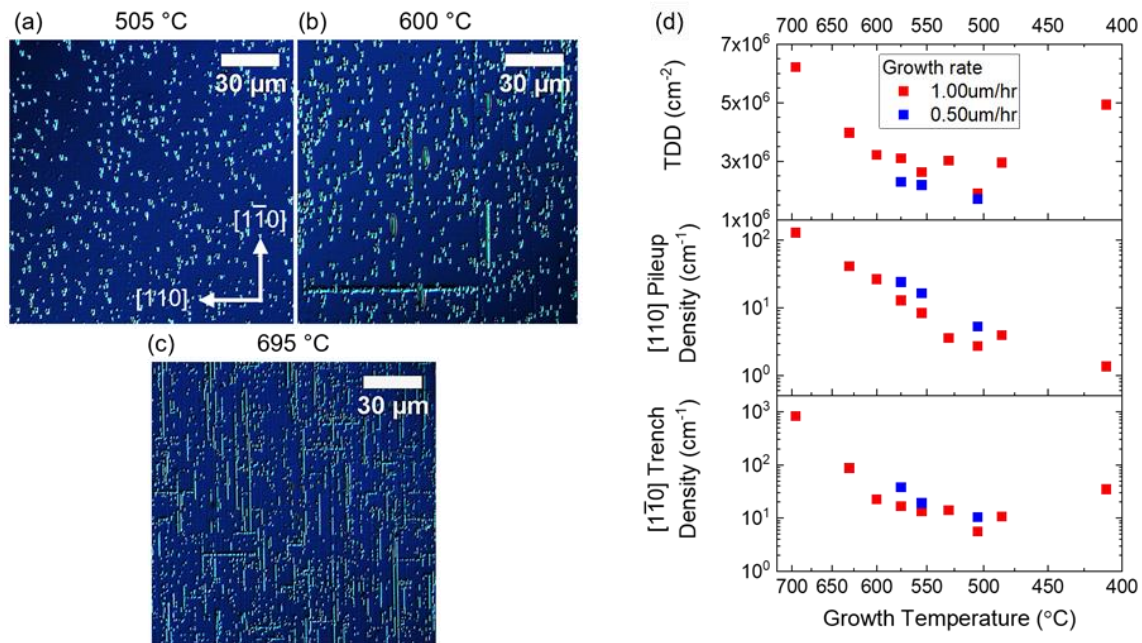
Fig. 4.5: Increasing trench and pileup density with increasing T_{growth}. Nomarski micrographs after DSE for relaxed *p*-GaP on Si at (a) 505 °C, (b) 600 °C, and (c) 695 °C representative of measured defect densities. (d) Defect densities for relaxed *p*-GaP on Si with varied T_{growth} and growth rate. Top panel data from Ref. [34].
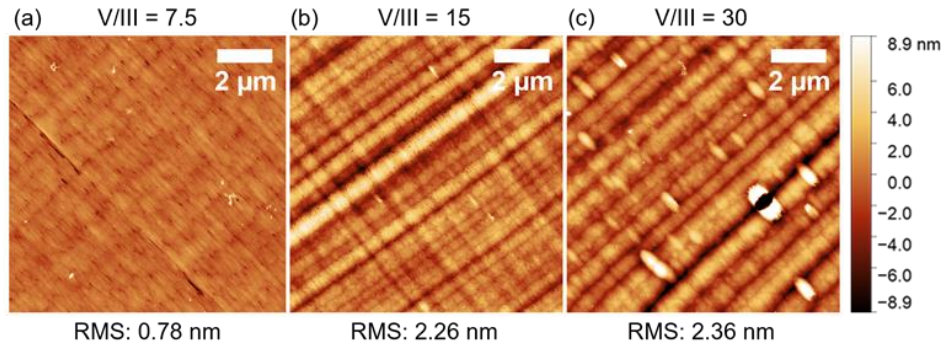
Fig. 4.6: AFM images of the as-grown surface morphology (z-range = 17.8 nm) for relaxed *p*-GaP on Si with T_{growth} = 550 °C and V/III ratio of (a) 7.5, (b) 15, and (c) 30.

and 0.5 μm/hr growth rates were compared, indicating a slight increase in trench and pileup densities with lower growth rate. Possibly the lower growth rate may allow more time for trenches and pileups to form while at high temperature.

The V/III ratio was varied from 7.5 to 30 to observe the effect of modified adatom mobility on defect densities for relaxed *p*-GaP grown on GaP/Si at 550 °C. As shown in Fig. 4.6, as-grown surface morphology was improved with lower V/III, strongly reducing RMS roughness and crosshatching. Due to increased adatom mobility with reduced V/III, the morphology appears more analogous to samples with higher T_{growth}.[15] While morphology changed, no significant changes in the densities of dislocations, trenches, and pileups were observed with varied V/III ratio.

4.3 Two-step GaP on Si for Defect Reduction

From our group's previous TDD vs T_{growth} study, Nay Yaung observed competing factors limiting the achievable TDD for relaxed *p*-GaP on Si – rampant dislocation introduction at high T_{growth} or insufficient dislocation glide velocity at low T_{growth} [34]. Samples grown with less MBE growth thickness (down to 200 nm MBE *p*-GaP on templates with 45 nm MOVPE GaP nucleation on Si) indicated that most strain relaxation occurred during the latter half of the 500 nm MBE *p*-

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[15] Note, V/III of 3.75 was later attempted with 615 °C T_{growth} and caused Ga droplets to form on the growth surface, damaging the morphology.
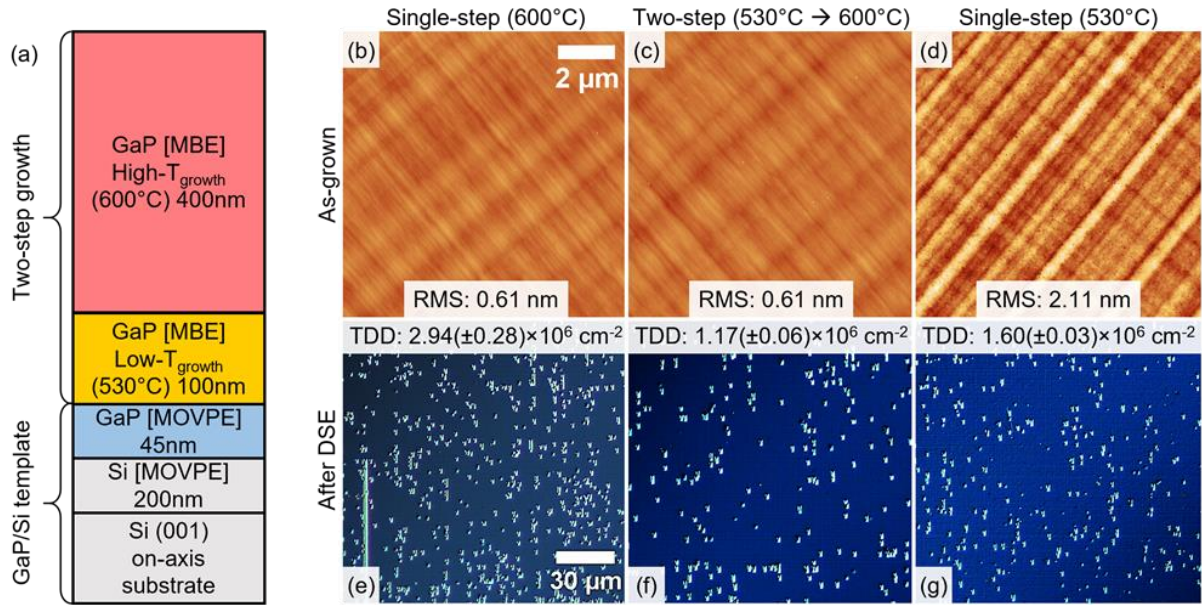
Fig. 4.7: (a) Layer structure of two-step MBE *p*-GaP growth and GaP/Si template from NAsP$_{III/V}$. Growth temperatures and thicknesses were varied for different samples but are shown here for the growth in (c) and (f). (b – d) AFM images of as-grown surface morphology (z-range = 17.8 nm) and (e – g) Nomarski micrographs after DSE for samples with growth at either (b, e) only 600 °C, (d, g) only 530 °C, or (c, f) two-step with 530 °C before 600 °C. Two-step growth yields the smooth morphology of 600 °C growth with a lower TDD than single-step growth. From this work, Ref. [36].

GaP growth even though the critical thickness would be reached after ~45 nm of MBE growth. I hypothesized that utilizing high T_{growth} for improved dislocation glide velocity might not be necessary until after the critical thickness and devised a two-step MBE growth process attempting to reduce the rampant dislocation introduction by initiating with low T_{growth} (see Fig. 4.7(a)) [36]. I suspected the low T_{growth} step would bury surface imperfections that might act a dislocation sources to suppress dislocation introduction and after pausing growth to change substrate temperature the high T_{growth} step would enable high glide velocity during GaP relaxation without triggering excessive dislocation introduction.

Two-step GaP growth with 530 °C low T_{growth} and 600 °C high T_{growth} not only reduced the GaP TDD in comparison to single-step growth at 600 °C, but also at 530 °C (Fig. 4.7 (e – g)) [36]. With two-step GaP growth, I achieved TDD significantly lower than any of our previous relaxed *p*-GaP on GaP/Si results [34]. GaP on Si surface morphology also depends strongly on T_{growth}, with

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low T_{growth} (530 °C, Fig. 4.7(d)) single-step samples being considerably rougher than their high T_{growth} (600 °C, Fig. 4.7(b)) counterparts. As shown in Fig. 4.7(b, c), nearly identical surface morphology and roughness to the single-step growth at 600 °C was observed by growing the top layer of the two-step growth at 600 °C. Two-step samples were grown with varied combinations of low T_{growth} and high T_{growth} as discussed later in this section, and consistently the morphology of two-step growths adopted the morphology for the higher T_{growth} of the second step.

A series of two-step growths was grown with varied low T_{growth} layer thickness but constant 500 nm total MBE p-GaP thickness, 530 °C low T_{growth}, and 600 °C high T_{growth}, reaching the lowest TDD for around 100 nm of low T_{growth} thickness [36]. Results for the TDD (blue circles) and AFM RMS roughness (orange diamonds) are shown in Fig. 4.8(a) for this two-step series, as well as single-step growths at 530 °C and 600 °C. The TDD decreased with increased low T_{growth} thickness up to 100 nm indicating reduced dislocation introduction. In addition, all these samples

(d) T_{growth} (°C)	Thickness (nm)	TDD (×10^6 cm^{-2})	RMS (nm)	Relaxation at RT for A-/B-directions
530	200	1.30 (±0.07)	1.12	15% / 10%
530	500	1.60 (±0.03)	2.11	93% / 93%
530+600	200+300	1.32 (±0.03)	0.70	106% / 87%
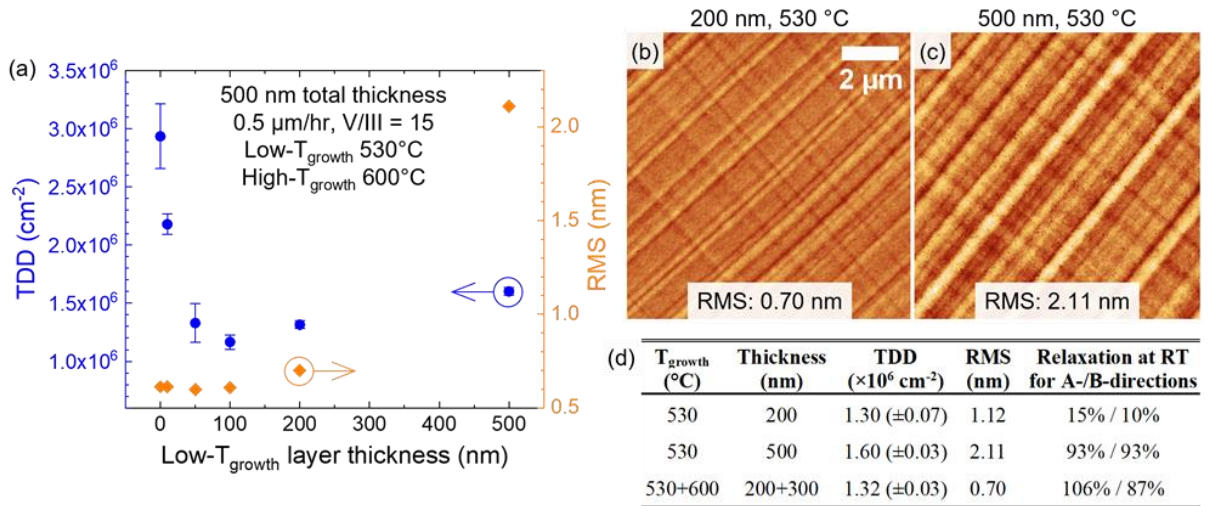
Fig. 4.8: (a) TDD and RMS roughness for relaxed p-GaP on GaP/Si as a function of the low T_{growth} layer thickness. All samples grown to ~500 nm of total MBE GaP thickness. Samples with 0 nm and 500 nm low T_{growth} thickness are single-step growths at 600 °C and 530 °C, respectively. From this work, Ref. [36]. AFM micrographs after 530 °C growth to (b) 200 nm and (c) 500 nm showing intensifying crosshatch morphology with increasing thickness. (d) Table comparing TDD, RMS, and strain relaxation for thin 200 nm 530 °C p-GaP on GaP/Si against single-step 530 °C and two-step (530 °C low T_{growth}, 600 °C high T_{growth}) relaxed p-GaP growths.

displayed the same roughness as the single-step at high T_{growth}. However, for greater low T_{growth} thickness, the TDD and roughness both increased.

In selecting a low T_{growth} layer thickness, a balance must be struck between suppression of dislocation introduction and poor dislocation glide velocity [36]. ~45 nm of MBE growth on the ~45 nm GaP on Si templates reaches the critical thickness for GaP on Si. As the two-step design minimized TDD when the low T_{growth} layer thickness was around 50 – 100 nm, the design was most effective at suppressing dislocation introduction when the low T_{growth} layer extends through the critical thickness. Low dislocation introduction rates from low T_{growth} appear critical for the first 10s of nm of thickness past the critical thickness when dislocation introduction begins. In addition, the low T_{growth} layer likely buries surface inhomogeneities that could activate as dislocation nucleation sources at high T_{growth}; see how the two-step sample with only 10 nm of low T_{growth} also decreased TDD, though to a lesser extent. Simultaneously, it is also important not to use an excessively thick low T_{growth} layer in order to avoid significant relaxation with inferior low T_{growth} glide dynamics.

As compared in Fig. 4.8(b – d), an extra single-step sample of 200 nm at 530 °C was grown for comparison against samples completing growth with either the last 300 nm at 530 °C or at 600 °C. The 200 nm sample was just 10% - 15% relaxed, indicating that most relaxation occurs during the last 300 nm of growth. Though only slightly relaxed, the TDD of this sample was already at $1.30 (\pm 0.07) \times 10^6$ cm^{-2}. While the TDD remained essentially constant for two-step growth (200 nm at 530 °C, 300 nm at 600 °C) at $1.32 (\pm 0.03) \times 10^6$ cm^{-2}, the TDD increased for single-step growth (500 nm at 530 °C) to $1.60 (\pm 0.03) \times 10^6$ cm^{-2}. These results indicate that most dislocation introduction occurs during the first 100 or 200 nm of growth, and that switching to high T_{growth} enables relaxation by glide of existing dislocations. In contrast, continuing at low T_{growth} leads to

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additional dislocation formation due to insufficient glide kinetics during relaxation. Also highlighted in Fig. 4.8(b – d), the crosshatch surface roughness builds up with increasing 530 °C thickness but can be smoothed to the 600 °C surface morphology with two-step growth.

Single-step growth at 660 °C was strongly dominated by dislocation introduction as shown in Fig. 4.9(a) and thus was chosen to further test the ability of two-step growth to suppress dislocation nucleation. As shown in Fig. 4.9(b), two-step growth with a 100 nm layer at 530 °C before 400 nm at 660 °C greatly reduced the TDD by $> 4 \times$ compared to 660 °C single-step growth, confirming the benefits of an initial low T_{growth} step. In fact, TDD comparison by SEI surveys was even more dramatic with $1.1 \, (\pm 0.3) \times 10^7 \, cm^{-2}$ for single-step and $1.6 \, (\pm 0.5) \times 10^6 \, cm^{-2}$ for two-step with 660 °C high T_{growth}. Besides TDD reduction, two-step growth reduced the density of
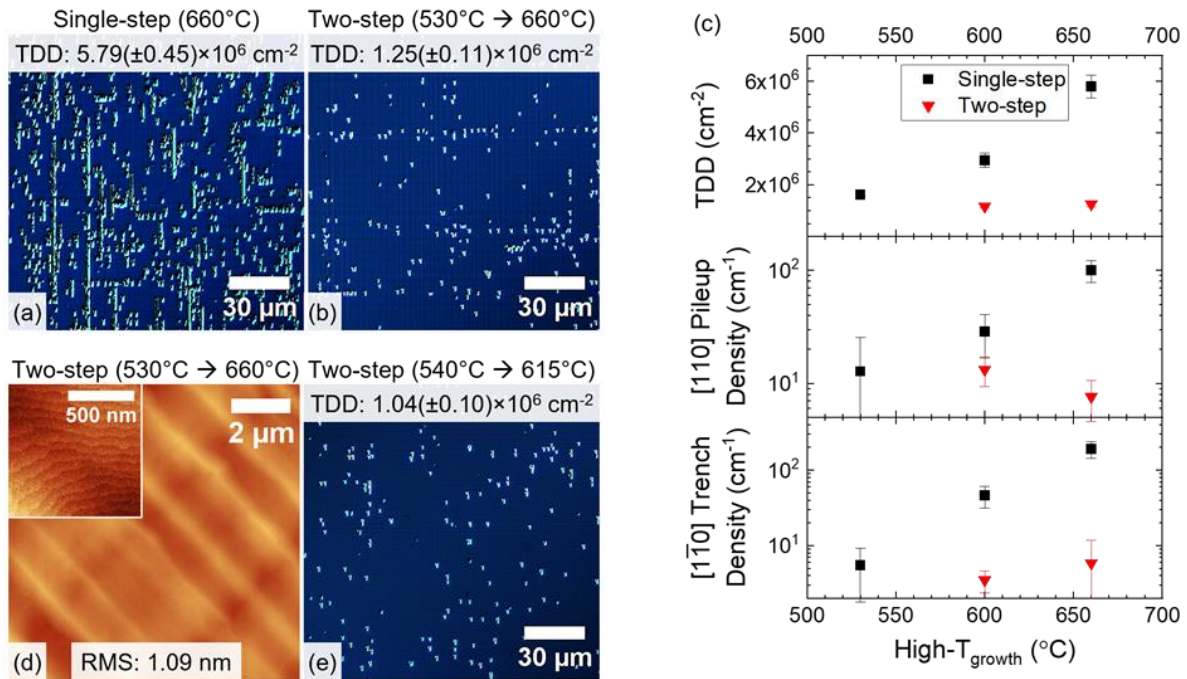
Fig. 4.9: Nomarski micrographs after DSE for relaxed p-GaP grown with 660 °C high T_{growth} by (a) single-step and (b) two-step growth with 530 °C low T_{growth}. (c) Defect densities from the survey of Nomarski micrographs for single and two-step growths with the same high T_{growth}. (d) AFM image of the as-grown surface morphology with 660 °C high T_{growth} (z-range = 17.8 nm). Inset 1 x 1 μm^2 AFM image shows monoatomic steps (z-range = 3.2 nm). (e) Nomarski micrograph after DSE of the lowest TDD achieved by two-step p-GaP growth (540 °C low T_{growth}, 615 °C high T_{growth}). Modified from this work, Ref. [36].

trenches and pileups greatly (Fig. 4.9(c)); the low T_{growth} layer suppressed these dislocation-ridden features by more than an order of magnitude for high T_{growth} of 660 °C.

Similar to observations by Ratcliff *et al.* [106] for GaP homoepitaxy, 660 °C growth led to a step-flow morphology (Fig. 4.9(d) inset), though RMS roughness increased with respect to 600 °C due to an increased cross-hatch amplitude (Fig. 4.9(d)). While the morphology changed markedly by increasing the high T_{growth} from 600 °C to 660 °C, the TDD of the two-step growths saw almost no change, demonstrating a wide growth window. While the optimal T_{growth} for initiating GaP on Si must be low, subsequent growth can be done over a much wider temperature range. This finding could be important for MOVPE, where a T_{growth} of 600 °C – 700 °C is typical.

Additional changes for the two values of T_{growth} enabled relaxed *p*-GaP on Si TDD as low as $1.0 – 1.1 \times 10^6$ cm^{-2}. While I expected decreasing low T_{growth} would reduce TDD due to lower defect introduction rates, decreasing low T_{growth} to lower than 530 °C actually resulted in higher TDD. For 600 °C high T_{growth}, TDD was $1.17\ (\pm0.06) \times 10^6$ cm^{-2}, $1.23\ (\pm0.02) \times 10^6$ cm^{-2}, and $1.52\ (\pm0.10) \times 10^6$ cm^{-2} for 100 nm low T_{growth} of either 530 °C, 505 °C, and 480 °C, respectively. However, increasing both low T_{growth} and high T_{growth} slightly resulted in our lowest GaP on Si TDD of $1.04\ (\pm0.10) \times 10^6$ cm^{-2} by Nomarski survey (Fig. 4.9(e)) and $1.1\ (\pm0.4) \times 10^6$ cm^{-2} by SEI survey. This sample was grown with a 200 nm low T_{growth} layer at 540 °C followed by a 300 nm high T_{growth} layer at 615 °C. I believe that 540 °C may be an improved low T_{growth} condition with improved glide but without a significant increase in dislocation introduction.

Beside samples studying T_{growth} changes, one sample was grown without a growth pause when changing T_{growth} to investigate whether the pause was beneficial, detrimental, or caused no effect. This sample was grown with 50 nm layer at 530 °C low T_{growth}, ~30 nm layer during the T_{growth} change, and ~420 nm layer at 600 °C high T_{growth}. Minimal change in TDD was observed

for the two-step sample without growth pause when compared against two-step samples with growth pause and similar low T_{growth} thickness – 1.26 ($\pm$0.15) $\times$ 10^6 cm^{-2} without growth pause, 1.33 ($\pm$0.17) $\times$ 10^6 cm^{-2} with 50 nm low T_{growth}, and 1.17 ($\pm$0.06) $\times$ 10^6 cm^{-2} with 100 nm low T_{growth}. Given the large unexplored design space for our two-step design including T_{growth} combinations, thicknesses, and growth rate, further optimization could enable relaxed p-GaP TDD below 1×10^6 cm^{-2}. In particular, experiments for $50 - 100$ nm low T_{growth} GaP on GaP/Si could prove helpful for optimizing the suppression of defect introduction.

4.4 Chapter Findings

Primary findings in this chapter are listed below:

- Two morphological defects for relaxed GaP on Si, trenches and dislocation pileups, have very high local threading dislocation density (TDD) on the order of 10^8 cm^{-2}.

- Densities of trenches and dislocation pileups for relaxed p-GaP on Si increased more strongly with growth temperature (T_{growth}) than TDD.

- Two-step growth design for relaxed p-GaP on GaP/Si templates suppressed defect introduction with a thin low T_{growth} layer before changing to a high T_{growth} layer for higher dislocation glide velocity during stain relaxation.

- Optimum low T_{growth} thickness should balance having enough thickness to bury surface inhomogeneities and to grow past the critical thickness for low defect introduction and not having too much thickness with poor dislocation glide velocity.

- Two-step design enabled TDD as low as $1.0 - 1.1 \times 10^6$ cm^{-2} for relaxed p-GaP on Si, the lowest reported TDD for relaxed GaP on Si.

CHAPTER 5

DOPING EFFECTS OF RELAXED GAP ON SI

While our group studied *p*-type relaxed GaP on Si [34], [36] as was used in our group's ~1.7 eV GaAsP single-junction (1J) design, *n*-type buffers are needed for our GaAsP/Si double-junction (2J) design. The *n*-type GaP/Si interface is preferred over the *p*-type interface as the band alignment for the *n*-interface (small conduction band offset and large valence band offset) is more suitable for the Si bottom cell [107]–[110]. With the transition from GaAsP 1J to GaAsP/Si 2J design, Fan and I observed indications that *n*-type $GaAs_yP_{1-y}$/GaP buffers caused increased threading dislocation density (TDD) in the GaAsP top cell – in one case GaAsP TDD on *n*-type buffers was > 2.5 × higher than on *p*-type buffers [55]. Previously, Yonenaga and Sumino demonstrated that *n*-GaAs dislocation glide velocities decrease by orders of magnitude with increased doping concentration [111], however, no studies for GaP with varied doping were performed. In this chapter, I investigated the effects of dopant type, choice, and concentration for relaxed GaP on Si observing TDD strongly depends on doping [65]. While TDD values for unintentionally-doped (UID) and *p*-type Be-doped samples were essentially identical at ~1.1×10^6 cm^{-2}, TDD escalated with increasing *n*-type Si doping to ~3.1×10^7 cm^{-2}, nearly 30 × higher, at doping concentration of ~2×10^{18} cm^{-3}. High *n*-doping also could lead to increased surface roughness, anisotropic strain relaxation, and inhomogeneous TDD distributions from blocking of the dislocation glide. TDD for varied dopant choices of each doping type – *n*-doped (Si, Te, Si+Te), undoped (UID, compensated Si+Be), and *p*-doped (Be, C) – followed the above trends based on electrical activity.[16]

5.1 GaP Doping Effects Background

The previous chapter investigated p-type relaxed GaP on Si for TDD as low as $1.0 - 1.1 \times 10^6$ cm^{-2}, however, I was not aware if this low TDD was transferable to n-type GaP on Si. Recent reports were published during the time of this chapter's work indicating that growing n-type relaxed GaP buffers on Si and the following n-type GaAs$_y$P$_{1-y}$ buffers resulted in high TDD $> 10^7$ cm^{-2} [37], [55]. Boyer et $al.$ observed TDD $> 4 \times 10^7$ cm^{-2} for Si-doped n-GaP with ~$1 - 2 \times 10^{18}$ cm^{-3} doping concentration, though no direct comparison was made against p-type or UID GaP on Si [37]. For ~1.7 eV GaAsP on GaAs$_y$P$_{1-y}$/GaP buffers on Si, Fan and I also found $> 2.5 \times$ higher GaAsP TDD for n-type buffers (Si-doped, ~2×10^{18} cm^{-3}) than on p-type buffers, indicating that the TDD of n-GaP on Si strongly influences the final GaAs$_y$P$_{1-y}$ TDD and requires reduction to continue advancement of GaAsP/Si 2J devices which use n-type buffers.

GaAs$_y$P$_{1-y}$/GaP buffer layers for our n^+-on-p GaAsP 1J design were p-type (~$0.4 - 2 \times 10^{18}$ cm^{-3}) to aid lateral current spreading for double-top contact fabrication on n-GaP/Si templates or conduct holes for top-bottom contact fabrication on p-GaP substrates. Conversely, our GaAsP/Si 2J design utilizes n-type buffers to conduct electrons from the n^+-on-p Si bottom junction to the p^+-on-n^+ ~1.7 eV GaAsP-based tunnel junction. Either switching to a GaP-based tunnel junction or flipping polarity of all junctions would allow p-type buffers for a GaAsP/Si 2J. However, this tunnel junction would likely perform poorly due to lower tunneling probability with higher bandgap and the increased thermal load from buffer growth. Flipping junction polarity would require management of shorter minority hole diffusion lengths as well as worse band alignment for the p-GaP/p-Si interface.

Though literature has not agreed on values for conduction and valence band offsets, most reports indicate n-type GaP/Si interface is more beneficial than the p-type interface for the Si

bottom junction [107]–[110]. Most commonly, authors observe the GaP/Si band alignment as a straddling gap with small conduction band offset and large valence band offset. For an *n*-GaP on *n*-Si interface, this band alignment aids the n^+-on-*p* Si bottom junction with lower interface resistance for majority electrons due to a small barrier into the *n*-GaP conduction band and improved minority hole blocking due to a larger barrier into the *p*-GaP valence band. Note, other authors observed reports with larger conduction band offset than valence band offset and suggested that growth initiation sequence and interface polarity may alter band alignment for the GaP/Si interface [112], [113]. Even so, Feifel *et al.* showed Si solar cells with *n*-GaP frontside passivation exhibiting $V_{OC} > 0.63$ V [114], promising for III-V/Si solar cells with n^+-on-*p* subcells.

In addition to high TDD, Boyer observed anisotropic strain relaxation in *n*-GaP on Si, signifying very slow β-dislocation glide velocity [37]. In contrast, Nay Yaung and I observed essentially isotropic strain relaxation in *p*-GaP on Si despite the anisotropic glide velocities [34], [36]; Yonenaga found that β-dislocations were ~20 – 30 × slower than α-dislocations in GaP (Fig. 5.1(a)) [104]. Additionally, dislocation glide velocities in GaP are more than two orders of magnitude slower than other III-V semiconductors such as GaAs, InP, and InAs (Fig. 5.1(a); see Fig. 4.1(a) for comparison also against InP and InAs). While not studied for GaP, Yonenaga and
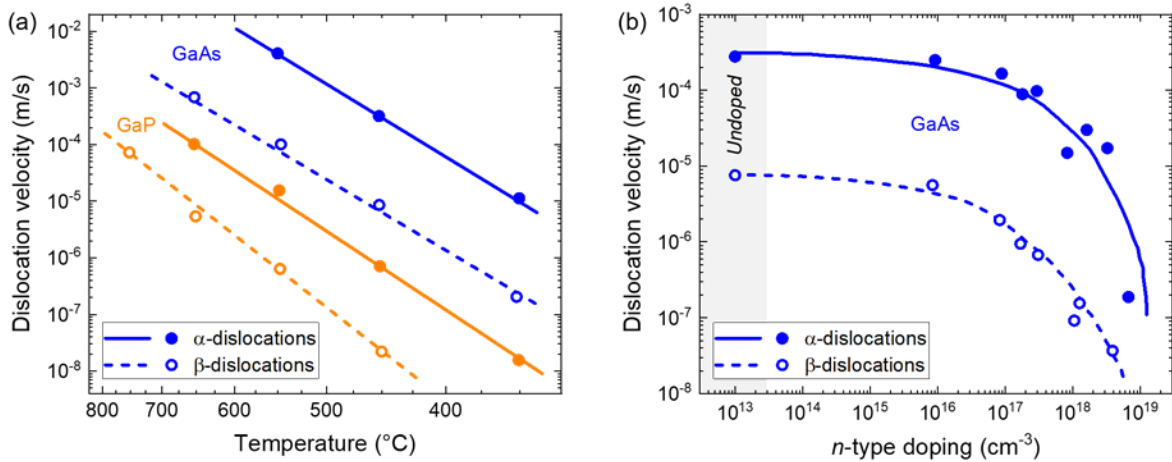
Fig. 5.1: (a) Arrhenius plot of α- and β-dislocation glide velocities for GaP and GaAs. (b) α- and β-dislocation glide velocities for GaAs as a function of *n*-type doping. Both adapted from Ref. [104].

Sumino demonstrated that *n*-GaAs dislocation glide velocities decrease by orders of magnitude with increased doping concentration (Fig. 5.1(b)) [104], [111]. If similar behavior occurs in GaP, then *n*-GaP could suffer from largely-decreased dislocation velocities, which are low to begin with.

However, literature had not investigated dislocation dynamics in GaP as a function of doping, and doping/impurity effects are more complicated than shown in Fig. 5.1(b). For GaAs, isovalent impurities caused no change, *n*-type dopants strongly decreased all dislocation velocities, while *p*-type dopants decreased α-dislocation velocity but increased β-dislocation velocity [104], [111]. Alternatively for InP the effects were swapped between dopant types, instead with *p*-type dopants strongly decreasing all dislocation velocities and *n*-type dopants increased α-dislocation (decreased β-dislocation) velocity [104], [115]. Yonenaga suggested that the influence of doping on dislocations may result from electronic effects, such as the Fermi level or free electron concentration influencing the dislocation kink formation energy, and/or from solute effects, such as dopant atom clusters or complexes retarding dislocation motion with a local drag force [104], [116]. High TDD and anisotropic strain relaxation from slow β-dislocation glide velocity as observed by Boyer *et al.* [37] may indicate the dislocation behavior of GaP more closely resembles that of GaAs than InP.

5.2   Investigation of Be-doped, Undoped, and Si-doped GaP

Similar to last chapter, two-step GaP samples were co-grown by molecular beam epitaxy (MBE) on high-quality GaP/Si templates (NAsP$_{III/V}$ GmbH, Germany) after dilute *aqua regia* precleaning and on undoped GaP substrates (ITME, Poland). Two-step GaP samples were grown at 0.5 μm/hr and V/III of 15 with a 100 nm low growth temperature (T$_{growth}$) layer at 530 °C – 535 °C prior to a 400 nm high T$_{growth}$ layer at 600 °C – 615 °C (see Fig. 4.7(a) for layer and template structure).

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Type	Dopant(s)	Nominal Doping (cm^{-3})	Conductivity (S/m)	RMS (nm)	Relaxation at RT for A-/B-directions	TDD ($\times 10^6$ cm^{-2})
n-doped	Si	2×10^{18}	1667	0.98	92% / 64%	31 (±4)
		4×10^{17}	504	0.66	82% / 43%	4.12 (±0.50)
		5×10^{16}	0*	0.71	98% / 88%	2.94 (±0.18)
	Te	2×10^{18}	328	1.29	108% / 71%	2.51 (±0.39)
	Si+Te	2×10^{18} each	1887	1.57	136% / 33%	42 (±5)
"Undoped"	UID	None	0*	0.76	101% / 97%	1.15 (±0.11)
	Si+Be	4×10^{17} each	0*	1.01	—	1.34 (±0.17)
p-doped	Be	2×10^{18}	1402	0.69	102% / 80%	1.11 (±0.11)
		4×10^{17}	394	0.61	87% / 106%	1.17 (±0.06)
	C	3×10^{18}	2899	0.79	—	1.89 (±0.34)

Table 5.1: List of two-step GaP samples on GaP/Si sorted by dopant choice(s) and doping concentration as well as measured conductivity, RMS surface roughness, strain relaxation for the A/B-directions at room temperature (RT), and TDD. 0* indicates the sample was too resistive for our measurement system, so no conductivity was recorded. Relaxation for the samples doped with Si+Be or C have not been measured. Adapted from this work, Ref. [65].

Table 5.1 details the samples grown with varied dopant choices and doping concentrations; dopant sources used in this work included elemental effusion cells for Si and Be, a GaTe effusion cell for Te, and a CBr$_4$ gas source for C. I discuss the common MBE doping choices (Si, UID, and Be) in this section and less common or unconventional doping choices (Te, co-doped Si+Te, co-doped Si+Be, and C) in the following section, Chapter 5.3. Nominal doping was determined from Hall measurements of GaAs doping calibrations. Hall measurements of GaP were unreliable due to non-ohmic contacts since a contact layer such as heavily-doped GaAs would complicate GaP morphology and defect selective etching (DSE). Conductivity was measured for samples grown on undoped GaP substrates by the van der Pauw method.[17] As-grown surface morphology was inspected by atomic force microscopy (AFM) with root mean square (RMS) roughness reported from 10×10 μm^2 images. GaP room temperature (RT) strain relaxation on Si was determined from high-resolution x-ray diffraction (XRD) reciprocal space mapping with maps measured in

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[17] Some samples with low doping concentration were too resistive for our measurement system, so these samples lack conductivity results.

both symmetric and asymmetric geometries for both the A/B-directions. The A/B-direction is measured with the x-ray beam incident in the $(1\bar{1}0)/(110)$ plane with projection in $[110]/[1\bar{1}0]$, sampling relaxation by α/β-dislocations that glide in $[1\bar{1}0]/[110]$ on the A (group III)/B (group V) slip planes. More details on the geometry can be found in Appendix A. The TDD was estimated by hot phosphoric acid DSE at ~130 °C – 140 °C in combination with microscopy surveys to count the etch pit density. DSE was performed for either ~5 min or ~2 min to tune the etch pit size for Nomarski microscopy or scanning electron microscopy (SEM) and to survey low- or high-TDD samples, respectively.

Direct comparison between $\sim 2 \times 10^{18}$ cm^{-3} Be-doped (*p*-type) and Si-doped (*n*-type) two-step GaP on Si confirms that Si doping leads to a much higher TDD, in this case $> 27 \times$ (Fig. 5.2) [65]. In contrast, the TDD of homoepitaxial GaP on GaP was not affected by doping. Additionally, I observed anisotropic strain relaxation for this Si-doped GaP with 92%/64% for the A/B-directions at RT, similar to Boyer *et al.* who grew *n*-GaP by MOVPE on a 2° offcut Si substrate [37]. The high TDD and anisotropic relaxation of *n*-GaP on Si appears to be unaffected by the growth technique or substrate offcut. Other *n*-type samples in this work, aside from the $\sim 5 \times 10^{16}$ cm^{-3} Si-doped sample, also exhibited anisotropic strain relaxation with more relaxation in the A-direction (see Table 5.1), likely resulting from the slower glide of β-dislocations compared to α-
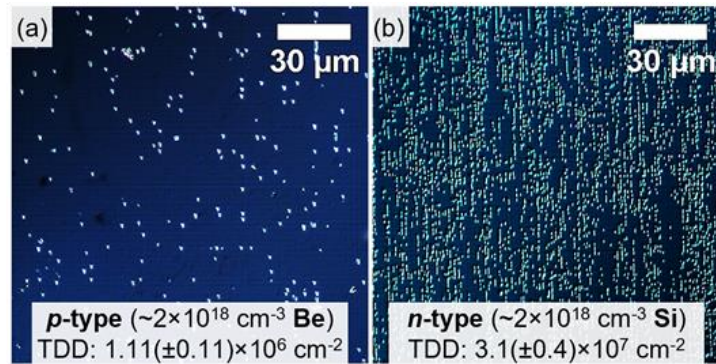
Fig. 5.2: Comparison of Nomarski micrographs after DSE of two-step GaP on GaP/Si with (a) Be doping (*p*-type) and (b) Si doping (*n*-type) of $\sim 2 \times 10^{18}$ cm^{-3}. The high TDD of (b) needed to be counted by SEM imaging. From this work, Ref. [65].

dislocations (Fig. 5.1). I found more isotropic strain relaxation for Be-doped and UID samples, with relaxation at RT for the A/B-directions of 102%/80% and 87%/106% for $\sim 2 \times 10^{18}$ cm^{-3} and $\sim 4 \times 10^{17}$ cm^{-3} Be-doped samples, respectively, and 101%/97% for the UID sample. It is unclear why the $\sim 4 \times 10^{17}$ cm^{-3} Be-doped sample had higher strain relaxation in the B-direction, especially considering that previously measured GaP on GaP/Si samples with $\sim 4 \times 10^{17}$ cm^{-3} Be doping showed isotropic strain relaxation [36].

I estimated the ratio of average misfit dislocation length for two samples by assuming that misfit dislocations are the only significant contributor to strain relaxation and that all dislocations result from the half-loop geometry giving a misfit dislocation at the GaP/Si interface terminated at both ends by a threading dislocation exiting the GaP surface. With these assumptions, the average strain relaxation of the A- and B-directions is proportional to the number of misfit dislocations; so the average misfit dislocation length is proportional to the average strain relaxation divided by the TDD. Therefore, the average misfit dislocation length is estimated to be $> 32 \times$ higher in UID or in Be-doped GaP than in Si-doped GaP with $\sim 2 \times 10^{18}$ cm^{-3} doping using our two-step GaP growth conditions, indicative of much slower glide velocities in *n*-type GaP [65].

Fig. 5.3 shows that GaP on Si TDD does not change for UID and Be doping but escalates with increasing Si doping concentration [65]. Thus, one strategy to reduce the TDD of *n*-GaP on Si is to decrease Si doping: TDD reduced from 3.1 (± 0.4) $\times 10^7$ cm^{-2} to 4.12 (± 0.50) $\times 10^6$ cm^{-2} to 2.94 (± 0.18) $\times 10^6$ cm^{-2} for Si doping lowered from $\sim 2 \times 10^{18}$ cm^{-3} to $\sim 4 \times 10^{17}$ cm^{-3} to $\sim 5 \times 10^{16}$ cm^{-3}, respectively. While promising for reduced *n*-GaP TDD, lowering *n*-doping may be harmful to III-V/Si multi-junction solar cells due to possible increased series resistance decreasing fill factor. A test of $\sim 5 \times 10^{16}$ cm^{-3} Si-doped GaAs$_y$P$_{1-y}$/GaP buffers indicated this doping was too low
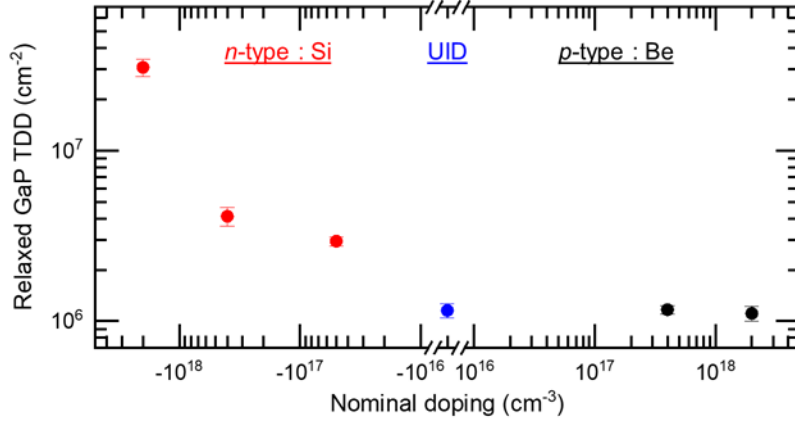
Fig. 5.3: Dependence of relaxed two-step GaP TDD on nominal doping for Si-doped, UID, and Be-doped samples. From this work, Ref. [65].

for GaAsP/Si 2J cells, however, a moderate Si doping of ~4×10^{17} cm^{-3} was sufficient to prevent resistance losses for Fan and my 2J device results [117].

5.3   Investigation of Additional Dopant Choices

Each report observing TDD escalation with *n*-type doping utilized Si as the dopant [37], [55], [65]. If the solute properties of Si as an impurity rather than the electronic effects of Si as a donor more strongly influence the dislocation dynamics for GaP, then substituting another donor species might enable lower *n*-GaP on Si TDD. In addition, high Si doping led to rougher surface morphology in comparison to Be-doped or UID GaP on Si (Fig. 5.4 and previously in Table 5.1). Changing from ~2×10^{18} cm^{-3} Be (Fig. 5.4(a)) to Si (Fig. 5.4(b)) increased RMS roughness by ~40%; increased height variation along the [110] direction primarily caused the rougher morphology (Fig. 5.4(e, f, i, j)). Since Te has been demonstrated as a surfactant that can modify surface kinetics during growth due to an accumulated Te surface layer and often can smoothen surface morphology in a variety of III-V materials [118]–[122], I tested Te as an alternate donor and as a surfactant [65]. Samples grown included one with nominal doping of ~2×10^{18} cm^{-3} Te by itself (Fig. 5.4(c)) and one sample co-doped with Si and Te (Si+Te, ~2×10^{18} cm^{-3} nominal doping of each, Fig. 5.4(d)).
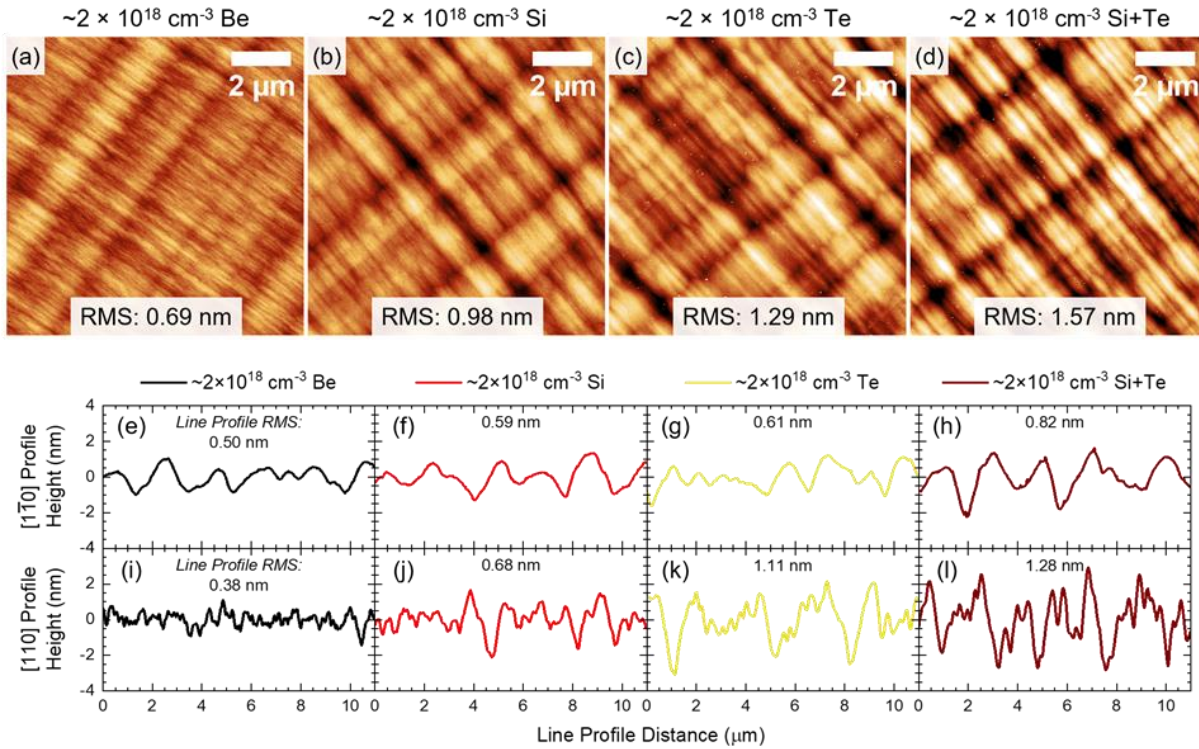
Fig. 5.4: (a – d) AFM images of as-grown surface morphology (z-range = 6.8 nm) for two-step GaP on GaP/Si samples and AFM line profiles in the (e – h) [1$\bar{1}$0] and (i – l) [110] directions for each AFM image. Comparison of samples with ~2 × 10^{18} cm^{-3} nominal doping for each dopant choice: (a, e, i) Be doping, (b, f, j) Si doping, (c, g, k) Te doping, (d, h, l) both Si and Te doping. The [110] direction goes from roughly bottom left to top right of images. RMS roughness increased more strongly in [110] than in [1$\bar{1}$0] when changing from Be doping to Si or Te doping. Adapted from this work, Ref. [65].

While Te had poor incorporation as expected for a surfactant (discussed in more detail later in section), the surface morphology was adversely affected by the likely Te surface layer leading to increased crosshatch amplitude. Te by itself had higher RMS roughness than Si with ~2 × 10^{18} cm^{-3} nominal doping, and when both *n*-type dopants were combined in the Si+Te sample, the RMS roughness increased further. AFM of co-grown GaP homoepitaxy samples (Fig. 5.5) also demonstrated modified surface morphology with "islands" appearing to merge with those adjacent in the [110] direction (Fig. 5.5(c, d)). While this visually appears to "smooth" the island morphology as expected for a surfactant, the RMS roughness was unaffected. In addition, swapping between Be and Si doping did not change the morphology or RMS roughness for GaP homoepitaxy samples (Fig. 5.5(a, b)). Taken together, comparisons of TDD and RMS data for GaP
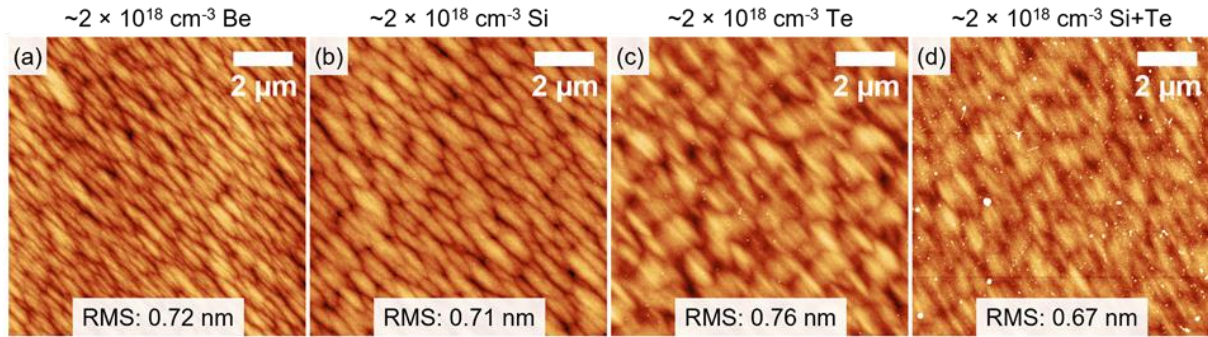
Fig. 5.5: AFM images of as-grown surface morphology (z-range = 6.8 nm) for two-step GaP homoepitaxy samples with ~2×10^{18} cm^{-3} nominal doping for each dopant choice: (a) Be doping, (b) Si doping, (c) Te doping, (d) both Si and Te doping. The [110] direction goes from roughly bottom left to top right of images. Note white spots in (d) were from sample handling after growth and were masked out of the RMS calculation.

grown on GaP/Si templates (Table 5.1) or on GaP substrates suggest the existence of complicated interactions between dopant choice, adatom mobility, strain, TDD, and surface morphology.

The GaP on Si sample with the highest *n*-type doping, the Si+Te sample, provided the most extreme example of anisotropic strain relaxation with 136%/33% for the A/B-directions at RT (105%/25% at high T_{growth}) [123], indicating that *n*-doping can increase the discrepancy between α- and β-dislocation glide velocities [65]. In addition, this sample demonstrated inhomogenous TDD distribuitons, examples shown in Fig. 5.6, which appear to result from dislocation blocking and other dislocation interactions. Nomarski microscopy of samples after DSE aided the identification of local TDD variations due to the ease of rapidly imaging large areas of the order of several mm^2. Inhomogeneous TDD was common for highly *n*-doped GaP on Si, with most areas having high TDD (high-TDD "matrix"), and some local regions having an order of magnitude lower TDD (low-TDD "pockets"). Following this work [65], Boyer also observed similar TDD distributions for relaxed *n*-GaP on Si [86].

I hypothesize that low-TDD pockets arise from the blocking of α-dislocation glide by dislocation pileups, resulting in regions between parallel dislocation pileups with low TDD and less relaxation [65]. Pockets were consistently located between parallel dislocation pielups; see
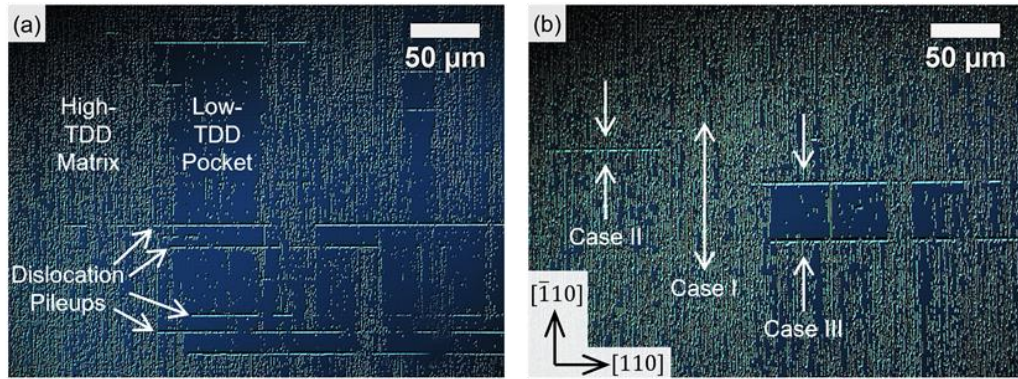
Fig. 5.6: Nomarski micrographs after DSE demonstrating inhomogeneous TDD distribution in highly *n*-doped two-step GaP on GaP/Si (a) showing a complex network of low-TDD pockets in a high-TDD matrix and (b) illustrating representative cases for blocking of dislocations gliding in [1$\bar{1}$0]. Case I – No pileups are encountered so dislocations glide unhindered. Case II – A single pileup likely blocks dislocations on either side but no inhomogeneity in TDD is observed. Case III – Two parallel pileups block dislocations approaching from either direction forming a low-TDD pocket in between the pileups. Adapted from this work, Ref. [65].

Fig. 5.6 for examples. As shown in Chapter 4.2, dislocation pileups consist of tightly-spaced threading dislocations making a line along [110]. Due to the high local density of similar dislocations and the accompanying strain fields, pileups may block orthogonally approaching dislocations [124]. Fig. 5.6(b) illustrates three potential scenarios for α-dislocations gliding in [1$\bar{1}$0] depending on the number of parallel dislocation pilues encountered. α-dislocations are either free to glide when encountering no pileups (case I), blocked by a single pileup causing no significant TDD inhomogeneity (case II), or blocked from entering the low-TDD pocket by a pair of parallel pileups (case III).

To support this hypothesis, I tested local strain with polarized micro-Raman spectra comparing locations within the high-TDD matrix and within low-TDD pockets (Fig. 5.7) [65]. GaP on Si samples with roughly isotropic strain relaxation were also compared to set expectations for the transverse optical (TO) peak shift with GaP relaxation on Si; these samples included a relaxed and a strained sample with 101%/97% and 15%/10% relaxation, respectively, for the A/B-directions at RT. Biaxial compressive strain blue-shifted the TO peak to higher Raman shift, while
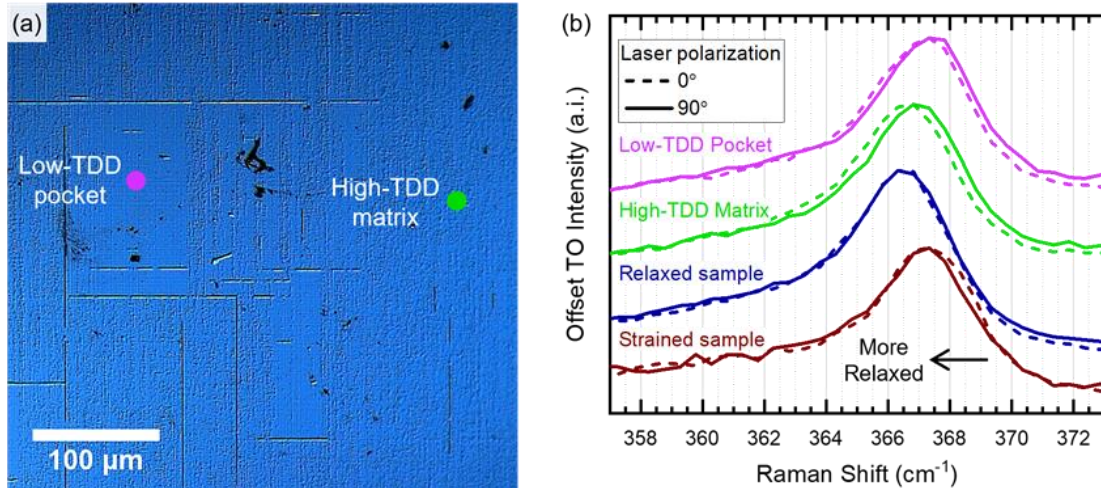
Fig. 5.7: Polarized micro-Raman testing of highly *n*-doped two-step GaP on GaP/Si sample. (a) Nomarski micrograph after DSE for ~2 min (for small etch pits) of Si+Te sample used for micro-Raman testing. Light purple and light green circles represent approximate locations of point-and-shoot Raman spectra for a low-TDD pocket and the high-TDD matrix. (b) Comparison of Raman spectra obtained with a 532 nm laser for locations in (a) against samples with roughly isotropic strain relaxation. Adapted from this work, Ref. [65].

fully relaxing this strain red-shifted the TO peak to ~366.3 – 366.8 cm^{-1} giving a peak shift rate of about –0.3 to –0.4 cm^{-1}/%-strain similar to Ref. [125].[18] Relaxed and stained samples do not show a difference with respect to laser polarization due to nearly isotropic strain relaxation. While anisotropic strain was observed in the high-TDD matrix with slight peak separation with polarization, the observed separation was smaller than expected from XRD measurements of 136%/33% relaxation for A/B-directions at RT. Fig. 5.7(b) shows higher strain within the low-TDD pocket than within the high-TDD matrix for both orthogonal laser polarization directions, consistent with expectations of lower strain relaxation due to dislocation blocking. Similar results were observed in various alternate pockets and matrix regions. The existence of low-TDD, poorly-relaxed pockets with areas of > 1000 μm^2 also shows that dislocation nucleation does not occur uniformly over the sample. While dislocation blocking may occur in UID and *p*-type GaP, low-

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[18] The micro-Raman setup utilized had a limited data step size of ~0.5 cm^{-1} around the GaP TO peak so reported peak value and shift rate lack precision.
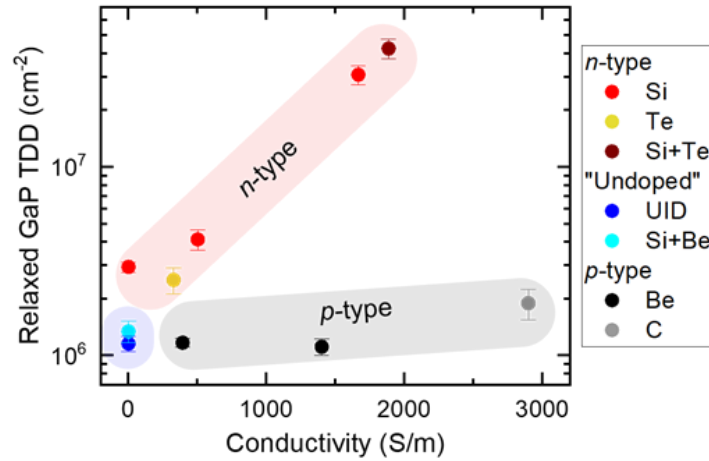
Fig. 5.8: Relaxed two-step GaP TDD vs conductivity of samples with varied doping concentrations and dopants. Undoped, *n*-doped, and *p*-doped sample trends are highlighted. Samples at 0 S/m were too resistive for our measurement system. TDD escalates with increased *n*-type doping. TDD escalates with increased *n*-type doping. Adapted from this work, Ref. [65].

TDD pockets are not observable due to reduced dislocation interactions and improved β-dislocation glide.

Fig. 5.8 shows the TDD of relaxed GaP on Si as a function of conductivity for samples with varied doping concentrations and dopant choice(s) (measured values are in Table 5.1 at the start of Chapter 5.2) [65]. Both samples using Te, nominal doping of $\sim 2 \times 10^{18}$ cm^{-3} Te or Si+Te, led to elevated TDD in comparison to UID and Be-doped samples. While the TDD of 2.51 ($\pm$0.39) $\times 10^6$ cm^{-2} for the Te-doped sample was lower than the Si-doped samples, I suspect that the large size discrepancy between P and Te led to minimal incorporation giving low *n*-type doping concentration and, therefore, lower TDD. I estimate that $\sim$10% of the $\sim 2 \times 10^{18}$ cm^{-3} nominal doping is present and activated in the bulk based on the low conductivity for the Te-doped sample and the small conductivity difference between the Si+Te sample and the $\sim 2 \times 10^{18}$ cm^{-3} Si-doped sample. Capacitance-voltage measurements were unable to obtain reliable Te dopant profiles; further study of Te dopant incorporation and activation is warranted. TDD of *n*-type samples with Si, Te, and Si+Te doping all followed the TDD escalation trend vs conductivity.

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Conversely, C as an alternative *p*-type dopant led to a slight increase in TDD compared to UID and Be-doped samples [65]. The increased TDD to 1.89 ($\pm$0.34) $\times$ 10^6 cm^{-2} for a nominal doping of ~3 $\times$ 10^{18} cm^{-3} C was small in comparison to *n*-type dopants even with low doping. Conductivity for the C-doped sample was ~2 $\times$ that for the Be-doped sample with ~2 $\times$ 10^{18} cm^{-3} nominal doping, suggesting > 3 $\times$ 10^{18} cm^{-3} C doping and therefore higher incorporation or activation in GaP than in GaAs when using CBr$_4$. Interestingly, this C doping modified the morphology of GaP homoepitaxy (Fig. 5.9(f)) to give much lower RMS roughness, but did not significantly alter the morphology on GaP/Si templates (Fig. 5.9(c)).

As a key last dopant test, I grew a fully compensated sample co-doped with Si and Be (Si+Be, ~4 $\times$ 10^{17} cm^{-3} of each) to have Si present as a solute in the sample while preventing the Fermi level from moving toward the conduction band edge [65]. If Si solute effects are the dominant reason for TDD escalation, then one would expect high TDD, like that found for the sample only doped with ~4 $\times$ 10^{17} cm^{-3} Si. Alternatively, if electronic effects from active *n*-dopants
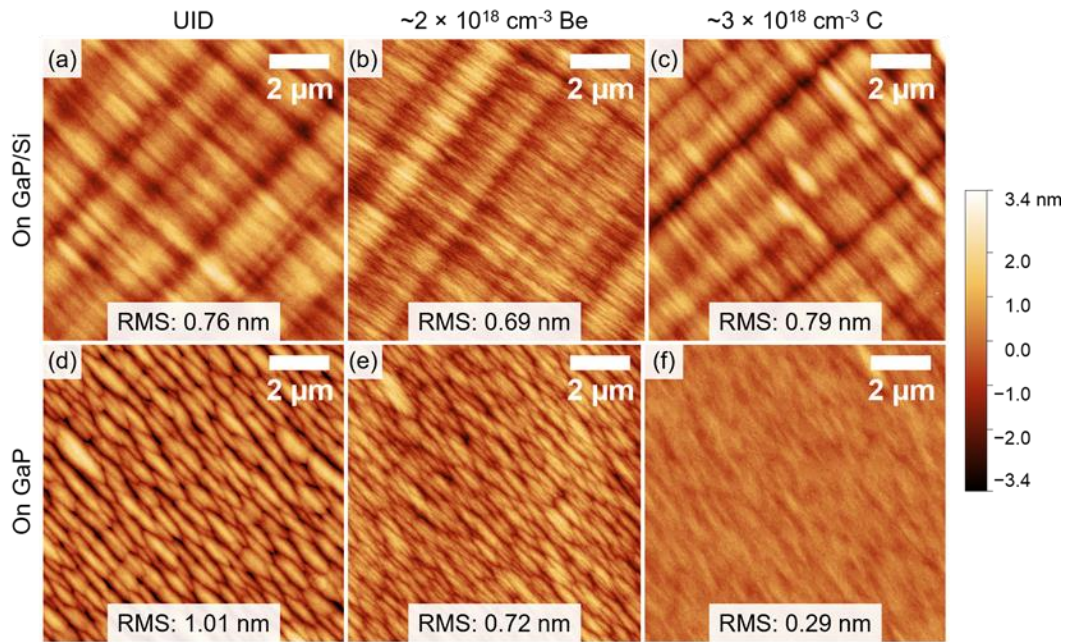
Fig. 5.9: AFM images of as-grown surface morphology (z-range = 6.8 nm) for two-step GaP (a – c) on GaP/Si or (d – f) on GaP with doping of either (a, d) UID, (b, e) ~2 $\times$ 10^{18} cm^{-3} Be, or (c, f) ~3 $\times$ 10^{18} cm^{-3} C. The [110] direction goes from roughly bottom left to top right of images.

are the dominant reason, then one would expect a similar TDD to the UID sample. Nominal doping of $\sim 4 \times 10^{17}$ cm^{-3} was chosen to lessen the impact of an imbalance in actual doping from Si and Be; higher doping would cause a larger remainder of uncompensated dopants. As shown in Fig. 5.8, TDD for the Si+Be sample was 1.34 (± 0.17) $\times 10^6$ cm^{-2}, only slightly higher than the UID sample, confirming that electronic effects dominate. Taken together, the experiments in this section suggest that increased free electron concentration plays a primary role in TDD escalation with increased *n*-type doping. I speculate that a change in the free electron concentration could modify activation energies for dislocation kink formation and/or for dislocation introduction, as proposed in prior literature [104], [116], [124], [126]. Future work could investigate whether solute effects become significant at higher doping concentrations (e.g., $10^{19} - 10^{20}$ cm^{-3}) or if electronic effects still dominate.

5.4   Chapter Findings

Primary findings in this chapter are listed below:

- Unintentionally-doped (UID) and *p*-type Be-doped relaxed GaP on Si samples have essentially identical threading dislocation density (TDD) of $\sim 1.1 \times 10^6$ cm^{-2}.

- Increasing *n*-type Si doping concentration results in escalating TDD, with $\sim 3.1 \times 10^7$ cm^{-2} TDD, nearly 30 $\times$ higher than UID or Be-doped samples, for $\sim 2 \times 10^{18}$ cm^{-3} Si.

- Anisotropic strain relaxation common for *n*-doped GaP on Si with B-direction not fully relaxed, indicating poor dislocation glide velocities in particular for β-dislocations.

- Te dopants poorly incorporated in GaP as expected for a surfactant, but surface roughness did not change for GaP on GaP and worsened for GaP on Si.

- High n-doping can lead to inhomogeneous TDD and strain distributions with low-TDD pockets in a high-TDD matrix due to the blocking of α-dislocation glide by dislocation pileups.

- TDD for varied dopant choices of each doping type – n-doped (Si, Te, Si+Te), undoped (UID, compensated Si+Be), and p-doped (Be, C) – followed the above trends based on electrical activity.

CHAPTER 6

STRATEGIES FOR TDD REDUCTION OF *N*-GAP ON SI

The previous chapter discussed investigation of doping trends for relaxed GaP on Si and correlated these trends with electrical activity. However, the escalation of threading dislocation density (TDD) with increasing *n*-doping concentration is problematic for our GaAsP/Si double-junction (2J) that requires *n*-type metamorphic buffer layers. While lowering *n*-type doping from ~2×10^{18} cm^{-3} to ~5×10^{16} cm^{-3} Si decreased *n*-GaP TDD by an order of magnitude from 3.1 (±0.4) $\times 10^7$ cm^{-2} to 2.94 (±0.18) $\times 10^6$ cm^{-2}, respectively [65], the reduction in buffer conductivity would harm GaAsP/Si 2J performance. Additional strategies are needed to narrow the TDD discrepancy between *n*-doped and unintentionally-doped (UID) or *p*-doped buffers. Boyer *et al.* showed growth of a compressively strained superlattice (CSS) of alternating GaAs$_{0.17}$P$_{0.83}$ and GaP layers directly on GaP/Si templates enabled relaxed *n*-GaP TDD as low as 2.4 (±0.4) $\times 10^6$ cm^{-2} with $1 - 2 \times 10^{18}$ cm^{-3} Si doping [37]. Boyer hypothesized the CSS structure combated poor dislocation dynamics in *n*-GaP by adding excess stress, enhancing dislocation glide velocities to lower dislocation nucleation rates [37], [86]. In this chapter, I incorporated a CSS structure for molecular beam epitaxy (MBE) growth of relaxed *n*-GaP on Si and also observed TDD reduction. Combining Boyer's CSS design with my two-step design and lowering *n*-doping to ~4×10^{17} cm^{-3} resulted in a TDD of 1.54 (±0.20) $\times 10^6$ cm^{-2} [65]. Later in this chapter, I describe the effect of the improved *n*-doped GaAs$_y$P$_{1-y}$/GaP buffers on the performance of ~1.7 eV GaAsP single-junction (1J) solar cells, showing similar device performance and TDD to devices on UID buffers [127].[19]

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[19] Parts of this chapter are reproduced from [R. D. Hool *et al.*, "Challenges of relaxed n-type GaP on Si and strategies to enable low threading dislocation density," *J. Appl. Phys.*, vol. 130, no. 24, p. 243104, Dec. 2021, doi: 10.1063/5.0073525.], with the permission of AIP Publishing, and from [R. D. Hool *et al.*, "Reducing the dependence of threading dislocation density on doping for GaAsP/GaP on Si," in *2021 48th IEEE Photovoltaic Specialists Conference (PVSC)*, Jun. 2021, pp. 0666–0668. doi: 10.1109/PVSC43889.2021.9519041.], with permission © 2021 IEEE.

6.1   Compressively Strained Superlattice (CSS) Background

Authors most commonly employ strained layer superlattice (SLS) structures, consisting of alternating compressive/tensile-strained interfaces, for reduction of TDD for GaAs on Si already with high TDD and often with thermal cycle annealing [128]–[130]. SLS's can increase dislocation movement to promote annihilation reactions among closely-spaced dislocations [131], however, SLSs are less effective at TDD reduction with lower pre-existing TDD ($\sim 1 \times 10^7$ cm^{-2}) due to the larger average distance between dislocations [132], [133]. Alternatively for low-TDD GaAs on GaAs, SLS's have been utilized to enhance dislocation glide such that threading dislocations would exit the substrate via the wafer edge [134], [135].

Inspired by SLS structures used for dislocation filtering or enhancing dislocation glide, Boyer *et al.* designed a compressively strained superlattice (CSS) of GaAs$_{0.17}$P$_{0.83}$ and GaP for use in relaxed *n*-GaP on Si [37], [86]. Boyer hypothesized that placing a CSS around the critical thickness, as opposed to after relaxation for traditional dislocation filtering SLSs, might improve the initial relaxation process [37]. The CSS design is intended to utilize the newly-formed dislocation loops for strain relief more efficiently by increasing the effective stress. This is expected to enhance dislocation glide velocities thus resulting in longer misfit segments and a lower number of new dislocation loops required for strain relaxation [37]. While Boyer did not find a significant change in relaxation amount, Boyer observed strong TDD reduction for relaxed *n*-GaP on Si when including a CSS structure, indicating the average misfit dislocation length was around an order of magnitude longer with a CSS. In addition, no evidence of dislocation filtering was observed as TDD increased monotonically with thickness even for *n*-GaP with CSS [37].

Boyer's GaP with CSS samples consisted of alternating layers of 10 nm *n*-GaAs$_{0.17}$P$_{0.83}$ and 10 *n*-GaP (20 nm for single period; $1 - 2 \times 10^{18}$ cm^{-3} Si doping) grown directly on GaP/Si

templates and followed by *n*-GaP overgrowth for a total of 500 nm of III-V on Si.[20] Samples with 1-period, 3-period, and 5-period CSS structures grown on 50 nm GaP/Si templates were compared against a sample without CSS. TDD decreased for all samples with CSS, from 4.4 ($\pm$0.4) $\times$ 10^7 cm^{-2} without CSS to 4.6 ($\pm$0.4) $\times$ 10^6 cm^{-2}, 2.4 ($\pm$0.4) $\times$ 10^6 cm^{-2}, and 6.0 ($\pm$3.0) $\times$ 10^6 cm^{-2} for 1-period, 3-period, and 5-period samples, respectively [37]. CSS effectiveness improved with increasing period count for the 1-period to 3-period sample, but the 5-period case was less effective due to increased dislocation pileup density. This 3-period CSS structure resulted in the lowest-reported *n*-GaP on Si TDD by Boyer's experiments, a reduction by a factor of nearly 20 from bulk samples [86].

Boyer also investigated the effect of the CSS distance from the GaP/Si interface by growing the 3-period CSS structure directly on 30 – 90 nm GaP/Si templates [86]. CSS placement closer to the GaP/Si interface, 30 nm and 40 nm, resulted in unchanged to slightly increased TDD, while CSS placement further from the interface, 70 nm and 90 nm, led to elevated TDD though still a factor of 5 lower TDD than without a CSS. Boyer posited that CSS may be most effective when placed to span the region where dislocation introduction spikes (~80 – 100 nm from GaP/Si interface) [86].

6.2   Implementation of CSS in MBE

In this section, I detail the implementation of CSS structures in MBE growth for GaP on GaP/Si templates. Similar to the last two chapters, samples were grown on commercial ~45 nm GaP/Si templates (NAsP$_{III/V}$ GmbH, Germany) after dilute *aqua regia* precleaning, so the closest CSS placement to the GaP/Si interface was 45 nm. MBE GaP layers were grown at 0.5 µm/hr and

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[20] Note in comparison, the growth thickness specified for my works and Nay Yaung's works does not include the template thickness, so a 500 nm GaP layer on GaP/Si template has ~545 nm III-V on Si.
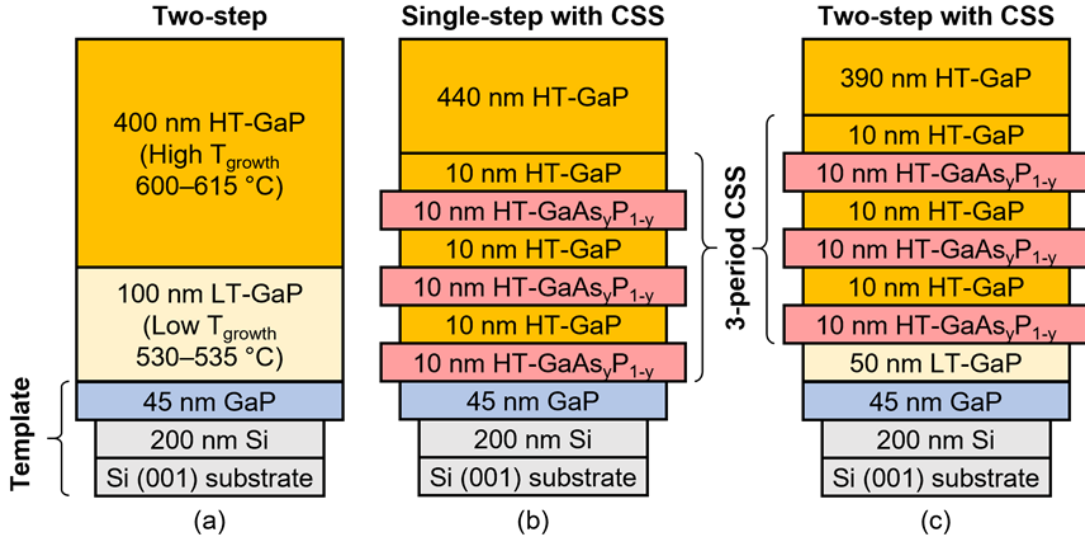
Fig. 6.1: Layer structures for (a) "two-step", (b) "single-step with CSS", and (c) "two-step with CSS" designs of relaxed GaP on GaP/Si templates. The template and CSS structures are highlighted. For ease, high and low T_{growth} are abbreviated as HT and LT, respectively. Adapted from this work, Ref. [65].

V/III of 15, while GaAs$_y$P$_{1-y}$ of the CSS was grown with the same Ga and P fluxes resulting in slightly higher growth rate and V/III due to increased lattice constant and added As flux. All samples with a CSS used a 3-period structure with a period of 10 nm GaAs$_y$P$_{1-y}$ and 10 nm GaP similar to Ref. [37]. Fig. 6.1 shows the MBE layer structures in this study including the "two-step" design (Fig. 6.1(a), samples from Chapter 5), "single-step with CSS" design (Fig. 6.1(b)) where the CSS was grown directly on the GaP/Si template similar to Ref. [37], [86], and "two-step with CSS" design (Fig. 6.1(c)) initiating growth with 50 nm GaP at low growth temperature (T_{growth}) of 530 °C – 535 °C before the CSS combining ideas from Refs. [36] and [37], [86]. CSS and GaP overgrowth to 500 nm MBE GaP thickness (545 nm III-V on Si) were grown at high T_{growth} of 600 °C – 615 °C. Two-step with CSS samples included 50 nm low T_{growth} GaP instead of 100 nm to balance observations from my prior work indicating < 50 nm of low T_{growth} was less effective at suppressing dislocation introduction [36] and from Boyer's prior work indicating placing the CSS > 50 nm from the GaP/Si interface was less effective at TDD reduction [86].

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GaAs$_y$P$_{1-y}$ layers in CSS samples were integrated into GaP growth using As and P valved cracker cells and bulk GaAs$_y$P$_{1-y}$ composition calibration results. The growth procedure utilized for the CSS on our solid-source MBE was as follows: start with P overpressure and keep same P valve position throughout CSS, add As overpressure with As valve position based on calibrated flux measurements before growth, wait a few seconds for As flux to roughly stabilize, open Ga for GaAs$_y$P$_{1-y}$ growth, close Ga and As and wait a minute for As to be pumped away, open Ga for GaP growth, close Ga, and repeat. GaAs$_y$P$_{1-y}$ composition in the CSS samples was measured with high-resolution x-ray diffraction (XRD) by fitting a (004) symmetric ω–2θ line scan (Fig. 6.2(a)) [65].

Initially, I grew a bulk GaAs$_y$P$_{1-y}$ composition calibration intended for the CSS at ~0.5 μm/hr and P flux of 1.12E-5 Torr (on beam flux monitor (BFM)) as used for GaP, since this calibration was expected to be different from the graded buffer calibration at ~1.0 μm/hr and P flux of 1.88E-5 Torr BFM due to the P flux change. However, Fig. 6.2(b) demonstrates lower y$_{As}$ was found in the CSS than in either bulk calibration. Samples discussed in this chapter followed the ~0.5 μm/hr bulk calibration; following this work I utilized the ~1.0 μm/hr bulk calibration with
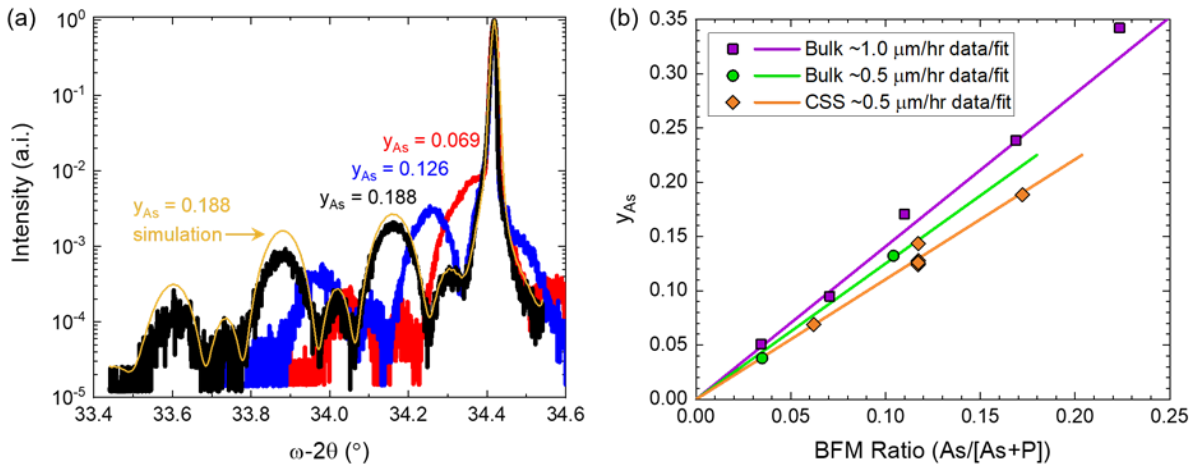
Fig. 6.2: Compositions calibration for GaAs$_y$P$_{1-y}$ in CSS. (a) Examples of (004) symmetric ω–2θ line scans for samples with various measured y$_{As}$ in the CSS. The simulation curve fit to measured data for the y$_{As}$ = 0.188 sample is also shown in yellow. (b) 600 °C GaAs$_y$P$_{1-y}$ layer data points and composition calibration fits against BFM ratio comparing bulk samples grown at either ~1.0 μm/hr and 1.88E-5 Torr P BFM (purple) or ~0.5 μm/hr and 1.12E-5 Torr P BFM (green) against GaAs$_y$P$_{1-y}$ in CSS layers at ~0.5 μm/hr and 1.12E-5 Torr P BFM (orange).

a slope correction factor (Fig. 6.2(b)). Most CSS samples were originally targeted for $y_{As} \sim 0.15$ but were measured as $y_{As} \sim 0.124 - 0.144$. Two additional samples to be discussed in Chapter 6.3 were grown at higher and lower targets resulting in $y_{As} = 0.188$ and 0.069, respectively. Measured CSS period thickness ranged from 18.7 nm to 19.9 nm, slightly lower than the 20 nm target. Ga and As flux transients likely caused the lower y_{As} and lower thickness for CSS layers as each 10 nm layer was around 1 min.

Similar to Boyer *et al.* [37], [86], Fig. 6.3 shows that incorporating a three-period GaAs$_y$P$_{1-y}$ CSS early in growth significantly reduced the TDD of *n*-GaP on Si [65]. Initiating growth at high T_{growth} with the CSS directly on the GaP/Si templates as done by Boyer [37], [86] reduced TDD from 3.1 ($\pm$0.4) $\times$ 10^7 cm^{-2} for the two-step design to 3.71 ($\pm$0.08) $\times$ 10^6 cm^{-2} for the single-step with CSS design when doped with $\sim$2 $\times$ 10^{18} cm^{-3} Si [65] though to a lesser extent than observed by Boyer [37]. For the two-step with CSS design TDD reduced further down to 2.54 ($\pm$0.23) $\times$ 10^6 cm^{-2} [65], similar Boyer's lowest of 2.4 ($\pm$0.4) $\times$ 10^6 cm^{-2} [37]. While Boyer observed higher TDD when placing the CSS further from the interface between GaP/Si, CSS starting at 90 nm GaP was worse than at 50 nm GaP [86], I observed lower TDD with increased CSS separation from Si, 45 nm GaP for single-step with CSS was worse than 95nm GaP for two-step with CSS design. The

Two-step   Single-step with CSS   Two-step with CSS

(a)   30 μm   (b)   30 μm   (c)   30 μm

TDD: 3.1($\pm$0.4)$\times$10^7 cm^{-2} TDD: 3.71($\pm$0.08)$\times$10^6 cm^{-2} TDD: 2.54($\pm$0.23)$\times$10^6 cm^{-2}
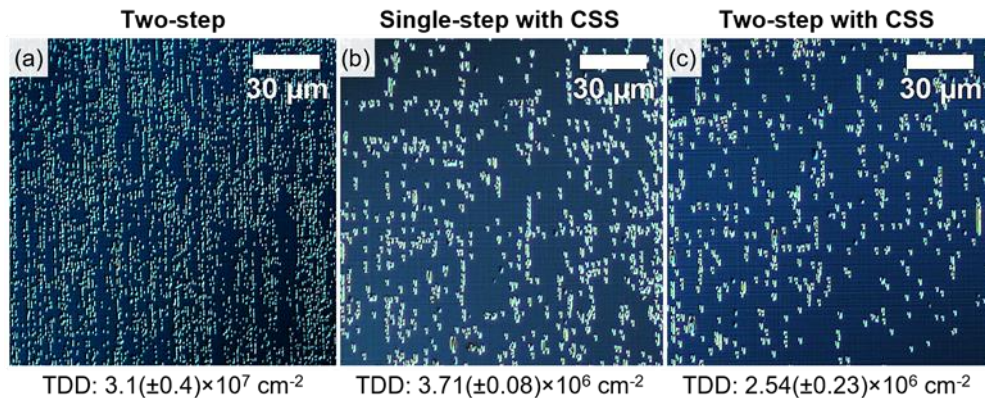
Fig. 6.3: Comparison of Nomarski micrographs after DSE of two-step *n*-GaP on GaP/Si with $\sim$2 $\times$ 10^{18} cm^{-3} Si doping grown with (a) two-step, (b) single-step with CSS, and (c) two-step with CSS designs. The high TDD of (a) needed to be counted by SEM imaging. CSS samples had $y_{As} = 0.124 - 0.144$. Adapted from this work, Ref. [65].

difference in these results indicates that low T_{growth} initiation on our GaP/Si templates through the critical thickness is again helpful for suppressing dislocation introduction early in the growth, consistent with my results discussed in Chapter 4 [36]. CSS inclusion for relaxed n-GaP on Si increased strain relaxation to 116%/72% for the A/B-directions at room temperature (RT) in comparison to 92%/64% for two-step n-GaP ($\sim 2 \times 10^{18}$ cm^{-3} Si; see Table 5.1 for other two-step growths) but the relaxation anisotropy remained, indicating similar improvement for α and β dislocation glide velocities. CSS inclusion eliminated TDD inhomogeneities and decreased surface roughness to levels of UID or Be-doped samples [65].

6.3 Variations for Two-step with CSS Design

Fig. 6.4 compares the effect of varied GaAs$_y$P$_{1-y}$ composition for the two-step with CSS design. The lowest n-GaP TDD for two-step with CSS growth was observed with y_{As} of $\sim$0.124 –
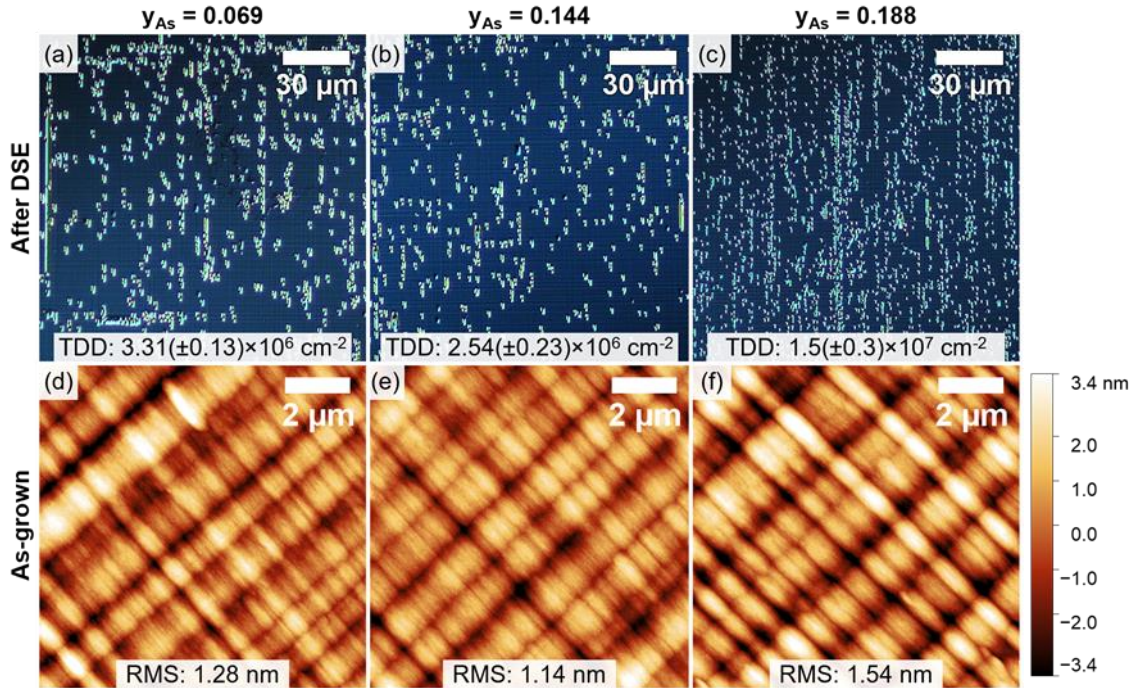
Fig. 6.4: Comparison of n-GaP on GaP/Si with $\sim 2 \times 10^{18}$ cm^{-3} Si doping grown with (a, d) two-step, (b, e) single-step with CSS, and (c, f) two-step with CSS designs. (a – c) Nomarski micrographs after DSE and (d – f) AFM images of as-grown surface morphology (z-range = 6.8 nm). The high TDD of (c) needed to be counted by SEM imaging. CSS samples had $y_{As} = 0.124 - 0.144$. Note, all samples here are grown with 600 °C high T_{growth} leading to higher baseline RMS; RMS was 1.23 nm for two-step samples with 600 °C high T_{growth} and $\sim 4 \times 10^{17}$ Be doping.

0.144 [65], and both the lower or higher y_{As} tested caused higher TDD (Fig. 6.4(a – c)). Reducing y_{As} to 0.069 caused a slight reduction in CSS efficacy, increasing TDD to 1.3 × of the y_{As} = 0.144 sample. The TDD increase for the lower y_{As} sample was primarily attributed to increased dislocation pileup density. I also observed TDD inhomogeneity for this sample from dislocation blocking by pileups. On the other hand, increasing y_{As} to 0.188 significantly limited CSS efficacy at reducing TDD; TDD of this sample was 1.5 ($\pm$0.3) × 10^7 cm^{-2}, half that of the two-step n-GaP sample without CSS while other samples with CSS decreased by an order of magnitude. The strong TDD increase for the higher y_{As} sample was from the field TDD and not from trenches or pileups. These results indicate that added local strain from higher y_{As} may reduce the formation of pileups, perhaps by providing additional energy to glide through dislocation glide barriers. However, too high of local strain may possibly cause dislocation introduction within the CSS. Oddly, the GaAs$_y$P$_{1-y}$ composition (y_{As} = 0.188) closest to that used by Boyer (y_{As} = 0.17) was much less effective than Boyer observed [37] or I observed at lower y_{As}. The difference might be due to difference in CSS placement as my comparison samples were grown with the CSS starting 95 nm from the GaP/Si interface as opposed to Boyer's 50 nm.

Similar to Chapter 5.2, I investigated the effect of doping level on effectiveness of the two-step with CSS design for TDD reduction (Fig. 6.5) [65]. A UID two-step with CSS sample was grown to test if TDD < 1 × 10^6 cm^{-2} would be achieved without n-type doping and served as proxy for p-type doping. TDD did not change when adding a CSS for UID GaP; TDD was 1.15 ($\pm$0.11) × 10^6 cm^{-2} for two-step and 1.15 ($\pm$0.06) × 10^6 cm^{-2} for two-step with CSS [65]. In Chapter 4.3, I showed that for p-GaP on Si, most dislocation introduction appears to occur within the first 100 or 200 nm of growth and that by switching to high T_{growth} in a two-step design allows relaxation by glide of existing dislocations [36]. The lack of benefit from the CSS in the UID case indicates that
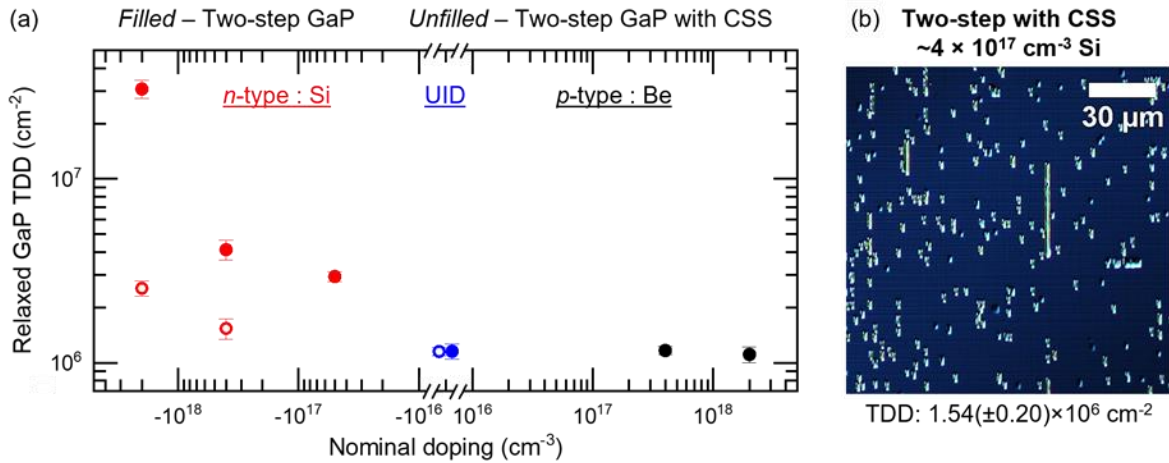
Fig. 6.5: (a) Dependence of relaxed GaP on Si samples with either two-step (filled points) or two-step with CSS (unfilled points) designs. Note, two-step samples were discussed when shown in Fig. 5.3 of Chapter 5.2. (b) Nomarski micrograph after DSE for the sample with the lowest reported TDD for relaxed *n*-GaP on Si to date. Adapted from this work, Ref. [65].

glide velocity is already fast enough at high T_{growth} in both the UID and *p*-doped cases. Research attempting to drop the TDD of relaxed GaP on Si below 1×10^6 cm^{-2} should focus on methods to suppress dislocation introduction when beginning growth on GaP/Si templates.

Even lower *n*-GaP TDD can be achieved when combining together TDD reduction strategies in Chapters 5 and 6, including a two-step design, a CSS, and lower *n*-doping. Dropping Si doping to ~4×10^{17} cm^{-3} for a two-step with CSS design resulted in a TDD of 1.54 (± 0.20) $\times$ 10^6 cm^{-2} (Fig. 6.5(b)), the lowest TDD I am aware of for relaxed *n*-GaP on Si. Taking together results comparing two-step and two-step with CSS designs at varied doping concentrations in Fig. 6.5(a), the efficacy of a CSS to decrease TDD reduces with lower *n*-type doping. Consequently, the disparity between *n*-GaP and UID/*p*-GaP could be decreased with lower *n*-type doping, but this would lead to trade-offs for III-V/Si multi-junction solar cells as noted in Chapter 5.2. Nonetheless, I decreased relaxed *n*-GaP TDD from 3.1 (± 0.4) $\times 10^7$ cm^{-2} with ~2×10^{18} cm^{-3} Si doping down by a factor of 20 with ~4×10^{17} cm^{-3} Si doping and two-step with CSS design, approaching TDD parity between *n*-doped and UID or *p*-doped GaP on Si.

6.4   Effect of Improved *n*-GaP Buffer for GaAsP Top Cells on Si

In this section, I compare ~1.7 eV GaAsP 1J top cells grown on GaP/Si templates with different $GaAs_yP_{1-y}$/GaP buffer layer doping, demonstrating similar GaAsP 1J TDD and device performance when grown on either UID buffers or *n*-doped buffers using the improved *n*-GaP design described in the previous paragraph. Previously, Fan and I found the TDD of GaAsP top cells was ~2.6 × higher on *n*-doped buffers (~2.5 × 10^{18} cm^{-3} Si doping) than on UID buffers [55]. Results from Chapter 5.2 indicated the GaAsP TDD difference was caused by an even larger relaxed GaP TDD difference with doping type as the TDD of *n*-doped GaP (~2 × 10^{18} cm^{-3} Si) was > 26 × higher than UID or *p*-doped GaP [65]. While TDD using UID $GaAs_yP_{1-y}$/GaP buffers on GaP/Si templates increased from 1.15 (±0.11) × 10^6 cm^{-2} for GaP to 4.5 (±0.6) × 10^6 cm^{-2} for ~1.7 eV GaAsP, TDD using *n*-doped (~2.5 × 10^{18} cm^{-3} Si) buffers decreased from > 3 × 10^7 cm^{-2} for GaP to 1.2 (±0.2) × 10^7 cm^{-2} for ~1.7 eV GaAsP [55], [65]. Interestingly, the *n*-$GaAs_yP_{1-y}$ step-graded buffer appears to have filtered the high *n*-GaP TDD. Even so, the high *n*-GaP TDD was detrimental to the final GaAsP TDD. With the TDD of *n*-doped (~4 × 10^{17} cm^{-3} Si) and UID GaP nearing parity using the two-step with CSS design as described in the previous section, ~1.7 eV GaAsP top cells were again compared on differently-doped buffers.

~1.7 eV GaAsP 1J top cells similar to Ref. [21] were grown by solid-source MBE on GaP/Si templates using $GaAs_yP_{1-y}$/GaP buffers either UID or *n*-doped (~4 × 10^{17} cm^{-3} Si) [127]. GaP buffers were initiated with low T_{growth} at 545 °C – 555 °C and followed by high T_{growth} at 610 °C – 620 °C using the two-step design for UID buffers and the two-step with CSS design for the "improved" *n*-buffers.[21] $GaAs_yP_{1-y}$ graded buffers (28-step, 2.79 μm, -1.04%/μm misfit grading rate) were grown at 605 °C – 615 °C. Low T_{growth} layers including the p^+-GaAsP lateral conduction

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[21] T_{growth} was unintentionally ~10 °C – 15 °C higher for all layers of these growths due to substrate mounting method.

layer (LCL), p^+-GaInP etch stop, n^+-AlInP window layer, and n^+-GaAsP contact were grown at 490 °C – 495 °C. On top of the GaInP etch stop, high T_{growth} layers including the p^+-GaAsP spacer, p^+-AlGaAsP (28.5%Al) back surface field (BSF), and $n^+/i/p$ active region were grown without pauses at 635 °C – 640 °C [127]. Chapter 7.2 discusses this GaAsP top cell design choice in more detail as well as resulting effects on graded buffer design, dark line defects, and device performance in more detail (see Fig. 7.3(f) in Chapter 7.1 for an example of the layer structure).

Solar cell devices were fabricated similar to [55] by photolithography and selective wet etching to define mesas with area from 1.21 – 12.25 mm^2 [65]. Metal contact was made with Ti/Au n-contact top grid with ~3% – 5% metal coverage of the mesa and a Cr/Au p-contact on top of the p^+-GaAsP LCL. A TiO$_2$/SiO$_2$ double layer anti-reflection coating (DLARC) was sputtered on the n^+-AlInP window layer after etching the n^+-GaAsP contact and before mesa isolation. External quantum efficiency (EQE) and specular reflection were measured with a PV Measurements QEX7; no significant differences in specular reflection were observed between the two solar cells studied [127]. In-house lighted current-voltage (LIV) measurements were tested with an ABET Technologies 10500 Solar Simulator approximating the AM1.5G spectrum. Electron beam-induced current (EBIC) mapping was performed with a JEOL JSM-6060LV scanning electron microscope at an accelerating voltage of 8 kV for estimating TDD (survey area $> 3.5 \times 10^4$ μm^2) and 16 kV for investigating dark-line defects affecting the back surface of the active region (survey area $> 6.8 \times 10^4$ μm^2). As demonstrated in Chapter 3.3.2 and prior work in Chapter 7.2 [21], plan-view EBIC with varied accelerating voltage was used to tune the imaging conditions for probing the front/back surface of the active region with low/high accelerating voltage.

Fig. 6.6 compares TDD of ~1.7 eV GaAsP top cells grown on UID vs improved n-doped GaAs$_y$P$_{1-y}$/GaP buffers. First, cells on UID buffers are discussed in detail before comparing against
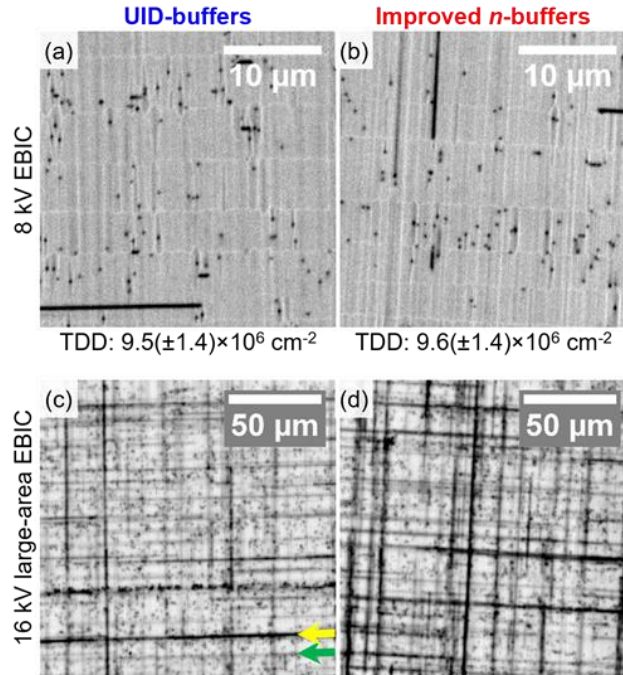
Fig. 6.6: EBIC comparisons of GaAsP top cells grown on (a, c) UID buffers or (b, d) improved *n*-doped buffers. (a, b) Comparisons with 8 kV accelerating voltage for GaAsP TDD estimation. (c, d) Large-area EBIC with 16 kV for comparing dark line defects affecting the back surface of the active region. Yellow/green arrows on (c) show an example of higher/lower contrast dark line defects. From this work, Ref. [127] © 2021 IEEE.

cells on improved *n*-doped buffers. GaAsP top cells on UID buffers had TDD of 9.5 ($\pm$1.4) $\times 10^6$ cm^{-2} (Fig. 6.6(a)), likely higher than previous work due to higher misfit grading rate and unoptimized T_{growth} for the graded buffer. Graded buffers in this study and presently in the Lee group are thinner than in previous work by Nay Yaung *et al.* [34] to avoid cracking from thermal mismatch while accommodating a thicker active region and the 0.5 μm GaAsP spacer layer beneath the AlGaAsP BSF. For ~1.7 eV GaAsP on UID and *p*-doped GaAs$_y$P$_{1-y}$/GaP buffers on Si, the Lee group and I have observed a roughly direct dependence of typical TDD with grading rate as expected by Fitzgerald *et al.* [33]; ~4 $-$ 5 $\times 10^6$ cm^{-2} (-0.56%/μm), ~5 $-$ 7 $\times 10^6$ cm^{-2} (-0.80%/μm), and ~7 $-$ 9 $\times 10^6$ cm^{-2} (-1.04%/μm) [21], [34], [52], [55], [127].

Even with elevated TDD and higher dark line defect density (Fig. 6.6(c)) than previous [21], GaAsP top cells on UID buffers reached 19.30 mA/cm^2 EQE-integrated J$_{SC}$ and 16.82%
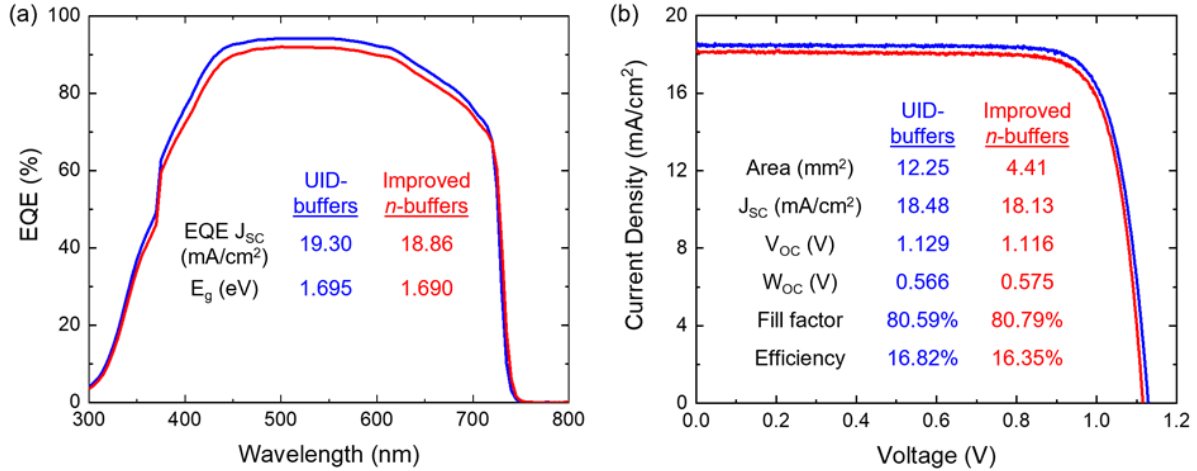
Fig. 6.7: (a) EQE and (b) in-house 1-sun AM1.5G LIV comparisons of hero devices for GaAsP top cells grown on UID buffers (blue) or improved *n*-doped buffers (red). Figures of merit are inset. Adapted from this work, Ref. [127] © 2021 IEEE.

efficiency (blue in Fig. 6.7) [127]. While back surface dark line density was ~2.5 × higher than previously shown for GaAsP top cells with AlGaAsP (34%Al) BSF [21], the increase was solely from lower contrast dark lines thought to be less harmful. As can be observed in Fig. 6.6(c), two populations of dark line defects are observed, a lower contrast population appearing gray and a higher contrast population appearing black; higher contrast indicates stronger non-radiative recombination. I suspect decreasing the AlGaAsP BSF from 34%Al to 28.5%Al may have decreased screening of the active region from the lower contrast population of dark line defects, and when combined with the effect of higher TDD, led to reduced long-wavelength EQE worth ~0.2 mA/cm^2. Further work on AlGaAsP BSF optimization (higher %Al, higher thickness, higher GaAsP spacer thickness) should be investigated to potentially enable reduced back surface dark line density and higher long-wavelength EQE. Promisingly, device performance similar to the best-reported GaAsP top cells on Si [21], [52] was realized, even with TDD approaching 1×10^7 cm^{-2} [127].

Instead of finding a large TDD increase for GaAsP top cells grown on *n*-doped buffers, I observed almost no change in TDD to 9.6 ($\pm$1.4) $\times 10^6$ cm^{-2} (Fig. 6.6(b)) using the improved *n*-

GaP buffer design [127]. Thanks to the improved *n*-GaP buffer, GaAsP TDD on *n*-buffers was reduced even with a ~2 × higher misfit grading rate of -1.04%/μm; GaAsP TDD was 1.2 (±0.2)× 10^7 cm^{-2} using -0.56%/μm grading rate on previous *n*-GaP buffers [55]. Now with parity between UID and *n*-doped GaAs$_y$P$_{1-y}$/GaP buffers on Si, further attention is required to decrease the large TDD contribution of the thinned GaAs$_y$P$_{1-y}$ graded buffer, ~8 × 10^6 cm^{-2}. Boyer *et al.* realized even lower ~1.7 eV GaAsP TDD with *n*-doped buffers on Si down to 3.0 (±0.6) × 10^6 cm^{-2} by growing the thinned GaAs$_y$P$_{1-y}$ graded buffer hot (675 °C – 725 °C, -1.0%/μm grading rate), only 6 × 10^5 cm^{-2} higher than the 2.4 (±0.4) × 10^6 cm^{-2} *n*-GaP buffer on which it was grown [37]. Taken together, these results indicate the possibility of enabling GaAsP TDD on *n*-buffers down to nearly 2 × 10^6 cm^{-2} in the near term.

With GaAsP TDD nearly equal, the ~1.7 eV GaAsP top cell device performance was similar on UID and *n*-doped buffers using improved *n*-GaP [127]. GaAsP efficiency on *n*-buffers was < 0.5% absolute efficiency (< 3% relative) lower than on UID buffers (Fig. 6.7(b)), primarily due to EQE loss spread over all wavelengths (Fig. 6.7(a)). Reflection losses from DLARC were almost identical and did not result in the EQE difference. While back surface dark line density only slightly increased, dark lines with higher contrast increased in density by > 2.5 × than on UID buffers (Fig. 6.6(c, d)). A stronger effect from back surface dark line defects might account for the higher bandgap-voltage offset ($W_{OC} = E_G/q - V_{OC}$) and lower long-wavelength EQE. However, it is uncertain why the short-wavelength and peak EQE were also lower, as front-surface dark line density from 8 kV EBIC was similar for both top cells. Instead, EQE loss over all wavelengths may suggest suboptimal substrate temperature during the active region growth on *n*-buffers. Despite the slight performance losses, GaAsP top cells on *n*-GaAs$_y$P$_{1-y}$/GaP buffers on Si achieved efficiency up to 16.35% by using our improved *n*-GaP buffer [127]. The results presented in this

section are promising for high-current GaAsP/Si 2J solar cells that could be further enhanced with even higher top cell current and V_{OC} by lowering TDD.

6.5   Chapter Findings

Primary findings in this chapter are listed below:

- Incorporating a compressively strained superlattice (CSS) structure of GaAs$_y$P$_{1-y}$/GaP reduced threading dislocation density (TDD) for relaxed n-type ($\sim 2 \times 10^{18}$ cm^{-3} Si) GaP on Si as low as 3.71 (± 0.08) $\times 10^6$ cm^{-2} for CSS growth directly on GaP/Si template.

- Two-step with CSS design decreased TDD to 2.54 (± 0.23) $\times 10^6$ cm^{-2} by using a thin low T$_{growth}$ layer extending past critical thickness for lower initial defect introduction.

- Lower n-doping of $\sim 4 \times 10^{17}$ cm^{-3} in combination with the two-step with CSS design enabled the lowest reported TDD for relaxed n-GaP on Si of 1.54 (± 0.20) $\times 10^6$ cm^{-2}.

- ~ 1.7 eV GaAsP single-junction solar cells had similar TDD and device performance on either UID or improved n-doped GaAs$_y$P$_{1-y}$/GaP buffers – previous n-doped buffers caused $\sim 2.6 \times$ higher TDD than comparable UID buffers.

CHAPTER 7

GAASP/SI SOLAR CELL DEVELOPMENT

Continued advancement of ~1.7 eV GaAsP solar cells on Si requires both improved methods to reduce defect densities hampering top cell performance and optimized device design to lessen losses from defects and light management. Research to improve the efficiency of GaAsP single-junction (1J) solar cells has primarily focused on threading dislocation density (TDD) reduction or on improved barrier layer choices. While intended for GaAsP/Si double-junction (2J) solar cells, GaAsP 1J cells in the Lee group utilized *p*-doped GaAs$_y$P$_{1-y}$/GaP buffer layers for convenience. However, the GaAsP/Si 2J architecture provides additional challenges by requiring considerations for *n*-doped buffers, tunnel junction inclusion, and current-matching to the Si sub-cell. In this chapter, I first detail the history of metamorphic GaAsP 1J development in the Lee group and initial GaAsP/Si 2J development. I also discuss additional electrically-active defects, here called "dark line defects" (DLDs), that have been observed by electron beam-induced current (EBIC) imaging from the Lee group's earliest GaAsP 1J cells. Later in this chapter, I describe design and implementation of AlGaAsP back surface field (BSF) layer structure that reduced dark line defect density at the back surface of the top cell resulting in improved current collection. Switching from n^+/p to $n^+/i/p$ junction design increased the depletion width to further improve long-wavelength current collection. Lastly, top cell design improvements were applied to GaAsP/Si 2J solar cells. As a result of design improvements, Fan and I achieved AM1.5G efficiencies up to 17.6% and 25.0% for GaAsP 1J and GaAsP/Si 2J solar cells, respectively [21].[22]

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[22] Parts of this chapter are reproduced from [S. Fan, Z. J. Yu, R. D. Hool *et al.*, "Current-Matched III–V/Si Epitaxial Tandem Solar Cells with 25.0% Efficiency," *Cell Rep. Phys. Sci.*, vol. 1, no. 9, p. 100208, Sep. 2020, doi: 10.1016/j.xcrp.2020.100208.] as open access article under the CC BY-NC-ND license © 2020 Elsevier.

7.1 History of GaAsP/Si in the Lee Group 2009 – 2018

With the Lee group's molecular beam epitaxy (MBE) growth of $GaAs_yP_{1-y}$ dating back to 2009, the Lee group has spent > 10 years developing metamorphic ~1.7 eV GaAsP for solar cells. While not among the earliest investigating GaAsP solar cells [45], [136]–[139], the Lee group's timing coincided with the development of high-quality pseudomorphic GaP on Si templates [23], [24]. Lang *et al.* received and utilized the first template wafers received from NAsP$_{III/V}$ GmbH, 2" GaP/Si (001) with 6° offcut [47]. Following, the Lee group used cleaved pieces of commercial 300 mm (12") wafers of GaP/Si (001) on-axis from NAsP$_{III/V}$. The Lee group primarily focused on GaAsP 1J solar cell development, often co-grown on GaP/Si templates and GaP substrates, resulting in *p*-doped buffer use to either aid current spreading for double top-contacted devices or conduction to a bottom contact for some devices on GaP substrates. This research centered around device design as well as TDD reduction; see Fig. 7.1(a) for TDD comparison against bandgap-
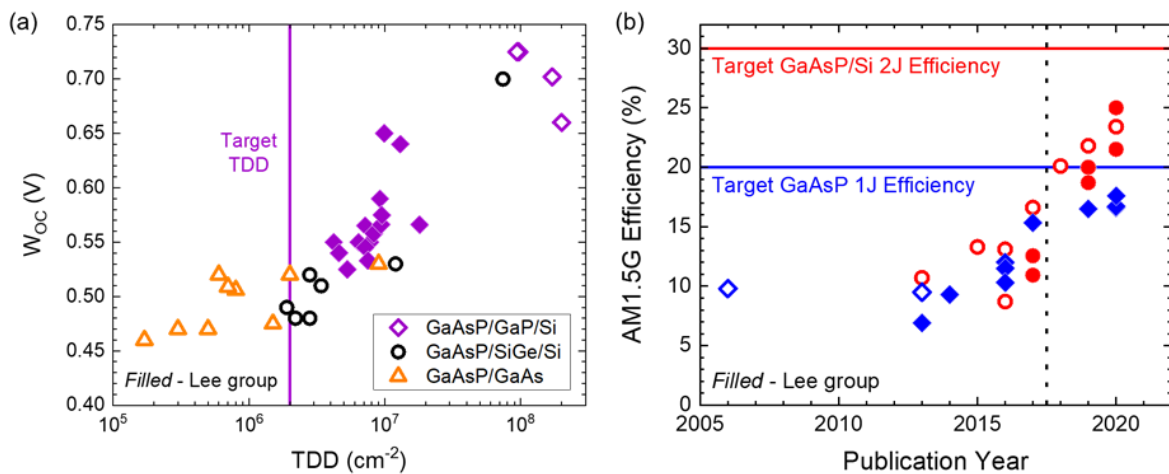
Fig. 7.1: Advancement of GaAsP solar cells. (a) Bandgap-voltage offset ($W_{OC} = E_G/q - V_{OC}$) plotted against TDD to demonstrate the reduction in W_{OC} (improvement in V_{OC}) from lower TDD [21], [34], [43], [45], [47], [48], [50], [52], [57], [127], [136]–[142]. W_{OC} is used to compare V_{OC} between samples with varying E_G. Alternative substrate and buffer choices are shown to demonstrate achievable W_{OC} values at low TDD. Vertical line indicates targeted TDD for GaAsP on GaP/Si. (b) AM1.5G efficiency of ~1.7 eV GaAsP 1J and GaAsP/Si 2J solar cells with $GaAs_yP_{1-y}$/GaP buffers on Si [14], [21], [34], [41], [45]–[53], [55], [56], [143]. Horizontal lines show target GaAsP 1J and GaAsP/Si 2J efficiencies. Data left of the dotted line was performed before I joined the Lee group. For both (a) and (b), filled points show data from the Lee group.

voltage offset ($W_{OC} = E_G/q - V_{OC}$) (V_{OC} is open-circuit voltage), a common metric to compare device performance for materials with varying E_G [21], [34], [43], [45], [47], [48], [50], [52], [57], [127], [136]–[142]. During the same timeframe, Grassman *et al.* developed a high-quality GaP/Si template recipe [25], [26] and utilized the template to mostly focus on GaAsP/Si 2J solar cell development [14], [41], [46], [49]. Fig. 7.1(b) shows the advancement of GaAsP 1J and GaAsP/Si 2J solar cell efficiencies primarily by the Lee and Grassman/Ringel groups [14], [21], [34], [41], [45]–[53], [55], [56], [143].

Fig. 7.2 and Fig. 7.3 summarize the development of ~1.7 eV GaAsP 1J solar cell performance in the Lee group based on changes to the layer structure over years of iteration [21], [34], [47], [48], [50], [52], [57]. These figures illustrate the changes from a simplistic diode structure with only GaAs$_y$P$_{1-y}$ for demonstration purposes to a complex device structure producing high current. Many additional experimental comparisons besides the main changes mentioned below were performed and are detailed in the referenced literature.

In 2011, Tomasulo *et al.* grew devices (n^+/p, 100/2000 nm, $3 \times 10^{18}/1 \times 10^{17}$ cm^{-3}) on p-GaP substrates with thick compositionally-graded buffer (CGB) layers (~5 − 6 μm, grading rate ~
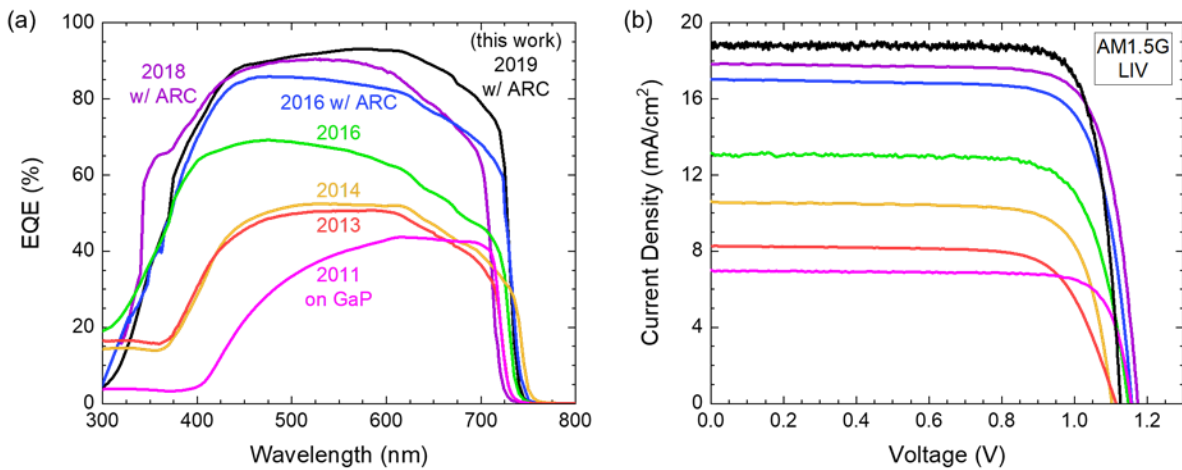
Fig. 7.2: Advancement of best (a) external quantum efficiency (EQE) and (b) lighted current-voltage (LIV) under approximate 1-sun AM1.5G illumination for ~1.7 eV GaAsP 1J solar cells in Lee group. Device results from [21], [34], [47], [48], [50], [52], [57]. Note years reported here are in relation to sample growth date.
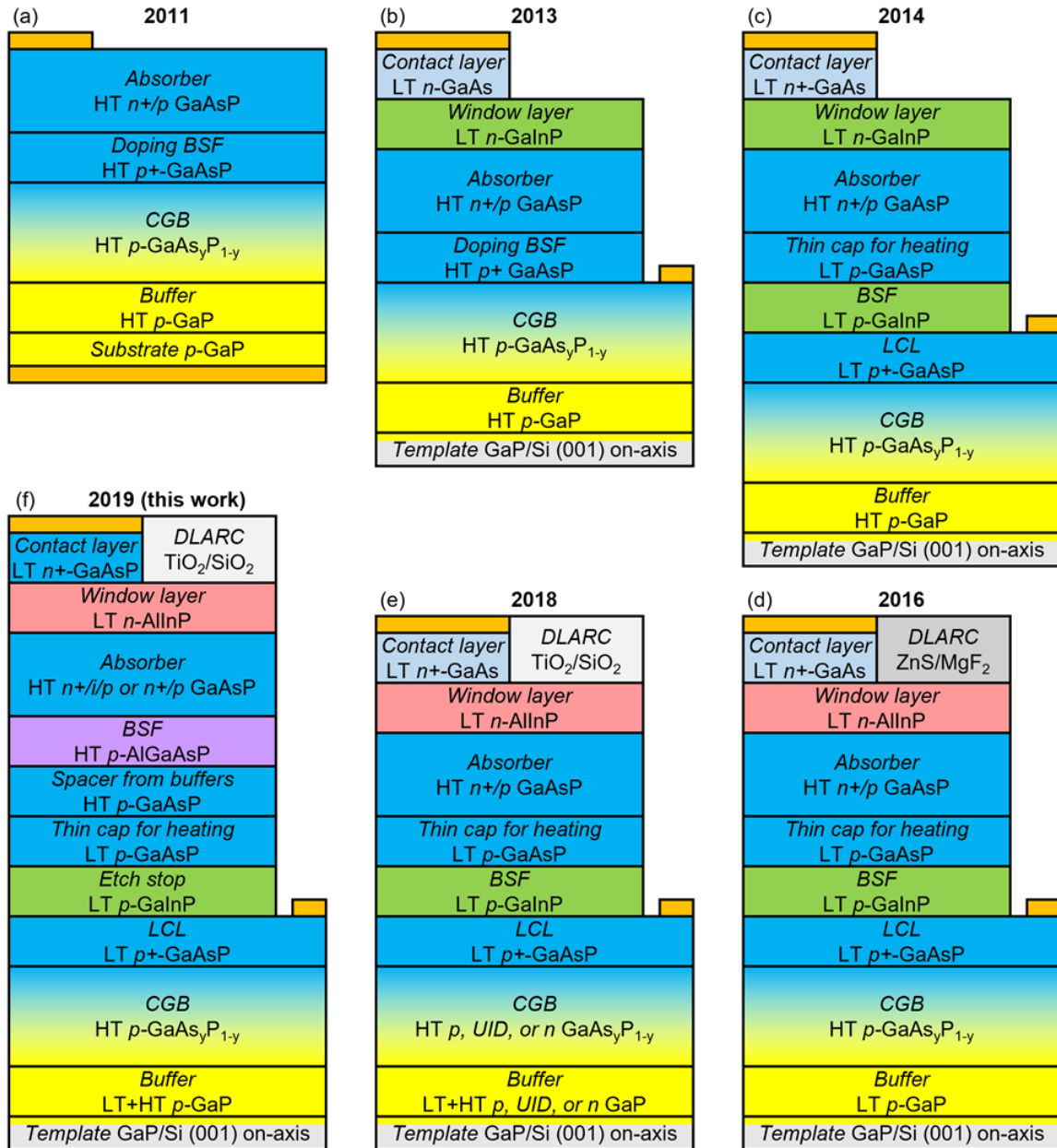
Fig. 7.3: Advancement of ~1.7 eV GaAsP 1J solar cell design in the Lee group. The year and complexity of the design increases from (a) – (f) clockwise from top left. Layer structures are simplified to focus on layer material choices and doping type, instead of thicknesses, growth temperatures, and doping concentrations which also affected material and device quality. Unmarked gold rectangles indicate contact metal placement. Abbreviations used: HT/LT (high/low growth temperature), DLARC (dual-layer anti-reflection coating), BSF (back surface field), LCL (lateral conduction layer), CGB (compositionally-graded buffer), UID (unintentionally doped). Adapted from [21], [34], [47], [48], [50], [52], [57].

-0.4%/μm) for TDD of $4.1 - 6.3 \times 10^6$ cm^{-2} [57]. Recombination at the barrier-less front surface and within the highly-doped emitter hampered short-wavelength carrier collection. Following in

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2013, Lang *et al.* grew the Lee group's first devices on GaP/Si templates [47]. Addition of an *n*-GaInP window layer improved front surface passivation and improve short-wavelength EQE; emitter doping was also decreased to 2×10^{18} cm^{-3}. TDD increased due to thinner CGB (~3.6 μm, -0.79%/μm) to $6.4 - 7.6 \times 10^6$ cm^{-2} on GaP and $0.92 - 1.3 \times 10^7$ cm^{-2} on GaP/Si. However, high series resistance from poor *n* contact (limited Si doping due to amphoteric effects) harmed fill factor, resulting in AM1.5G efficiency up to 6.9% on GaP/Si [47].

In 2014, Nay Yaung *et al.* changed the BSF from *p*-GaAsP with higher doping to a hetero-barrier *p*-GaInP layer resulting in a small change in EQE [48]. However, improved Si doping for the n^+-GaAs contact,[23] better top contact metal grid design, and use of a heavily p^+-doped lateral conduction layer (LCL) to the bottom contact increased efficiency to 9.3%. Additionally, the relaxed GaP on GaP/Si growth process was improved leading to 7.8×10^6 cm^{-2} TDD on GaP/Si [48]. In 2016, Nay Yaung and Vaisman optimized the growth temperature (T_{growth}) of both *p*-GaAs$_y$P$_{1-y}$ CGB and relaxed *p*-GaP buffer layers and increased the CGB thickness (~5.4 μm, -0.54%/μm)[24] to realize TDD on GaP/Si of $4.0 - 4.6 \times 10^6$ cm^{-2} [34]. Enhancements to the device design including changing from *n*-GaInP to *n*-AlInP window layer, decreasing the emitter thickness and doping (~50 nm, 1×10^{18} cm^{-3}), and adding an anti-reflection coating (ARC) all contributed to improved EQE. The switch from an *n*-GaInP to an *n*-AlInP window layer greatly improved short-wavelength EQE due to the Γ-valley (direct E_G) of the window increasing from ~2.1 eV to ~2.9 eV, respectively; the photon wavelength range affected by parasitic window

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[23] Low growth temperature (~480 °C) and higher V/III ratio (often ~30) were used to "force" Si atoms onto group III lattice sites for improved levels of *n*-type doping.

[24] Note, CGB thicknesses and grading rates were recalculated here to account for the change in GaAs$_y$P$_{1-y}$ growth rate with constant incident Ga flux since lattice constant increases with y_{As}. Previous reports did not account for this effect that results in almost 9% higher growth rate for 1.7 eV GaAs$_{0.77}$P$_{0.23}$ than GaP.
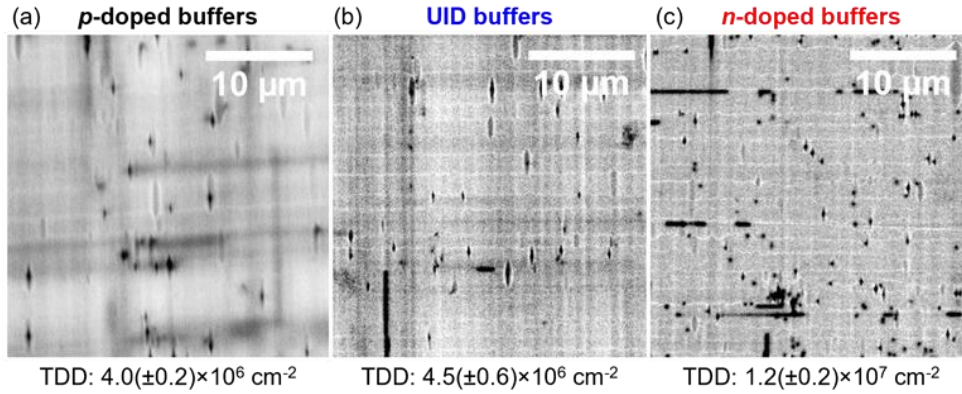
Fig. 7.4: EBIC TDD comparison of ~1.7 eV GaAsP solar cell samples grown on GaAs$_y$P$_{1-y}$/GaP buffers either (a) *p*-doped with Be ~2 × 10^{18} cm^{-3}, (b) unintentionally-doped (UID), or (c) *n*-doped with Si ~2.5 × 10^{18} cm^{-3}. The same buffer thickness was used for all samples (40-step CGB, ~5.4 μm, -0.54%/μm). Note, junction designs and EBIC conditions are different giving altered defect and background contrast. (a) is *n*$^+$/*p* with ~1.5 μm *p*-base, (b) is *n*$^+$/*p* with ~1.0 μm *p*-base, and (c) is *n*$^+$/*i*/*p* with ~0.3 μm intrinsic layer and ~0.7 μm *p*-base. Nay Yaung performed EBIC for (a) with 10.5 kV accelerating voltage using a Philips (now FEI) XL30 [34]. I performed EBIC for (b, c) with 8 kV accelerating voltage using a JEOL JSM-6060LV [55].

absorption reduces from about < 590 nm to < 430 nm, respectively. Taken together, these changes resulted in efficiency up to 12.0% without ARC and 15.3% with ARC [34], [50].

In 2018 during my initial involvement with the Lee group GaAsP/Si project, Fan *et al.* developed an in-house ARC with lower reflection, designed a top contact metal grid with less shadowing, and increased T$_{growth}$ of the ~1.7 eV GaAsP absorber to 625 °C to reach 16.5% efficiency on GaP/Si [52]. Fan and I also investigated the TDD of ~1.7 eV GaAsP 1J solar cells grown on GaAs$_y$P$_{1-y}$/GaP buffers with different doping type (see Fig. 7.4), showing ~3 × higher TDD of with *n*-doped (Si ~ 2.5 × 10^{18} cm^{-3}) buffers than with *p*-doped or unintentionally-doped (UID) buffers; 1.2 × 10^7 cm^{-2} (*n*-doped), 4.0 × 10^6 cm^{-2} (*p*-doped), and 4.5 × 10^6 cm^{-2} (UID), respectively, for similar CGB to 2016 (~5.4 μm, -0.54%/μm) [34], [55].

For 2018 and prior, Fan primarily focused on initial development of GaAsP/Si 2J solar cells. To begin, Fan utilized GaAsP/Si 2J material growth from 2016 to demonstrate 2J solar cell efficiency of 10.92% without ARC and 12.55% with single-layer ARC [143]. Efficiency was limited by an unoptimized GaAsP top cell with high E$_G$ leading to strong current mismatch, an

insufficient tunnel junction (TJ) that harmed fill factor, and unoptimized Si bottom cell with thick substrate and poor back-side passivation causing high recombination at the back contact [143]. The p^+-GaInP:Be/p^+-GaAs:Be/n^+-GaAs:Si/n^+-GaInP:Si TJ layer structure did not maintain adequate performance after thermal treatment from GaAsP top cell growth [144]. In response, Fan designed and tested an (Al)GaAsP-based TJ with high peak tunneling current and low specific resistance even after thermal treatment. High stable doping with C and Te from recently-installed sources on the Lee group MBE enabled sufficient TJ performance using a p^+-AlGaAsP:C/n^+-GaAs:Te/n^+-GaAsP:Te layer structure. Next, Fan advanced processing capabilities for GaAsP/Si 2J device fabrication with a dual-layer ARC, a process for back-side etching to thin the Si substrate without damaging the III-V front-side, and hydrogenated amorphous Si (a-Si:H) carrier-selective Si back contact from collaboration with the Holman group at Arizona State University. With combined TJ and processing improvements, Fan realized GaAsP/Si 2J solar cell efficiency of 20.0% [52]. The 1.69 eV GaAsP top cell current-limited the 2J short-circuit current density (J_{SC}) to 15.9 mA/cm^2, with EQE-integrated J_{SC} of 16.1 mA/cm^2 and 17.5 mA/cm^2 for the GaAsP top cell and Si bottom cell, respectively. GaAsP top cell J_{SC} possibly degraded from the n-doped buffers resulting in ~1 mA/cm^2 lower J_{SC} than expected. Fan further enhanced the GaAsP-filtered Si bottom cell J_{SC} to ~20 mA/cm^2 with back-side random pyramid texturing [52]. While this high current is promising for GaAsP/Si 2J solar cells, the result further emphasized the Lee group's need to improve GaAsP top cell current collection.

7.2   GaAsP Single-Junction (1J) Solar Cell Improvement

From the Lee group's earliest GaAsP 1J solar cells, EBIC imaging of these solar cells has revealed dark line defects (DLDs) for each design (Fig. 7.5). However, the origin of DLDs and the effects on solar cell performance were not known. Vernon *et al.* previously observed DLDs in

Year	Emitter /Base (nm)	BSF Choice	Grading Rate (%/µm)	Substrate	EBIC User	SEM Name	AccV (kV)
2011	100/2000	p^+-GaAsP	-0.44	GaP 2° offcut	Nay Yaung	600	12.5
2013	100/1000	p^+-GaAsP	-0.72	GaP/Si 6° offcut	Nay Yaung	XL30	11
2014	100/1000	p^+-GaInP	-0.75	GaP/Si on-axis	Nay Yaung	XL30	10.5
2016	50/1500	p^+-GaInP	-0.54	GaP/Si on-axis	Nay Yaung	XL30	10.5
2018	50/1000	p^+-GaInP	-0.54	GaP/Si on-axis	Hool	6060LV	8
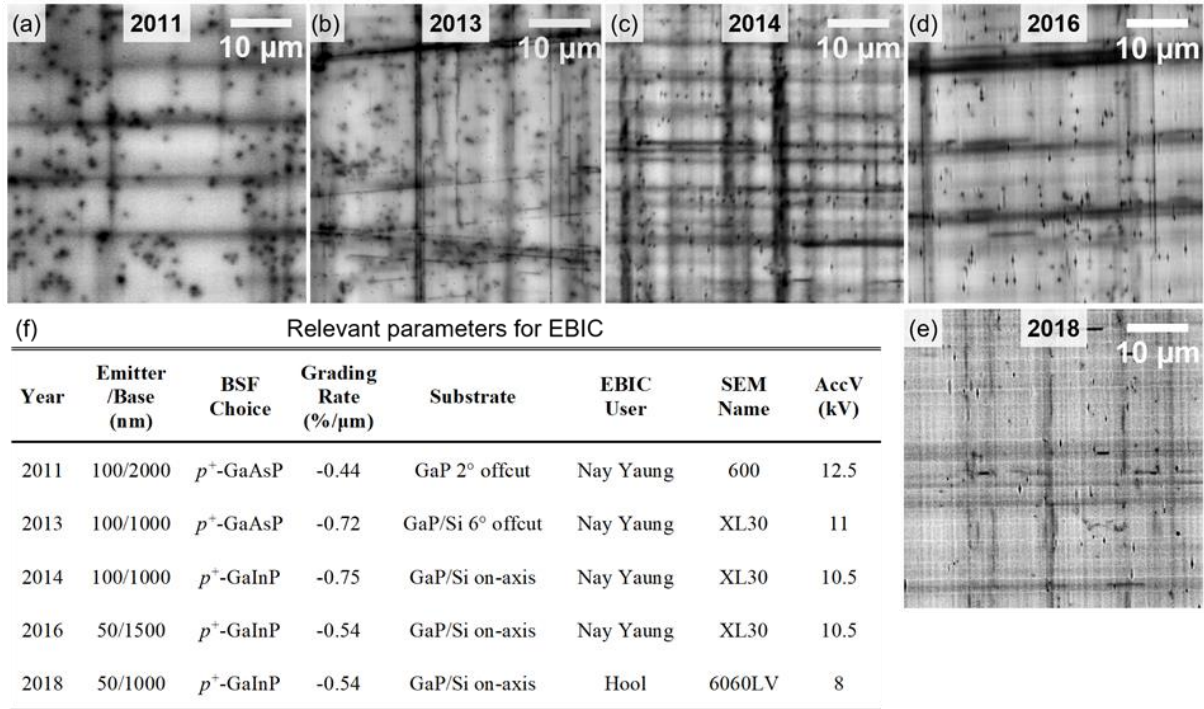
Fig. 7.5: Historical observations of DLDs for metamorphic GaAsP solar cells in Lee group. (a – e) EBIC map examples of ~1.7 eV GaAsP 1J cells by year. Images selected to demonstrate DLDs and *NOT* to compare defect numbers or defect contrast between years. (f) Table with suggested parameters relevant to EBIC for growth design and for EBIC measurement. Full SEM names: Helios NanoLab *600*, FEI Philips *XL30*, and JEOL JSM-*6060LV*. "AccV" is short for SEM accelerating voltage. Data for (a – d) from Nay Yaung related to [34], [47], [48], [57]. Data for (e) by me related to [55].

EBIC for ~1.7 eV GaAsP 1J solar cells (doping BSF and AlGaAsP window layer) grown on GaAs, suggesting DLDs are threading dislocations with segments bent parallel near the junction possibly from composition non-uniformity or strain from doping changes [138]. Other authors have observed DLDs in $Si_{1-x}Ge_x$ on Si or $In_{0.16}Ga_{0.84}As$ quantum wells on GaAs [145]–[148], identifying those DLDs as bundles of misfit dislocations that have enhanced electrical recombination activity [145], [146]. With increasing CGB thickness Vernon demonstrated both reduced TDD and DLD density [138]. Smaller misfit grading rates reduce interactions between misfit dislocations, possibly decreasing the number of misfit dislocation bundles, if any. However, further increasing thickness is not feasible on Si due to thermal expansion mismatch. Thus, understanding of DLDs in GaAsP 1J structures and strategies to mitigate these defects are needed.
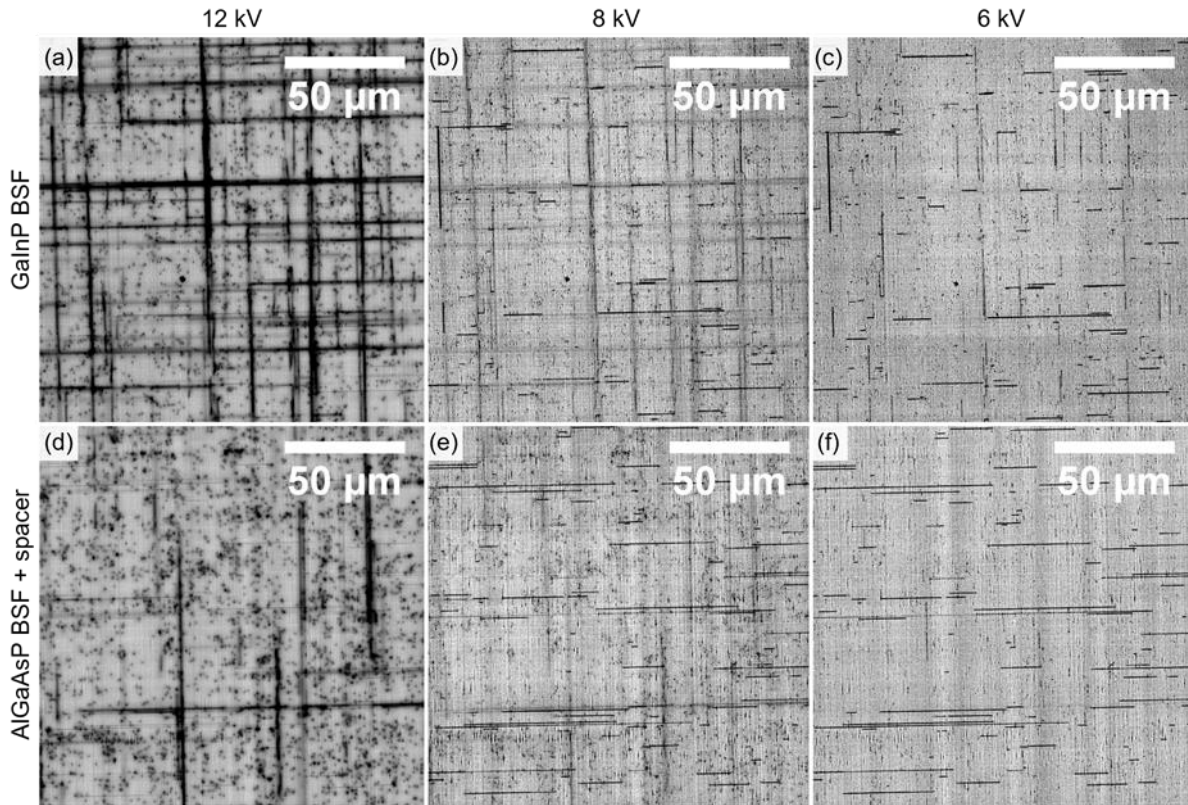
Fig. 7.6: EBIC maps of ~1.7 eV GaAsP 1J solar cells with either (a – c) low T_{growth} GaInP BSF design from 2016 or (d – f) high T_{growth} AlGaAsP BSF with GaAsP spacer design from 2019 for varying electron beam accelerating voltages of (a, d) 12 kV, (b, e) 8 kV, and (c, f) 6 kV. Maps from left to right are taken at the same location to compare dark line defects with varied electron beam interaction depth. Thick DLDs are either observed strongly with 12 kV, faintly with 8 kV, or vanish at 6 kV. Thin DLDs are observed sharpest but faintest at 12 kV and are stronger at 8 kV and 6 kV. Both devices have similar n^+/p junction design and thickness. Adapted from [21].

By varying EBIC accelerating voltage, I observed thick DLDs would lose contrast and vanish with decreasing accelerating voltage, while thin, sharp DLDs would become visible elsewhere (Fig. 7.6). As the electron beam probes deeper into the sample at higher accelerating voltages, I realized thick DLDs affected the back surface of the solar cell active region whereas thin dark lines affected the front surface. Cross-sectional transmission electron microscopy (XTEM) analysis by another Lee group member indicated the thick DLDs at the back surface may be from interfacial misfit dislocations observed at the GaInP BSF layer [21]. However, the difference between scales of XTEM and EBIC inspections as well as non-uniformity of DLDs made the correlation difficult to investigate.

Based on calibrations, I expected the GaInP BSF to be lattice-matched to ~1.7 eV GaAsP, but multiple factors might lead to misfits at GaInP interfaces. Slight composition variations for GaAsP could result from T_{growth} variations in comparison to calibrations. Also, strain from incomplete relaxation of the CGB might result in misfit dislocation introduction with further growth. In addition, temperature ramping between high (> 600 °C) and low (< 500 °C) T_{growth} for the GaAsP solar cell and GaInP BSF, respectively. The MBE growth window for GaInP is < 500 °C leading to In loss and roughened morphology at higher temperatures; the GaInP BSF is capped with ~3 – 5 nm of ~1.7 eV GaAsP at low T_{growth} prior to heating for solar cell growth. Strain from thermal mismatch could drive dislocation glide, and dislocation glide velocity differences between dissimilar materials, such as GaAsP and GaInP, are speculated to pin dislocations [149]. However, it should be noted that DLDs have been observed for each GaAsP 1J solar cell structure on GaP or GaP/Si from the Lee group (Fig. 7.3 and 7.5) [21], [34], [47], [48], [57] including structures *without* GaInP BSF and instead lattice-matched GaAsP doping BSF [47], [57].

In 2019, Fan proposed and tested an "AlGaAsP BSF + spacer" structure as shown in Fig. 7.3(f) for reasons described below [21]. Instead of an GaInP BSF, this structure utilizes a ~55 nm AlGaAsP BSF grown on a 500 nm GaAsP spacer layer and GaInP etch stop layer.[25] Use of AlGaAsP (x_{Al} ~0.34, y_{As} same as GaAsP absorber) for the BSF enables growth of the GaAsP spacer, AlGaAsP BSF, and GaAsP absorber to all be grown at the same high T_{growth} to eliminate growth pauses and temperature ramping between these layers. I showed that adding flux for x_{Al} ~ 0.34 did not affect the y_{As} calibration at this high T_{growth} resulting in consistent nearly perfect

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[25] For double-top metal fabrication for GaAsP 1J devices, mesa isolation etches selectively to the GaInP etch stop layer. Then this GaInP layer is selectively etched to reveal the GaAsP LCL. Then *p*-contact is made to the GaAsP LCL. The layer structure for GaAsP/Si 2J devices with AlGaAsP BSF + spacer replaces the GaInP etch stop, GaAsP LCL, and GaAsP cap for heating layers with low T_{growth} AlGaAsP/GaAs/GaAsP layers for the TJ; also buffer layers are changed to *n*-type doping for the 2J structure. GaAsP/Si 2J devices have top-bottom metal fabrication with mesa isolation stopping within the CGB.
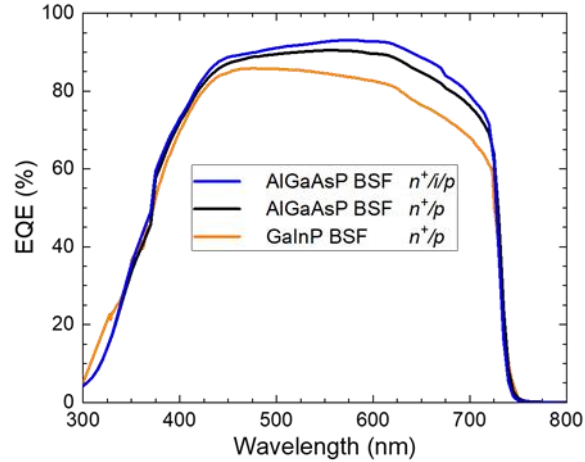
Fig. 7.7: EQE comparison of ~1.7 eV GaAsP 1J solar cells with different BSF design (GaInP BSF from Fig. 7.3(d) vs AlGaAsP BSF + spacer from Fig. 7.3(f)) or different junction design (n^+/p vs $n^+/i/p$). All samples compared here have similar absorber thickness. Adapted from [21].

lattice matching (slight difference in lattice constant due to x_{Al}, analogous to GaAs/AlGaAs). In addition, the 500 nm GaAsP spacer layer was included to increase separation between the top cell and the defect-ridden CGB. If DLDs result from misfit dislocation bundles in the CGB, then the spacer layer may reduce the influence of bundles on the active region.

I observed a reduction in back surface DLDs when replacing the GaInP BSF structure with the AlGaAsP BSF + spacer structure [21]. As shown in Fig. 7.6(a, d), EBIC at 12 kV probing near the back surface of the top cell showed strongly reduced thick DLD density by a factor of ~3. In fact, DLD density decreased even with reduced CGB thickness – ~2.8 μm, -1.04%/μm for the AlGaAsP BSF + spacer device; ~3.8 μm, -0.77%/μm for the GaInP BSF device – that would be expected to increase DLD density [138]. Due to decreased CGB thickness to lessen thermal cracking, TDD increased from 5.3×10^6 cm^{-2} for the GaInP BSF device to 7.5×10^6 cm^{-2} for the AlGaAsP BSF + spacer device. Even so, Fan and I found significant long-wavelength current collection improvement (> 1 mA/cm^2 higher, Fig. 7.7, black) as the effect of back surface DLD reduction was more beneficial than the effect of increased TDD. These results indicate the Lee

group's GaAsP solar cells have consistently suffered from DLDs siphoning carriers from the back side of the solar cell.

Fan also implemented an $n^+/i/p$ junction design with ~325 nm intrinsic layer to lengthen the depletion region [21]. The $n^+/i/p$ design enhanced long-wavelength EQE (Fig. 7.7, blue), as photons absorbed deeper in the absorber had increased probability of reaching the depletion region. With advancements from the AlGaAsP BSF + spacer and $n^+/i/p$ designs, Fan and I obtained ~1.7 eV GaAsP 1J solar cell AM1.5G efficiencies ranging from 16.6% to 17.6% on Si [21]. To further advance GaAsP top cells, TDD reduction and device optimization are both needed. Challenges remain for further DLD reduction, as both front and back surface DLDs are still present. Initial attempts to switch from an AlInP window layer to an AlGaAsP-based structure did not reduce front side DLD density but increased parasitic absorption.

7.3   GaAsP/Si Dual-Junction (2J) Solar Cell Improvement

After improving the GaAsP top cell efficiency, Fan applied changes to the GaAsP/Si 2J solar cells increasing AM1.5G efficiency from 20.0% to 21.5% (in-house measurement). However, these solar cells were suboptimal as the extra thickness from the GaAsP spacer led to cracking during processing and as faulty source materials and chemicals caused subpar ARC and poor backside texturing of Si. In response, CGB thickness was reduced from ~3.8 μm to ~2.8 μm resulting in slightly higher TDD as mentioned above but greatly reduced cracking. With the improved solar cell design, close current matching, and successful fabrication, Fan and I achieved GaAsP/Si 2J solar cell efficiencies up to 25.0% (in-house measurement) [21]. Though not certified and small area, Fan verified device measurements using two separate solar simulator measurement setups. This is the highest reported GaAsP/Si 2J efficiency to date, greater than the current larger-
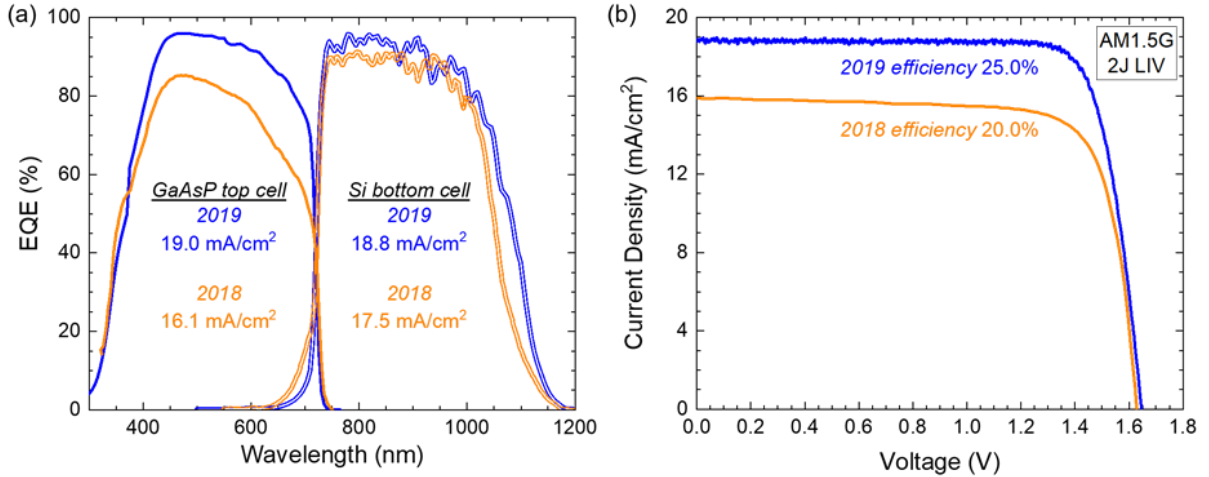
Fig. 7.8: Comparison of GaAsP/Si 2J solar cell (a) EQE and (b) approximate 1-sun AM1.5G LIV of hero devices from 2018 cells [52] and 2019 cells [21]. Adapted from [21].

area certified AM1.5G record of 23.4% [14], [51]; the highest epitaxial III-V/Si multi-junction solar cell has large-area certified record of 25.9% with GaInP/GaAs/Si [22].

Fig. 7.8 compares device performance between the 20.0% (2018, orange [52]) and 25.0% (2019, blue [21]) efficiency results. The 2019 design increased carrier collection for both sub-cells achieving higher current and better current matching. Back side texturing of Si increased Si bottom cell EQE while utilization of AlGaAsP BSF + spacer design, $n^+/i/p$ junction, and reduced n-doping of GaAs$_y$P$_{1-y}$/GaP buffer layers strongly increased GaAsP top cell EQE. The 2019 design was slightly current-limited by the Si bottom cell even with slightly higher GaAsP E_G for 2019 (1.71 eV) than for 2018 (1.69 eV). Improved carrier collection in particular for GaAsP was critical to the achieved efficiency improvement. While the $n^+/i/p$ design causes lower V_{OC} – typically around 20 – 40 mV lower when tested in GaAsP 1J cells – due to higher dark current contribution from a wider depletion region, the resulting increase in J_{SC} benefits GaAsP/Si 2J devices more. Increased GaAsP current collection shifts the GaAsP E_G for current matching higher, such that the Si bottom cell receives more of the incident light.

7.4   Chapter Findings

Primary findings in this chapter are listed below:

- Electrically-active "dark line defects" (DLDs) have been observed with electron beam-induced current (EBIC) imaging for the Lee group's metamorphic GaAsP 1J solar cells with varied layer structures even including 2011 GaAsP 1Js using only $GaAs_yP_{1-y}$.

- Populations of DLDs are present in GaAsP top cells at either the front or back surface of the active region.

- Replacing the GaInP BSF layer to a structure with AlGaAsP BSF layer and GaAsP spacer layer reduced DLD density at the back surface.

- Switching to this "AlGaAsP BSF + spacer" design and from an $n+/p$ to $n+/i/p$ junction design improved long-wavelength carrier collection to enable high-current ~1.7 eV GaAsP sub-cells (~19 mA/cm^2 with 1-sun AM1.5G illumination).

- These top cell design changes enabled the highest reported 1-sun AM1.5G efficiency for GaAsP 1J solar cells on Si of 17.6%.

- Incorporating this top cell as well as structure and processing modifications to mitigate challenges from the GaAsP/Si 2J architecture enabled the highest reported 1-sun AM1.5G efficiency for GaAsP/Si 2J solar cells of 25.0%.

CHAPTER 8

SPACE TESTING OF GAASP TOP CELLS

High specific power and low cost are crucial for increasing the cost competitiveness of solar energy in the terrestrial market and enabling a greater variety of space missions. Previous experiments and discussion in this dissertation focused on material characterization and device testing for terrestrial conditions (at room temperature, 1-sun AM1.5G solar spectrum). However, ~1.7 eV/1.1 eV GaAsP/Si double-junction (2J) solar cells may also be promising for space applications due to the potential combination of high efficiency and low cost: 34% – 40% calculated efficiency potential for AM0 [10], [11] and a low-cost, large-area, and high-volume Si substrate. Besides high efficiency, low cost, low weight, and low volume, understanding the reliability of solar cells under harsh space environments is critical such that the solar cells utilized supply sufficient power throughout the mission. Depending on the mission trajectory, the solar cell will experience a unique set of environments including differing levels of particle irradiation, high or low temperatures, thermal swings, and other factors such as particulates or reactive atomic oxygen. While ~1.7 eV GaAsP has received considerable attention for III-V/Si applications [14], [21], [34], [41], [51], [52], limited studies of these effects on GaAsP solar cells currently exist in the literature [44], [63], [64], [150]. In this chapter, I first describe electron irradiation experiments performed on metamorphic ~1.7 eV GaAsP single-junction (1J) top cells demonstrating promising radiation hardness [150]. Later in the chapter, I describe measurements of temperature-dependent device performance for GaAsP top cells on Si.[26]

8.1 Space Testing Background

Solar cells in space receive different spectral illumination than on Earth's surface as the Earth's atmosphere filters some of the incoming photon energies more favorably than others. Space solar cells are tested with the unfiltered Air Mass Zero (AM0) spectrum, while terrestrial solar cells are tested with the filtered Air Mass 1.5 spectra (either AM1.5D for direct normal irradiance or AM1.5G for global total). The air mass number indicates the reduction of the incoming spectrum by the atmosphere's spectral absorbance. Total solar irradiance at 1 AU (mean distance between Earth and Sun) is higher for AM0 than for AM1.5G or AM1.5D (Fig. 8.1).

High energy charged particles (electrons, protons, and ions) from the solar wind, solar flares, and galactic cosmic rays contribute to the radiation environment in space. The interaction of charged particles and a planetary magnetic field results in a trapped radiation environment with varying concentrations and energies of each particle type around the planet. For Earth, the zones of high particle concentration are called the Van Allen belts. Inner portions of the Van Allen belts mainly consist of protons and lower energy electrons, while the outer portion primarily consists of higher energy electrons. The particle spectrum observed for each mission will vary depending on
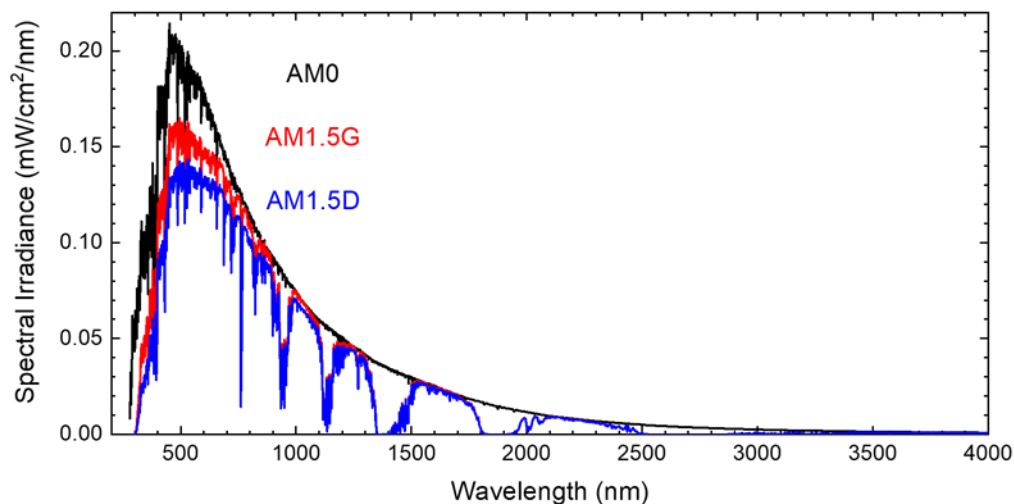
Fig. 8.1: Standard reference spectra for AM0, AM1.5G, and AM1.5D. From ASTM G-173-03.

the trajectory taken and can be predicted though with significant uncertainty due to variations in solar wind intensity and solar flare activity.

Charged particles transfer energy to a solar cell material through collisions that slow the particles and damage the material. Inelastic collisions with the material's electron cloud can cause ionization events that promote electrons to higher energy levels. Ionization events are primarily responsible for most energy transfer to a material but minimally affect solar cell performance. Elastic collisions are nonionizing events that displace atoms in the material; this is called displacement damage. Displacement damage leads to most solar cell performance degradation from particle irradiation, as atoms displaced from lattice sites create point defects. Generated point defects are often mid-gap states that can reduce minority carrier diffusion length by increasing non-radiative recombination or can compensate doping [151]–[153].

Performance degradation of solar cells under particle irradiation in space depends on a variety of factors including particle type/energy/fluence, solar cell materials/design, and shielding. Due to a higher scattering cross section, protons are significantly more damaging than electrons. In addition, damage from electrons increases with increasing incident energy, while damage from protons increases with decreasing incident energy. Each solar cell material degrades at different rates dependent on the ease of creating displacement damage, the resulting defect levels, and the material's ability to tolerate these defects; more radiation hard materials are affected less by particle irradiation [154]. Solar cell design parameters such as the layer thicknesses, doping concentrations, and number of junctions can affect radiation hardness (also called radiation resistance). Optimizing the design can reduce the effects of performance degradation from shortened diffusion length and majority carrier removal, though often with tradeoffs [155]. Additionally, shielding choice such as the cover-glass (front-side) or support structure (back-side)

can lessen the effect of particle irradiation by slowing down incident particles and possibly stopping some particle energies such as less energetic protons [153], [156].

The space radiation environment consists of particles with a spectrum of energies that interact omnidirectionally with a solar cell. Space testing under real conditions is time-consuming, so accelerated ground testing of unshielded solar cells is commonly performed using a unidirectional, monoenergetic particle beam incident normal on the solar cell. Modeling can predict the expected behavior of solar cells in space conditions and with shielding following ground testing at one or multiple particle type/energy choices depending on the modeling approach [151], [157]. Historically, the most common particle choice to study solar cell degradation is 1 MeV electrons investigated as a function of electron fluence. For a single comparative fluence of 1 MeV electrons, 1×10^{15} e/cm^2 is the most common and mimics the total displacement damage a solar cell would encounter during a 15-year mission in geostationary orbit [44], [153].

As shown in Fig. 8.2(a), III-V solar cells typically have good radiation hardness with remaining factor (RF, ratio of performance after vs before irradiation) for efficiency often > 0.80 with 1 MeV electron fluence of 1×10^{15} e/cm^2 [58]. In addition, investigations have shown higher
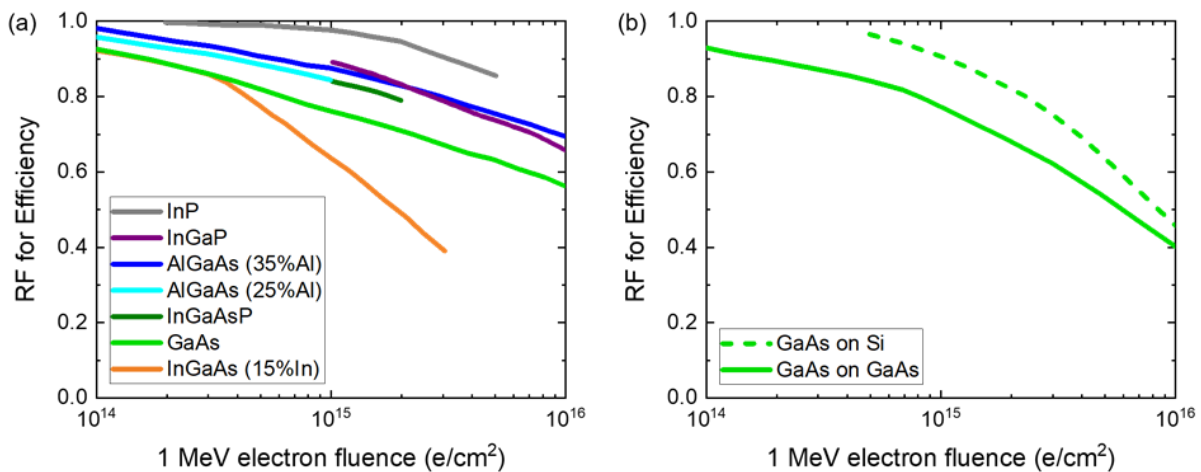
Fig. 8.2: Remaining factor for efficiency as a function of 1 MeV electron fluence (a) showing data for a variety of III-V 1J solar cells and (b) comparing GaAs solar cells grown on GaAs or on Si. In$_{0.49}$Ga$_{0.51}$P and In$_{0.32}$Ga$_{0.68}$As$_{0.34}$P$_{0.66}$ (~1.76 eV) in (a) were both grown lattice-matched to GaAs. Adapted from (a) Ref. [58] and (b) Ref. [61].

radiation hardness for metamorphic GaAs on Si than for GaAs homoepitaxially grown on GaAs (Fig. 8.2(b)) [59], [61], [62]. Metamorphic materials with significant threading dislocation density (TDD) begin with lower minority carrier diffusion lengths, so additional defects from particle irradiation reduce the diffusion length at a lower rate than high-quality starting materials. Taken together, these results imply the possibility that metamorphic GaAsP solar cells on Si could have high radiation resistance.

Before this work [150], literature included two investigations of the radiation hardness of metamorphic GaAs$_y$P$_{1-y}$ solar cells. Carlin *et al.* performed 10 MeV proton irradiation up to 2.7×10^{12} p/cm^2 (equivalent to ~6×10^{14} e/cm^2 of 1 MeV electrons) for ~1.55 eV GaAsP 1J cells on Si$_x$Ge$_{1-x}$ graded buffers on Si with TDD of ~3×10^6 cm^{-2} [63]. Carlin observed comparable radiation hardness for ~1.55 eV GaAsP to lattice-matched III-V solar cells with a remaining factor for efficiency of 0.86 [63]. Previously in the Lee group, Vaisman performed an electron irradiation study for ~1.7 eV GaAsP top cells with 1 MeV electrons to 1×10^{15} e/cm^{-2} fluence [44]. Vaisman compared GaAsP grown on GaP or GaP/Si (design from Ref. [34] with TDD ~$2 - 6 \times 10^6$ cm^{-2}) as well as against GaAs solar cells grown on Si (TDD ~3×10^7 cm^{-2}) or GaAs. The ~1.7 eV GaAsP 1J cells were more radiation hard than the GaAs cells on Si with RF for efficiency of $0.85 - 0.96$ vs 0.81 [44]. However, the reported spread in results for the GaAsP cells makes it challenging to compare against the best literature results with 1 MeV electrons to 1×10^{15} e/cm^{-2} fluence for GaAs cells on GaAs (0.849 RF for efficiency [158]) or on Si (0.905 RF for efficiency [61]), though RF for efficiency averaging 0.91 is promising for metamorphic GaAsP.

In space the temperatures observed by a solar cell depend on how a mission's trajectory or orbit affects the incident illumination. Incident illumination primarily provides heating to a solar cell based on the intensity and duration of illumination. Solar cells in orbit reach the lowest

temperatures during eclipse and the highest temperatures during illumination, going through thousands of thermal cycles during a mission's lifetime. Similarly, missions traveling closer to the sun receive higher intensity illumination and average higher temperatures than missions farther from the sun [156].

Besides possible damage to the solar cell from extreme temperatures or thermal cycling, increasing temperature decreases solar cell performance. Semiconductor bandgaps (E_G) decrease with increasing temperature (T) approximately following the Varshni equation: $E_G(T) = E_G(0 \ K) - \frac{\alpha T^2}{T+\beta}$ where α and β are material-specific constants. While higher operating temperature causes higher short circuit current density (J_{SC}) from bandgap reduction, the open circuit voltage (V_{OC}) suffers more strongly with increased temperature from a combination of bandgap reduction and increased dark current, overall decreasing efficiency. Dark saturation currents increase roughly exponentially with temperature due to dependences on intrinsic carrier concentration [159].

The changes in solar cell performance with temperature are described with temperature coefficients of the figures of merit. Temperature coefficients are commonly stated normalized against the performance at 25 °C such that a temperature coefficient is calculated by $\frac{1}{X(25 \ °C)}\frac{dX}{dT}$ where X is the figure of merit of interest such as the power density at max power point (P_{MPP}). Most solar cell materials have roughly constant temperature coefficients within ±100 °C [156]. Previously, Boyer *et al.* investigated the temperature-dependent behavior for lighted current-voltage (LIV) measurements of a GaAsP/Si 2J solar cell current limited by Si obtaining normalized (absolute) temperature coefficients of -2.2×10^{-3} K^{-1} (-3.8 mV/K) for V_{OC}, $+7.0 \times 10^{-4}$ K^{-1} (+0.013 mA/cm^2/K) for J_{SC}, and -2.9×10^{-3} K^{-1} (-0.071 mW/cm^2/K) for P_{MPP} [64].

8.2   Electron Irradiation Experiment

In this section, I detail 1 MeV electron irradiation experiments for ~1.7 eV GaAsP 1J solar cells, testing the effects of junction polarity, base thickness (t_{Base}), and TDD on radiation hardness [150]. All samples in this study were grown by molecular beam epitaxy (MBE) and fabricated into devices without anti-reflection coating (ARC), as described previously by Lang *et al.* [47]. Growth was performed on either pieces of 2" bulk GaP (001) substrates or of 2" GaP/Si templates ($NAsP_{III/V}$ GmbH, similar to [95]) consisting of a ~40 nm GaP nucleation layer on Si (001) offcut 6° toward (111). Fig. 8.3(a) shows the schematic layer structure for a fabricated solar cell including a nominally lattice-matched InGaP window layer, a GaAsP emitter, base, and doping back surface field (BSF) on top of a $GaAs_yP_{1-y}$ step-graded buffer and GaP buffer layer. Dopant concentration was graded from 2×10^{18} cm^{-3} at the end of the graded buffer to 1×10^{17} cm^{-3} at the start of the base to form the GaAsP doping BSF. Several solar cell design variants, as listed in Fig. 8.3(b), were investigated in this study to directly compare against the control (variant 1) for the effects of TDD (variant 2, co-grown with variant 1), base thickness (variant 3), and junction polarity (variant
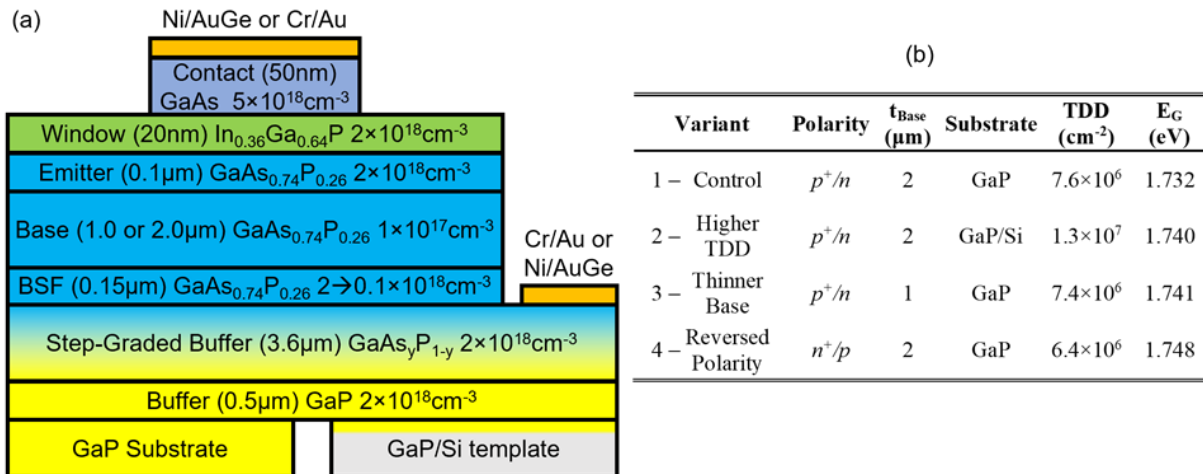
Fig. 8.3: GaAsP 1J solar cell sample summary for this study. (a) Schematic layer structure for fabricated GaAsP solar cells; no ARC was applied. Dopant concentrations are shown, and the dopant atom (Si for *n*-type, or Be for *p*-type) used for each layer depends on junction polarity. Ni/AuGe (Cr/Au) metal contacted *n*-type (*p*-type) material. (b) Solar cell design variants tested for comparisons of effects of TDD, base thickness, and junction polarity. The TDD was estimated by electron beam-induced current (EBIC) images [47]. Adapted from this work, Ref. [150].

4). As these solar cells were stored in air and room light for over six years, each sample was retested to ensure only minor performance loss and to obtain a set of measurements before irradiation [150].

Uncoated solar cells were irradiated at the NEO Beam facility (partnership between Mercury Plastics, Inc. and Kent State University; assisted by R. M. Uribe [160]–[162]) at room temperature with 1 MeV electrons to a fluence of 1×10^{15} e/cm^2. Device performance characterization was determined before (beginning-of-life, BOL) and after electron irradiation (end-of-life, EOL) by external/internal quantum efficiency (EQE/IQE), dark/lighted current-voltage (DIV/LIV), and Suns-V_{OC} measurements [150]. EQE and reflectance measurements were performed in a PV Measurements QEX7 system to calculate IQE and bandgap. AM0 LIV measurements were performed at NASA Glenn Research Center on their custom triple source AM0 solar simulator, including a Spectrolab X-25 and filtered and unfiltered tungsten halogen lamps [75]. AM0-calibrated [163], [164] SolAero ZTJ isotype cells were used to calibrate the three sources for approximate 1-sun AM0 illumination.

Fig. 8.4(a) compares the BOL LIV under AM0 illumination for the best device of each variant; Fig. 8.4(b) tabulates values for the figures of merit including V_{OC}, bandgap-voltage offset ($W_{OC} = E_G/q - V_{OC}$), J_{SC}, fill factor (FF), and AM0 efficiency. Samples on GaP substrates had W_{OC} of 0.57 V – 0.58 V, while the sample on the GaP/Si template had a higher W_{OC} of 0.63 V due to its higher TDD [150]. In comparison to variant 1, J_{SC} decreased due to reduced long-wavelength collection for either a higher TDD (variant 2) due to lower minority carrier diffusion length, or a thinner base (variant 3) due to incomplete absorption. Though J_{SC} was improved for reversed polarity to n^+/p (variant4) in comparison to any p^+/n variant, variant 4 had lower BOL efficiency than variant 1 due to poor fill factor, which will be discussed in detail below.
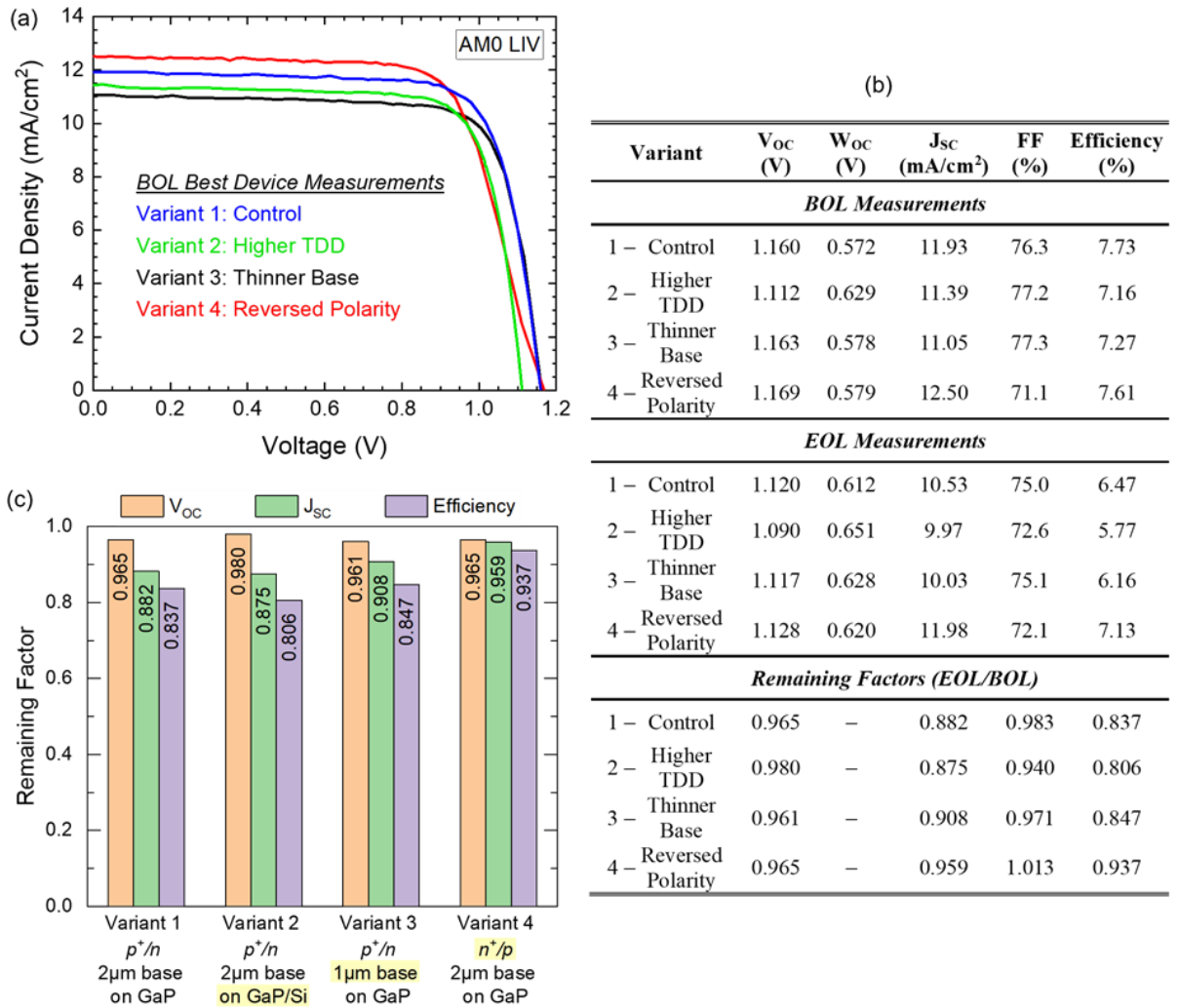
Fig. 8.4: 1-sun AM0 LIV characterization and performance of best GaAsP solar cell devices for each variant before and after 1 MeV electron irradiation to 1×10^{15} e/cm². (a) Comparison of BOL LIV for variants 1 – 4. (b) Tabulated figures of merit from LIV before and after irradiation and the resulting remaining factors. (c) Plotted remaining factors for figures of merit. The highlighted text indicates the difference from variant 1. Adapted from this work, Ref. [150].

Variant	V_{OC} (V)	W_{OC} (V)	J_{SC} (mA/cm²)	FF (%)	Efficiency (%)
BOL Measurements					
1 – Control	1.160	0.572	11.93	76.3	7.73
2 – Higher TDD	1.112	0.629	11.39	77.2	7.16
3 – Thinner Base	1.163	0.578	11.05	77.3	7.27
4 – Reversed Polarity	1.169	0.579	12.50	71.1	7.61
EOL Measurements					
1 – Control	1.120	0.612	10.53	75.0	6.47
2 – Higher TDD	1.090	0.651	9.97	72.6	5.77
3 – Thinner Base	1.117	0.628	10.03	75.1	6.16
4 – Reversed Polarity	1.128	0.620	11.98	72.1	7.13
Remaining Factors (EOL/BOL)					
1 – Control	0.965	–	0.882	0.983	0.837
2 – Higher TDD	0.980	–	0.875	0.940	0.806
3 – Thinner Base	0.961	–	0.908	0.971	0.847
4 – Reversed Polarity	0.965	–	0.959	1.013	0.937

Remaining factors after 1 MeV electron irradiation with 1×10^{15} e/cm² fluence are compared in Fig. 8.4(c) for each variant tested, showing that performance degradation from irradiation resulted primarily from reduced J_{SC} [150]. Fig. 8.4(b) also includes values of EOL and RF for each figure of merit and each variant. Consistent with earlier studies having high base doping in the low 10^{17} cm^{-3} range [155], the relative loss in V_{OC} was considerably less than the relative loss in J_{SC}. While for low base doping, the carrier concentration is significantly

compensated by point defects introduced as radiation damage and leads to larger depletion width and therefore more V_{OC} loss than J_{SC} loss, high base doping is minimally affected by compensation [155]. Instead for high base doping, the major effect of radiation damage is shortened minority carrier diffusion length from more defective material. With shorter diffusion length, carrier collection far from the junction is poor, and as expected, variant 3 with a thinner 1 μm base had higher RF for J_{SC}. With a higher TDD, variant 2 showed less V_{OC} degradation as the added point defects from irradiation influenced the overall defect density less, lowering V_{OC} by ~20 mV on GaP/Si as opposed to ~40 mV for the lower TDD on GaP [150].

The n^+/p variant 4 had superior radiation hardness to the p^+/n variant 1 due to the longer minority carrier diffusion length of electrons over holes in the respective base regions [150]. Similar to GaAs, electron diffusivities in ~1.7 eV GaAsP are estimated to be ~11 – 13 × higher than hole diffusivities [165]. IQE comparison between the p^+/n and n^+/p designs in Fig. 8.5(a) showed that the p^+/n variant 1 had higher short-wavelength IQE, while the n^+/p variant 4 had higher long-wavelength IQE. Ultimately, the n^+/p design was more radiation hard than the p^+/n design due to the higher minority electron diffusivity in the thick p-GaAsP base. With smaller J_{SC}
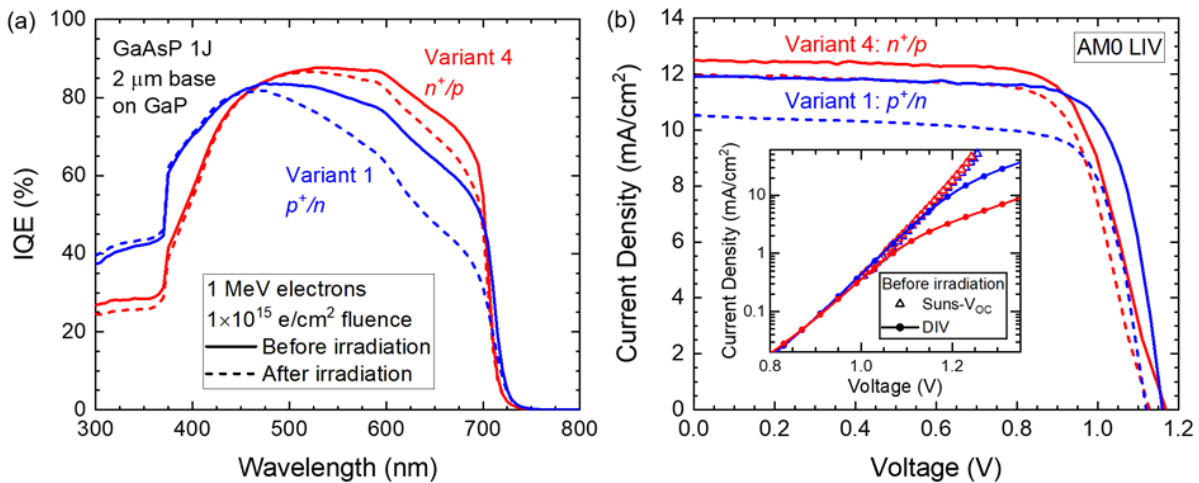
Fig. 8.5: Best device performance for variant 1 and variant 4 to compare reversed junction polarity. Comparison of BOL and EOL (a) IQE and (b) 1-sun AM0 LIV. DIV and Suns-V_{OC} for these two samples at BOL are inset in (b). Adapted from this work, Ref. [150].

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degradation, the n^+/p variant 4 achieved the highest EOL efficiency among the samples tested with 7.13% efficiency under AM0 illumination as compared to 6.47% for the p^+/n variant 1 [150]. However, as mentioned earlier, variant 4 suffered from low FF (71% – 72% versus 75% – 76%) as shown in the comparison of BOL and EOL LIV (Fig. 8.5(b)). Analysis of DIV and Suns-V_{OC} (inset Fig. 8.5(b)) showed the major cause of poor FF for variant 4 to be high series resistance, due to high contact resistance. For the n^+/p variant 4, DIV bends over due to series resistance at about an order of magnitude lower current density, indicating nearly $10 \times$ higher series resistance and leading to a reduced max power point voltage for LIV [150].

The n^+/p junction polarity demonstrated very good radiation hardness with a RF for efficiency of 0.937 after 1 MeV electron irradiation to 1×10^{15} e/cm^2 fluence for the best performing device [150]. Devices tested in this work for n^+/p variant 4 averaged RF for efficiency of 0.93 ± 0.04. This RF is similar to Vaisman's study having RF for efficiency of 0.91 ± 0.03 on average [44]. Devices tested by Vaisman also utilized a n^+/p design though with a reduced base thickness of $1 – 1.5$ μm and improved barrier layer choices [34], [44]. These results for metamorphic ~1.7 eV GaAsP compare favorably against the highest-reported RF for efficiency
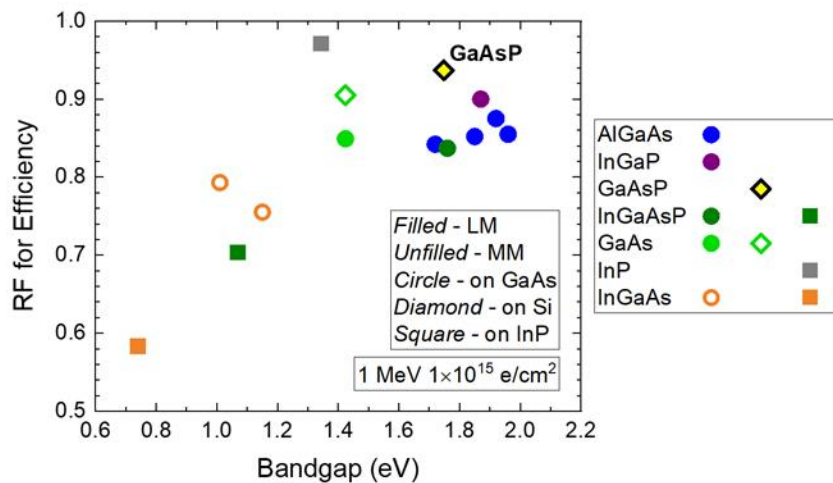
Fig. 8.6: Highest reported remaining factor for efficiency (1 MeV, 1×10^{15} e/cm^2) for III-V 1J solar cells plotted against bandgap. Filled data points were lattice-matched (LM) layers, and unfilled data points were metamorphic (MM) layers. Substrate is indicated by shape. Data from Ref. [58], [61], [150], [158], [166], [167].

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values (1 MeV, 1×10^{15} e/cm^2 fluence) for III-V 1J solar cells in literature, to the best of my knowledge (Fig. 8.6) [58], [61], [150], [158], [166], [167]. While metamorphic GaAsP does not match the exceptional radiation hardness of InP, GaAsP has the highest RF for efficiency among wide-bandgap III-V materials, exceeding those of AlGaAs and InGaP. The high TDD for GaAsP likely contributes to GaAsP's higher radiation hardness similar to how GaAs solar cells metamorphically grown on Si have higher radiation hardness than those homoepitaxially grown on GaAs [59], [61], [62]. Even so, metamorphic GaAsP in this work achieved higher RF for efficiency than metamorphic GaAs, possibly due to the increased bandgap or phosphorous content of ~1.7 eV GaAsP.

8.3 Temperature-dependent Device Performance

In this section, I detail temperature-dependent device measurements for a ~1.7 eV GaAsP 1J solar cell grown on Si. For these measurements, an additional solar cell device fabrication was performed for the GaAsP 1J sample studied in Chapter 6.4 and grown on unintentionally-doped (UID) GaAs$_y$P$_{1-y}$/GaP buffers. In short, this structure included a TiO$_2$/SiO$_2$ double layer ARC, n^+-AlInP window layer, n^+/i/p GaAsP active region, and p^+-AlGaAsP (28.5% Al) BSF on p^+-GaAsP spacer layer. Further specifics on the growth structure and fabrication can be found in Chapter 7.1, Chapter 7.2, and Ref. [21], [127]. Electron beam-induced current (EBIC) measurements gave an estimated TDD of 9.5 ($\pm$1.4) $\times 10^6$ cm^{-2} for the ~1.7 eV GaAsP 1J top cell [127].

Device measurements were performed within a Linkam HFS600E-PB4 temperature and environmental control stage. The Linkam stage was used in combination with Linkam T95 system controller and LNP95 liquid nitrogen pump and dewar to control the stage temperature using thermocouple, resistive heating, and liquid nitrogen cooling; this Linkam setup can enable electrical measurement ranging from -195 °C to +600 °C [168]. Device measurements in this study

ranged from -100 °C to +140 °C to cover the expected temperature range for low Earth orbit [64]. The Linkam stage chamber was purged with N_2 gas and left sealed with N_2 ambient to prevent water condensation at low temperatures. Measurements began at +25 °C before cooling to -100 °C, then temperature increased in 20 °C steps to +140 °C before cooling back to +25 °C. An additional +25 °C measurement was taken both following heating from low temperature and following cooling from high temperature so +25 °C data could be compared before/after cooling to -100 °C and before/after heating to +140 °C. Stage temperature was held at each temperature for > 2 min prior to measurement to assist sample temperature stability.

Temperature-dependent EQE and LIV/DIV were measured utilizing separate cleaved devices from the same fabrication. The EQE device has a top ring contact with no grid fingers for simple expected J_{SC} calculations without metal coverage and then scaled for devices with metal grid coverage. EQE measurements were performed in a PV Measurements QEX7 system. I extracted bandgap from the long-wavelength cut-off at band edge. The Linkam stage window for incident illumination had non-unity transmission. I corrected for transmission loss by measuring
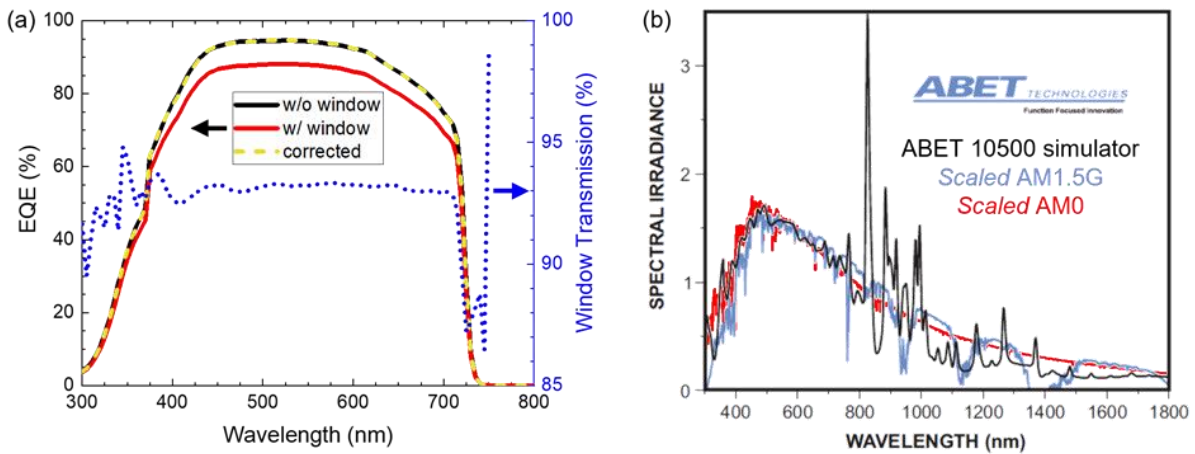
Fig. 8.7: (a) Window transmission loss correction for EQE with Linkam stage. Comparison of ~1.7 eV GaAsP 1J solar cell EQE without window (black), with window (red), and the with window data corrected with a constant for transmission loss (yellow dashed). Also shows window transmission as a function of wavelength (blue dotted); data not shown > 750 nm as EQE data noise causes continued oscillations as already shown at ~740 nm. (b) ABET 10500 solar simulator spectral irradiance compared against scaled AM1.5G and scaled AM0 spectra to demonstrate close spectral match for both standard spectra < 770 nm. Fig. 8.7(b) adapted from Ref. [21] supplemental.

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EQE at room temperature with and without the stage window installed; I found applying a constant transmission of ~93% estimated the window transmission across relevant wavelengths for ~1.7 eV GaAsP (Fig. 8.7(a)). The LIV/DIV device has a top T-contact with grid fingers to reduce series resistance losses; temperature-dependent LIV was performed prior to separate temperature-dependent DIV on the same device. Approximate 1-sun AM0 LIV measurements were performed under an ABET 10500 single-source solar simulator; the ABET simulator is rated as Class A spectral match for AM1.5G [21]. While the ABET simulator spectrum is infrared-rich, this spectrum matches closely to both AM0 and AM1.5G spectra for < 770 nm, the relevant range for ~1.71 eV GaAsP even after the bandgap shifts to ~1.65 eV at +140 °C. I set the solar simulator height to reach the expected integrated J_{SC} from +25 °C EQE after correcting for metal grid coverage, and then performed all temperature-dependent measurements with this height and device placement.

Fig. 8.8 shows temperature-dependent EQE results with changes primarily dominated by shifts in the Γ-valley bandgaps for $GaAs_{0.765}P_{0.235}$ active region and $Al_{0.655}In_{0.345}P$ window layer.[27] Fig. 8.8(b) compares the EQE-extracted GaAsP bandgap temperature dependence against that predicted from the Varshni equation,[28] observing similar dependence. However, at the most extreme temperatures tested the EQE-extracted bandgap indicated the device temperature was ~6 °C closer to room temperature – device at -94 °C (+134 °C) with stage at -100 °C (+140 °C). Likely this resulted from a temperature gradient between the sample stage and N_2 ambient as additional measurements at +140 °C up to 25 min after reaching temperature showed no change

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[27] GaAsP y_{As} determined from EQE-extracted bandgap at +25 °C and GaP and GaAs Γ-valley bandgap at +25 °C. AlInP x_{In} determined by lattice matching to the resulting GaAsP lattice constant. Bowing parameters were estimated as constant with temperature.

[28] All three bandgap valleys (Γ, X, Λ) for each binary of interest (GaAs, GaP, AlP, InP) were determined as a function of temperature based on associated Varshni parameters. Following, the temperature dependence of GaAsP and InAlP alloys of interest were determined by assuming the bowing parameters did not depend on temperature.

Fig. 8.8: Temperature-dependent EQE measurements of $GaAs_{0.765}P_{0.235}$ 1J solar cell with ARC ranging from -100 °C to +140 °C in 20 °C steps as well as specially noted +25 °C measurement. (a) EQE spectra and (b) EQE-extracted bandgap as a function of temperature and plotted against that predicted from the Varshni equation. GaAsP y_{As} determined from the EQE-extracted bandgap at +25 °C.

in bandgap as the device was already at steady state temperature by ~2 min. Most short-wavelength EQE changes, except the oddly-shaped decrease for +120 °C and +140 °C, was attributed to the changing $Al_{0.655}In_{0.345}P$ direct Γ-valley bandgap with temperature (Γ-valley ~2.90 eV, X-valley ~2.33 eV, Λ-valley ~2.99 eV at 25 °C). The extra short-wavelength EQE decrease for > 100 °C appears to be related to device degradation at high temperatures, as the EQE-integrated J_{SC} decreased by ~3.3% for measurements performed 20 min apart at +140 °C and by ~1.8% for +25 °C measurements compared before heating and after heating to +140 °C for 30 min. While the EQE shape was altered at +140 °C, the +25 °C measurement after heating returned to the same shape as +25 °C before heating; no change in EQE was observed after cooling to -100 °C. However, AM0 LIV measurements on a separate device with similar temperature treatment demonstrated < 1% J_{SC} degradation, indicating the high temperature degradation may be device dependent.

Fig. 8.9 displays the temperature-dependent 1-sun AM0 LIV curves and extracted device performance figures of merit, demonstrating that strong V_{OC} and fill factor losses overwhelm the

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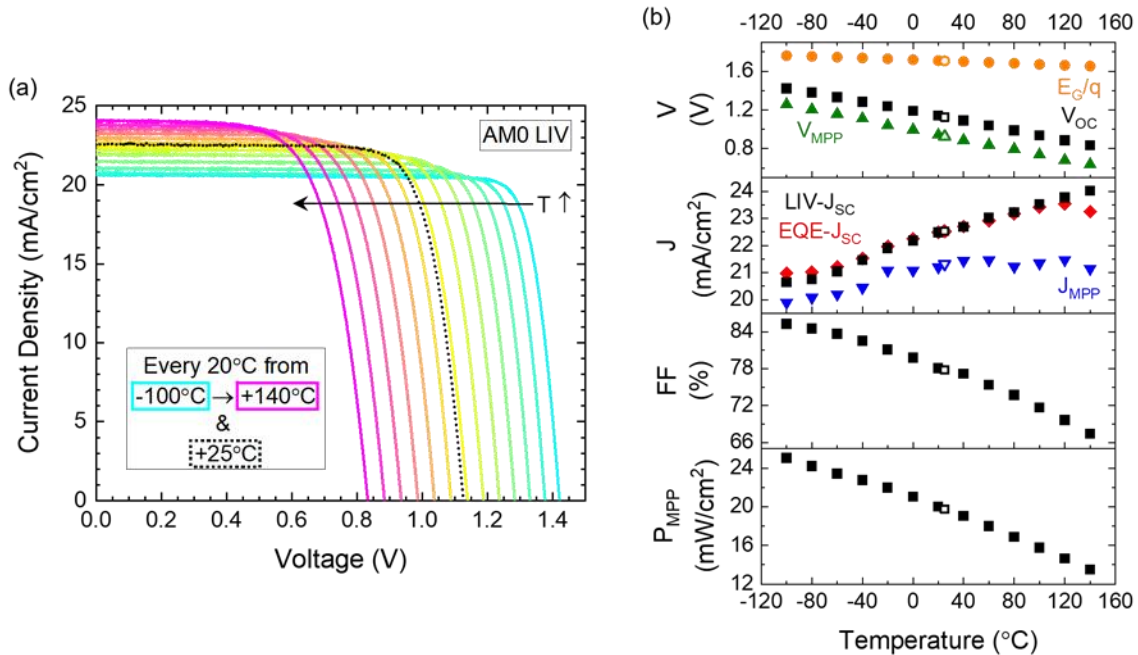
Fig. 8.9: Temperature-dependent 1-sun AM0 LIV measurements of $GaAs_{0.765}P_{0.235}$ 1J solar cell with ARC ranging from -100 °C to +140 °C in 20 °C steps as well as specially noted +25 °C measurement. (a) LIV curves and (b) LIV-extracted figures of merit (black squares; V_{OC}, J_{SC}, FF, P_{MPP}) as a function of temperature; V_{MPP} (green triangles) and J_{MPP} (blue triangles) are also shown. EQE-extracted E_G/q (orange circles) and EQE-integrated J_{SC} (red diamonds; accounting for metal grid coverage) are compared against V_{OC} and J_{SC} from LIV measurements. Additional abbreviations: current density (J), voltage (V).

J_{SC} gain, causing P_{MPP} to decrease with increasing temperature. As shown in Fig. 8.9(b, top panel), V_{OC} and V_{MPP} decreased more strongly with temperature than the bandgap energy due to the expected exponential rise in dark current (Fig. 8.10). Similarly, the higher dark current caused LIV curves at increasing temperature to be less "square" with lower fill factor (Fig. 8.9(b, middle panels)), resulting in roughly constant J_{MPP} above room temperature even with increasing J_{SC}. As mentioned in the previous paragraph, the J_{SC} from LIV measurements for this device only underwent slight J_{SC} degradation at the highest temperatures. Instead of lower J_{SC} at +140 °C than +120 °C like observed by EQE, J_{SC} from LIV continued increasing monotonically over the temperature range tested (Fig. 8.9(b, top middle panel)). 1-sun AM0 efficiency for this GaAsP 1J device ranged from 14.5% at +25 °C up to 18.3% at -100 °C and down to 9.9% at +140 °C; 1-sun AM1.5G efficiency of this device was ~16.0%. GaAsP 1J normalized (absolute) temperature
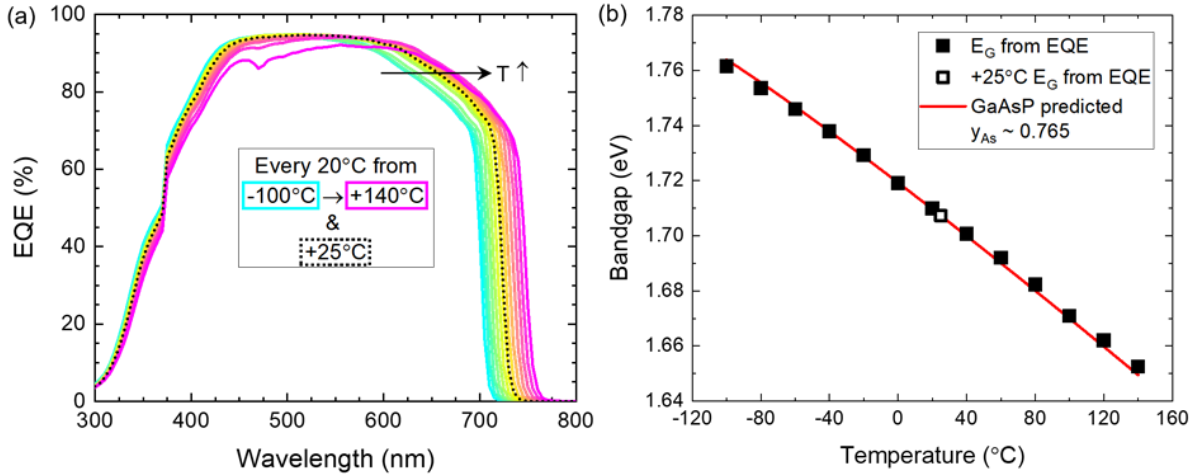
137
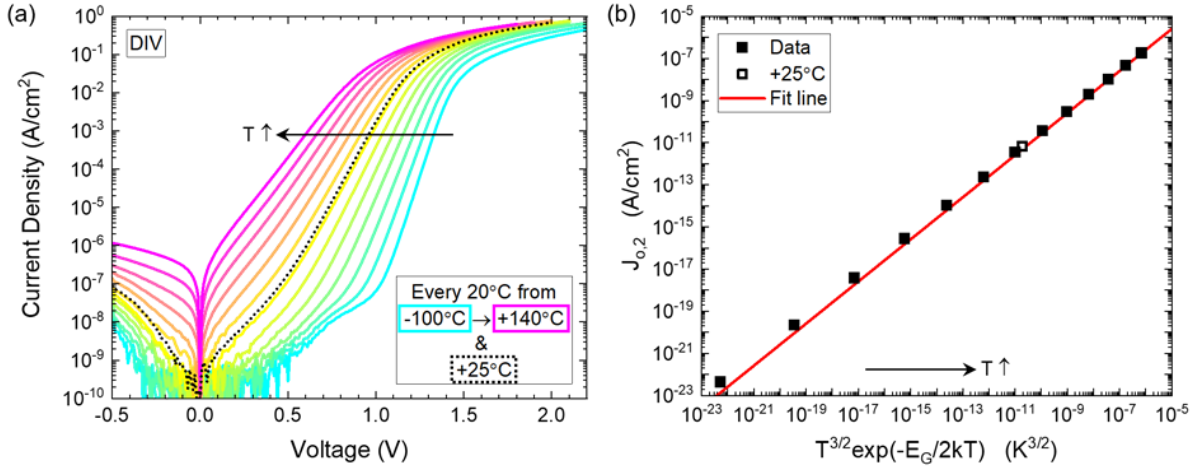
Fig. 8.10: Temperature-dependent DIV measurements of $GaAs_{0.765}P_{0.235}$ 1J solar cell with ARC ranging from -100 °C to +140 °C in 20 °C steps as well as specially noted +25 °C measurement. (a) DIV curves and (b) DIV-extracted J_{o2} against the expected temperature dependence. The linear fit is shown in a log-log plot to distribute data points more evenly.

coefficients obtained from this experiment included -2.2×10^{-3} K^{-1} (-2.5 mV/K) for V_{OC}, $+6.4 \times 10^{-4}$ K^{-1} (+0.014 mA/cm^2/K) for J_{SC}, and -2.5×10^{-3} K^{-1} (-0.049 mW/cm^2/K) for P_{MPP}, similar normalized coefficients to those found by Boyer *et al.* for a GaAsP/Si 2J [64].

Fig. 8.10 presents results from temperature-dependent DIV measurements showing behavior dominated by the change in dark current with temperature from a diode with ideality factor of ~2. For each curve, I calculated the dark saturation current density ($J_{o,n}$), ideality (n), and series resistance (R_S), finding consistent ideality of ~2 due to the large depletion region of the $n^+/i/p$ junction and TDD of $~1 \times 10^7$ cm^{-2}. With increasing temperature (T) the slope of log(J) vs V in the diode-dominated regime followed the expected n = 2 slope of q/2kT. As shown in Fig. 8.10(b), temperature dependence for $J_{o,2}$ agreed with that expected for an n = 2 diode, $J_{o,2}(T) \propto n_i(T) \propto T^{3/2}exp(-E_G/2kT)$ where n_i is the intrinsic carrier concentration [159]. The largest deviation from n = 2 behavior occurred at the lowest temperature, almost reaching n = 2.1 at -100 °C. Similarly, R_S remained mostly unchanged except below -40 °C where it increased with lower

temperature, to ~2 × higher at -100 °C. The higher R_S could result from freezing out majority carriers at lower temperatures in one or multiple layers, but this has not been investigated.

8.4 Chapter Findings

Primary findings in this chapter are listed below:

- Efficiency degradation from irradiation damage for metamorphic ~1.7 eV GaAsP solar cells dominated by reduced minority carrier diffusion length in the base such that designs with higher base diffusion length or thinner base were favored.

- Devices with n^+/p front junction polarity were the most radiation-hard devices tested, demonstrating promising remaining factor (RF) for efficiency of ~0.94 after 1×10^{15} e/cm^2 fluence of 1 MeV electrons.

- Average RF for efficiency of 0.93 ± 0.04 for n^+/p GaAsP is among the highest-reported RF for efficiency values for III-V 1J solar cells in literature, exceeding those of other wide-bandgap III-V materials and metamorphic GaAs.

- Temperature-dependent solar cell device measurement testing capabilities developed and used for -100 °C to +140 °C of ~1.7 eV $n^+/i/p$ GaAsP 1J solar cell on Si.

- Temperature effects followed expectations for bandgap changes of window/absorber, dark current, and device figures of merit.

- GaAsP 1J normalized (absolute) temperature coefficients were -2.2 × 10^{-3} K^{-1} (-2.5 mV/K) for V_{OC}, +6.4 × 10^{-4} K^{-1} (+0.014 mA/cm^2/K) for J_{SC}, and -2.5 × 10^{-3} K^{-1} (-0.049 mW/cm^2/K) for P_{MPP}.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

While epitaxial GaAsP/Si 2J solar cells have great potential, many challenges need to be addressed to realize high efficiency devices. Much of the limited performance for ~1.7 eV GaAsP top cells on Si stems from extended defects caused by crystal mismatches. This dissertation discusses results on investigation, management, and reduction of these defects in relaxed GaP and ~1.7 eV GaAsP grown by molecular beam epitaxy (MBE) on Si. In addition, results on improvement of GaAsP single-junction (1J) and GaAsP/Si double-junction (2J) solar cells as well as on testing of GaAsP 1J solar cells under simulated space environment conditions are presented. This chapter first provides a summary of the findings presented in this thesis. Following, I discuss ongoing or incomplete work for this project and propose potential future directions to further understand and improve GaAsP/Si 2J solar cells past the performance of Si 1J solar cells.

9.1   Conclusions

For relaxed GaP on Si, I first studied morphological defects and explored growth strategies to reduce defect densities. I improved etch pit size control for a defect selective etching (DSE) recipe and surveyed samples with multiple microscopy tools to enable study of larger ranges and inhomogeneity of threading dislocation density (TDD). Investigations of two heterogeneous features, trenches and dislocation pileups, revealed both features possess very high local threading dislocation density (TDD) on the order of 10^8 cm^{-2} and that nucleation of these dislocation-ridden features intensifies more strongly with increasing growth temperature (T_{growth}) than threading dislocations. Development of a two-step GaP growth design on thin GaP/Si templates suppressed nucleation of threading dislocations, trenches, and dislocation pileups to reduce the TDD of relaxed p-GaP on Si to the lowest reported value for GaP on Si, $1.0 - 1.1 \times 10^6$ cm^{-2}. The two-step growth design utilized an initial thin low T_{growth} step to suppress defect nucleation prior to high T_{growth} for increased dislocation glide velocities [36].

I observed strong effects from doping of relaxed GaP on Si with varied dopant type, species, and concentration. TDD values for p-type Be-doped and unintentionally-doped (UID) samples were essentially identical, however, TDD escalated with increasing n-type Si-doping to nearly 30 × higher, ~3.1×10^7 cm^{-2}. In addition, high n-type doping was found to cause increased surface roughness, anisotropic strain relaxation, and inhomogeneous TDD distributions from blocking of dislocation glide. TDD for varied dopant choices of each doping type – n-doped (Si, Te, and Si+Te), undoped (UID, compensated Si+Be), and p-doped (Be, C) – similarly followed the above trends based on electrical activity likely suggesting that increased free electron concentration plays a primary role in TDD escalation with increased n-type doping [65].

Following the above work and that of Boyer *et al.* [37], I designed and implemented strategies to reduce the high TDD of relaxed *n*-doped GaP on Si, the required buffer doping type for the preferred GaAsP/Si 2J architecture. I adapted a compressively strained superlattice (CSS) structure of GaAs$_y$P$_{1-y}$ and GaP for molecular beam epitaxy (MBE) growth of relaxed *n*-GaP on Si and observed TDD reduction by a factor of 8. Including low T$_{growth}$ *n*-GaP initiation on GaP/Si templates prior to high T$_{growth}$ of CSS and remaining *n*-GaP growth further reduced TDD to values achieved by Boyer [37]. Combining the CSS design and two-step design and lowering *n*-doping resulted in TDD of relaxed *n*-GaP on Si having the lowest reported value for *n*-GaP on Si, 1.54 (± 0.20) $\times 10^6$ cm^{-2}, nearing parity with *p*-GaP [65]. Using the improved *n*-GaP buffer design, I show similar TDD and device performance for ~1.7 eV GaAsP 1J solar cells on either *n*-doped or UID GaAs$_y$P$_{1-y}$/GaP buffer layers [127].

Next, I investigate "dark line defects" (DLDs) that have been observed by electron beam-induced current (EBIC) imaging from the Lee group's earliest GaAsP 1J device growths. I enhanced the Lee group's EBIC capabilities with varied accelerating voltage choice to adjust sampling depth, identifying populations of DLDs near either the front or back surface of the GaAsP active region. Switching from GaInP back surface field (BSF) layer to a structure with AlGaAsP BSF layer and GaAsP spacer layer reduced DLD density at the back surface. Both this design change and switching to an $n^+/i/p$ junction design improved long-wavelength carrier collection to enable high-current ~1.7 eV GaAsP sub-cells. New challenges from the GaAsP/Si 2J architecture were also mitigated to realize the highest reported AM1.5G efficiencies for both GaAsP/Si 2J and GaAsP 1J solar cells on Si, 25.0% and 17.6%, respectively [21].

Lastly, I studied the effects of simulated space conditions on ~1.7 eV GaAsP 1J solar cells to broaden the limited space testing literature for this metamorphic material. I performed electron

irradiation experiments on GaAsP solar cells comparing the effects of junction polarity, base thickness, and TDD on the degradation of solar cell performance under AM0 illumination. Efficiency degradation from irradiation damage was dominated by reduced minority carrier diffusion length in the base such that designs with higher base diffusion length or thinner base were favored. Accordingly, devices with n^+/p front junction polarity were the most radiation-hard devices tested, demonstrating promising remaining factor (value after irradiation divided by that before irradiation) of ~0.94 after 1×10^{15} e/cm^2 fluence of 1 MeV electrons [150]. Additionally, I developed the Lee group's capabilities for temperature-dependent measurements enabling solar cell device characterization from liquid nitrogen temperatures to 100s of °C. Following, I present temperature-dependent external quantum efficiency, ~1-sun AM0 lighted current-voltage, and dark current-voltage measurements and resulting temperature coefficients for ~1.7 eV GaAsP 1J solar cells on Si.

9.2   Ongoing and Future Directions

For GaP on Si, further understanding of trenches and dislocation pileups as well as the resulting effects on the following GaAs$_y$P$_{1-y}$ growth is of interest to determine strategies to reduce defect densities. P. Dhingra and I performed an initial study using cross-sectional transmission electron microscopy (XTEM) with a focused ion beam (FIB) cutout of a trench and found either multiple stacking faults or a microtwin extending from the GaP/Si interface to the bottom of the trench. In addition, dislocations appeared to be "pushed" one after another deeper into Si, up to nearly 400 nm, from this defect. These results are reminiscent to features observed in some tensile-strained materials such as tensile Si on Si$_{1-x}$Ge$_x$ virtual substrates [169] and tensile GaAs$_y$P$_{1-y}$ on GaAs [170]. However, it is unclear how trenches of compressive GaP on Si form and if high local densities of dislocations are caused by trenches or cause trenches, possibly by modifying lateral

mass transport at surface steps [171]. While cooldown of GaP on Si after growth causes tensile strain and trench density increases exponentially with T_{growth}, most samples are relaxed or slightly compressive at room temperature. Further analysis of relaxation of samples against trench densities may provide insight into the cause of trenches. In addition, thermal annealing under growth-like conditions followed by various cooldown rates could also reveal if the tensile strain during cooldown causes trenches.

In addition, the local creation/multiplication of threading dislocations during electron channeling contrast imaging (ECCI) of relaxed GaP on Si is not understood and possibly concerning. Capturing ECCI "movies" of this phenomenon *in-situ* could be helpful in aiding investigation. Also, the experiment to determine TDD vs distance from ECCI exposure in Chapter 3.2.2 could be repeated with different ECCI exposure conditions or samples. Factors such as accelerating voltage, channeling condition, beam current, or sample strain might affect the strength of this phenomenon.

Further optimization of the low T_{growth} initiation layer growth conditions may be able to push TDD of relaxed UID and *p*-doped GaP below 1×10^6 cm^{-2}. In addition, use of Al(Ga)P and/or optimization of deoxidation conditions for GaP/Si templates before growth could be investigated in an attempt to modify dislocation nucleation rates. For relaxed *n*-GaP on Si, there is almost too large of a parameter space to explore with the two-step with CSS design though this dissertation and Boyer's dissertation [86] test some simple variables. My initial suggestion would be to adjust high T_{growth} for both the CSS and GaP overlayer to higher T_{growth} to improve dislocation glide velocities. Also, the low T_{growth} initiation layer growth conditions and thickness (I suggest thicker low T_{growth} layer) for *n*-GaP have not been optimized, but were just tested at one condition/thickness choice.

While *p*-type GaAs$_y$P$_{1-y}$ compositionally-graded buffer (CGB) layers were previously optimized by Nay Yaung *et al.* [34], no such optimization has been performed in the Lee group for the thinned *n*-type CGB layers needed for GaAsP/Si 2J solar cells. Again, T$_{growth}$ would be my first suggested growth parameter to investigate, in particular for higher T$_{growth}$. With reduced TDD for *n*-GaP on Si of 2.4 ($\pm$0.4) $\times$ 10^6 cm^{-2}, Boyer *et al.* demonstrated only a small TDD increase to 3.0 ($\pm$0.6) $\times$ 10^6 cm^{-2} for *n*-GaAsP CGB layers at 675 °C – 725 °C (-1.0%/µm grading rate) to ~1.7 eV GaAsP on this *n*-GaP on Si using metalorganic vapor phase epitaxy (MOVPE) [37]. However, I showed an increase in TDD from 1.54 ($\pm$0.20) $\times$ 10^6 cm^{-2} to 9.5 ($\pm$0.4) $\times$ 10^6 cm^{-2} for GaP and ~1.7 eV GaAsP on *n*-type buffers using 600 °C (-1.04%/µm grading rate) CGB layers. The large TDD contribution from the CGB for my work (~8 $\times$ 10^6 cm^{-2}!) requires additional optimization and design strategies to reduce TDD and improve GaAsP top cell open-circuit voltage (V$_{OC}$).

Additionally, I wanted to but never was able to investigate the evolution of TDD throughout the CGB to help determine what y$_{As}$ regions of the CGB would be best to optimize. Omega broadening trends for high-resolution x-ray diffraction (HRXRD) reciprocal space mapping (RSM) measurements of CGBs may indicate that either the V/III ratio or indirect-to-direct bandgap (E$_G$) transition affects the TDD evolution in the CGB. A common trend is for omega to broaden with increasing y$_{As}$ up to around 0.6, which is where the GaAs$_y$P$_{1-y}$ calibration is switched from high to low V/III ratio curves (high P flux vs low P flux), and then remain roughly constant or decrease slightly. This may suggest the TDD increase occurs up to around y$_{As}$ ~ 0.6 and layers with y$_{As}$ < 0.6 need more optimization than other layers.

The origin of dark line defects in EBIC of GaAsP solar cells is also of interest. Similar to trenches, XTEM studies of FIB cutouts comparing regions with and without either back or front surface DLDs could identify the defects electrically affecting device performance. With this

information, improved buffer and device design strategies could be formulated to reduce the density and impact of these defects. Comparative acceleration voltage dependent EBIC measurements and analysis of the various GaAsP 1J solar cell designs grown in the Lee group may also improve understanding of how to reduce/eliminate DLDs. Work is currently in progress to investigate whether design modifications of the AlGaAsP BSF + spacer design such as increased AlGaAsP thickness can provide a better electrical barrier for the GaAsP top cell from possible misfit dislocation bundles. If back surface DLDs are from misfit dislocation bundles in the CGB, then another possible strategy to reduce the impact of bundles on the top cell could be to further separate the top cell from the CGB. Due to limited III-V thickness on Si, this likely would mean reduced CGB thickness followed by lattice matched spacer growth that could result in higher TDD. However, I already showed that GaAsP solar cell performance can increase because of decreased DLD density even with increased TDD.

In addition, further investigation of AlGaAsP-based window layer designs is encouraged as the design surprisingly increased GaAsP 1J fill factor to reach high efficiency despite lost carrier collection from window absorption. While I did not observe decreased front surface DLDs with the AlGaAsP window design, other designs could possibly affect these defects. However, AlGaAsP window layer design is complicated by possibly poor n-type doping, absorption loss with low x_{Al}, potential oxidation with high x_{Al}, higher growth rate than GaAsP if no growth pause is taken, and etch selectively challenges between the contact layer and window layer materials.

The ~1.7 eV GaAsP top cell junction design might also be further optimized by exploring doping levels and thicknesses for the $n^+/i/p$ design, such as changing thickness of the undoped layer. In addition, it is quite possible that an adjusted n^+/p junction design such as a thicker base and/or modified doping concentrations could be better than the $n^+/i/p$ design. A result by S. Fan in

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the Lee group indicates high efficiency from the n^+/p junction with thicker base, given the AlGaAsP BSF + spacer and high minority carrier lifetime in the base, can achieve high current, fill factor, and not suffer additional V_{OC} loss from a wider depletion region. Also, initial experiments indicate using delta doping in the window layer may allow thinner window layers and reduce surface Fermi-level pinning for lower emitter sheet resistance. Use of delta doping to act as spikes in the band diagram to potentially deter minority carriers from interacting with interfaces/surfaces and study of the resulting change (if any) in interface/surface recombination velocities may be warranted.

Though not discussed in this dissertation, the GaAsP-based tunnel junction (TJ) design could be modified to reduce absorption loss, specific resistance, or performance loss from thermal load of subsequent growth. While attempts in the Lee group to completely remove the n^+-GaAs:Te layer have resulted in non-functional TJ devices after thermal load, thinning this layer could reduce absorption loss of photons intended for the Si bottom cell. Other changes might also be helpful to maintain a functional TJ with thinned n^+-GaAs:Te, such as increased Te delta doping in this layer or adding p^+-AlGaAs:C for reduced E_G of the p-tunneling layer. Additionally, investigation of whether placing the GaAsP spacer layer of the AlGaAsP BSF + spacer design prior to TJ growth would affect GaAsP top cell performance could reduce the time the TJ is at high T_{growth} by ~25% or afford a thicker GaAsP top cell. Alternatively, changing the AlGaAsP BSF + spacer to just a single, thick AlGaAsP layer could reduce growth time with faster growth rate. Growth rates > 1 μm/hr for GaAsP could also be of interest to reduce time at high T_{growth}.

High defect densities in the GaAsP top cell reducing GaAsP long-wavelength current collection and V_{OC} along with high interface recombination velocity at the defect-ridden front surface of the Si bottom cell reducing Si V_{OC} presently limit further improvement of the 25%-

efficient GaAsP/Si 2J solar cell [21]. Advancements to the GaAsP top cell design as discussed in prior paragraphs could improve both GaAsP 1J and GaAsP/Si 2J solar cells. Heavier n-type doping of the Si emitter could boost Si bottom cell V_{OC} from ~0.51 V to > 0.6 V by reducing interface recombination [21], [172]. However, for the commercial GaP/Si templates ($NAsP_{III/V}$) utilized by the Lee group, the Si emitter has not been modifiable by the company and attempts by S. Fan to improve Si emitter doping have harmed the GaP layer and subsequent growth. Additionally, the Lee group's GaAsP/Si 2J fabrication process is area-constrained limiting the ability to target the large-area efficiency record requiring ≥ 1 cm^2 device size [3].

In response, collaborative work is in progress with a team at Fraunhofer Institute for Solar Energy Systems as I have grown GaAsP/Si 2J solar cells on their 100 mm GaP/Si template wafers for which Feifel *et al.* have achieved Si bottom cell V_{OC} of ~0.63 V [114]. The team at Fraunhofer is able to fabricate these wafers into high-quality large-area devices. Combination of the Lee group's GaAsP sub-cell with Fraunhofer's Si sub-cell could enable ~27%-efficient GaAsP/Si 2J solar cells. Comparison of ~1.7 eV GaAsP 1J solar cells on GaP/Si templates from $NAsP_{III/V}$ and Fraunhofer showed devices on Fraunhofer templates had slightly increased TDD resulting in decreased carrier collection and V_{OC}. Even so, GaAsP/Si 2J efficiencies up to 26% are possible from the initial GaAsP/Si 2J growths with Fraunhofer templates, able to exceed the present certified records for epitaxial III-V/Si multi-junction solar cells including 23.4% for GaAsP/Si 2J cells and 25.9% for GaInP/GaAs/Si triple-junction cells [3], [14], [22]. The team at Fraunhofer is in progress fabricating, testing, and certifying the GaAsP/Si 2J device results.

A second set of electron irradiation testing of ~1.7 eV GaAsP 1J solar cells is in progress. This experiment is more expansive than the first set of testing described in Chapter 8.2 including devices with a variety of different device designs, TDD, and performance. This time I am also

investigating degradation with varied fluence for p^+/n, n^+/p, and $n^+/i/p$ junction polarities. As degradation was largely dominated by loss of long-wavelength carrier collection in the base due to reduced base diffusion length, designs such as n^+/p devices with thinner base and $n^+/i/p$ devices could enable high remaining factors for efficiency.

Though not planned to be studied currently, annealing experiments for these devices after electron irradiation could demonstrate if performance recovery occurs following heating and/or light exposure similar to that observed in orbit. Initial experiments on p^+/n devices with 200 °C annealing recovered half of the lost efficiency from radiation damage after 6 hr. However, after 24 hr at 200 °C no additional benefit was observed but instead a harmful metal-semiconductor interaction appears to have damaged performance. In addition, this annealing is at higher temperature than for typical orbits, so testing lower temperature such as 80 °C would be more appropriate. For thermal testing of GaAsP on Si, thermal cycling using the temperature-dependent measurement setup as well as thermal shock tests with liquid nitrogen and oven/furnace could be performed similar to [173] to test for cracking due to thermal mismatch. GaAsP on Si samples with varying III-V thickness could also undergo thermal shock testing.

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APPENDIX A

SLIP SYSTEMS AND A/B-DIRECTION GEOMETRY

This appendix summarizes dislocation geometry relevant to zincblende III-V compound semiconductors under compression. The crystal structure for III-V compound semiconductors (AlGaIn-PAsSb) is zincblende having face-centered cubic lattices with basis having group III element at site A (0,0,0) and group V element at site B (¼,¼,¼). Slip systems are tabulated based on [118], [174], [175]. Info on associated dislocation type are also included with dislocations assumed to be of glide set [104], [116], [174], [176], [177]. In addition, further elaboration is provided for the A/B-direction geometry in relation x-ray diffraction (XRD) measurements.[29]

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[29] Parts of this appendix are reproduced from supplementary material of [R. D. Hool *et al.*, "Challenges of relaxed n-type GaP on Si and strategies to enable low threading dislocation density," *J. Appl. Phys.*, vol. 130, no. 24, p. 243104, Dec. 2021, doi: 10.1063/5.0073525.], with the permission of AIP Publishing.

Slip system	Line direction	$\vec{b}$	$\vec{b}_{misfit}$	$\vec{b}_{screw}$	$\vec{b}_{tilt}$	Slip plane and type	Dislocation type*	Dislocation core*
1	[110]	$\frac{a}{2}[011]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{4}[110]$	$\frac{a}{2}[001]$	$(1\bar{1}1)$ B+	β or A(g)	Group III
2	[110]	$\frac{a}{2}[\bar{1}01]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{4}[\bar{1}\bar{1}0]$	$\frac{a}{2}[001]$	$(1\bar{1}1)$ B+	β or A(g)	Group III
3	[110]	$\frac{a}{2}[\bar{1}0\bar{1}]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{4}[\bar{1}\bar{1}0]$	$\frac{a}{2}[00\bar{1}]$	$(\bar{1}11)$ B–	β or A(g)	Group III
4	[110]	$\frac{a}{2}[01\bar{1}]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{4}[110]$	$\frac{a}{2}[00\bar{1}]$	$(\bar{1}11)$ B–	β or A(g)	Group III
5	$[1\bar{1}0]$	$\frac{a}{2}[01\bar{1}]$	$\frac{a}{4}[110]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{2}[00\bar{1}]$	(111) A–	α or B(g)	Group V
6	$[1\bar{1}0]$	$\frac{a}{2}[10\bar{1}]$	$\frac{a}{4}[110]$	$\frac{a}{4}[1\bar{1}0]$	$\frac{a}{2}[00\bar{1}]$	(111) A–	α or B(g)	Group V
7	$[1\bar{1}0]$	$\frac{a}{2}[101]$	$\frac{a}{4}[110]$	$\frac{a}{4}[1\bar{1}0]$	$\frac{a}{2}[001]$	$(\bar{1}\bar{1}1)$ A+	α or B(g)	Group V
8	$[1\bar{1}0]$	$\frac{a}{2}[011]$	$\frac{a}{4}[110]$	$\frac{a}{4}[\bar{1}10]$	$\frac{a}{2}[001]$	$(\bar{1}\bar{1}1)$ A+	α or B(g)	Group V

Table A.1: Slip systems in compression for misfit dislocations in zincblende III-V semiconductors which are $a/2\langle 110\rangle\{111\}$ type. Adapted from Olsen *et al.* [174] with added detail for clarity [118], [175]. *Dislocations are assumed to be of the glide set [104], [116], [174], [176], [177], and consistent with strain relief for material in compression. From [65].

For a zincblende III-V semiconductor the A (group III) and B (group V) designation refers to the basis sites and therefore the slip planes; (111) and $(\bar{1}\bar{1}1)$ are the A-planes and $(1\bar{1}1)$ and $(\bar{1}11)$ are the B-planes as shown in Table A.1 [65]. In XRD, the A-/B-direction samples misfit dislocations that glide in the A-/B-planes. Below is the tracking for the A/B-direction alignment. Fig. A.1 shows the sample geometry when measuring in B-direction alignment.
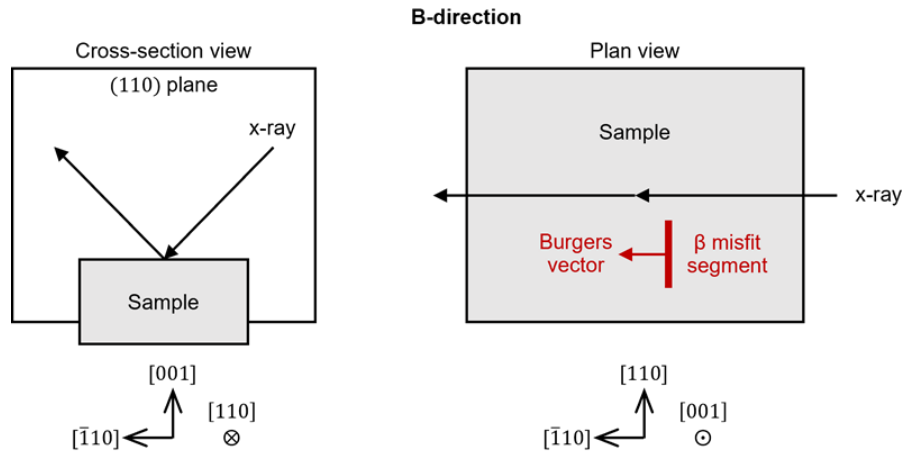

Fig. A.1: Schematic of XRD B-direction geometry in both cross-section and plan views to show the relation of the incident x-ray to β-dislocations.

To sample the B-direction, x-rays are incident in the (110) plane with projection in $[\bar{1}10]$. This measures the misfit dislocations with parallel misfit component of the Burgers vector (the strain-relieving component) in $[\bar{1}10]$. As shown in Table A.1, these are called β-dislocations which have $[110]$ line direction and glide on B-planes.

To sample the A-direction, x-rays are incident in the $(\bar{1}10)$ plane with projection in $[110]$. This measures the misfit dislocations with parallel misfit component of the Burgers vector (the strain-relieving component) in $[110]$. As shown in Table A.1, these are called α-dislocations which have $[1\bar{1}0]$ line direction and glide on A-planes.