TECHNIQUES FOR INTEGRATED ENERGY-EFFICIENT POWER CONVERSION

BY

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DISSERTATION

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ABSTRACT

Power converters are a fundamental part of any system that seek to transfer electrical energy from one voltage domain to another. Traditionally, the power converter required bulky off-chip power switches to maintain acceptable efficiency which resulted in them occupying a significant portion of the total system volume. As these systems evolved to reduce in volume the corresponding power converters needed to adapt by improving both power density and efficiency. This eventually led to the integration of power switches along with the control circuitry on a single die. This integration presented unique opportunities and challenges from a power converter perspective which has resulted in a renewed focus on integrated power converters.

The various DC-DC power converter topologies can be broadly categorised into two classes: switched-inductor and switched-capacitor types. Generally, the switched-inductor type is more suitable for power levels of the order of a few watts or higher, while the switched-capacitor type is more suited to low-power applications of a few hundred milli-watts. Recently, a third category has emerged: hybrid converters which tries to combine the advantages of both the aforementioned categories. The relatively new type of power converter primarily aims to improve power efficiency by easing the trade-off between switching and conduction loss by enabling the use of better power switches.

In the first technique, a hybrid boost converter architecture for improving the efficiency of LED drivers used in mobile applications, is presented. By cascading a low-switching frequency time-interleaved series-parallel SC-stage with an inductive boost converter, we facilitate lower voltage-rated switches, thus significantly reducing the switching losses. Charge-sharing losses of the SC stage are minimized by soft-charging flying capacitors with the inductor of the boost stage. Fabricated in 180 nm BCD process, the prototype converter generates 30 V output voltage from a Lithium-ion (Li-ion) battery source. It can provide a load current in the range of 0 to 100 mA with an excellent peak

power efficiency of 91.15% at 30 mA, which represents a 3% improvement over the state-of-the-art.

In the second technique, a novel current sensing architecture is explored. A new duty-cycle sensing technique with applications in current sensing for DC-DC power converters is presented. A time-based $\Delta\Sigma$ ADC with 1-bit delay-DAC accurately measures small changes in the duty-cycle of a PWM waveform. Fabricated in 65 nm general purpose CMOS process, the prototype senses changes in duty-cyle ranging from 4 m up to 20 m with 1% linearity, making it suitable for detecting small load current-dependent changes in the duty-cycle of a regulated DC-DC power converter.

The switching clock of a power converter is an important part of the whole system. It is essential to keep the frequency of this clock fixed under various operating conditions in order to prevent the generation of unwanted harmonics which might interfere with the proper functioning of the whole system. For most low-frequency integrated power converters, an on-chip relaxation oscillator is used. Even though this oscillator architecture is very power efficient, it has large variation in frequency over temperature. A method for improving the temperature stability of RC relaxation oscillators by precisely interpolating between resistors with opposing temperature coefficients is presented. By obviating the need for a large trimming network of switches and resistors, it achieves excellent frequency accuracy across PVT. Fabricated in 65 nm CMOS, the prototype 400 kHz oscillator achieves an inaccuracy of 16 ppm/^{o}C (-40^{o}C to 85^{o}C), 2.5 ppm/mV voltage sensitivity, and 5.6 ppm Allan deviation in one second strides.

To my parents, for their love and support.

ACKNOWLEDGMENTS

According to Albert Einstein, time is supposed to slow down for people traveling with high velocities measured from an inertial frame of reference. But going to graduate school has taught me that there is a big difference between measured time duration and perceived time duration. For even though the earth is hurtling around the sun at a whopping velocity of about 100,000 km/hr, I clearly remember the day I came to the U.S. for my higher education more than four years ago, as if it were yesterday. This discrepancy is perhaps because graduate school makes you ask yourself so many questions, both work-related and personal, that the brain has no bandwidth left to observe the passage of this large chunk of time. As I struggled with this unending set of questions, not only did I encounter self-doubt, uncertainty and fatigue, but also long-lasting joy and deep satisfaction. And for this I am most thankful to my advisor, Professor Pavan Kumar Hanumolu. I am forever indebted to him for providing me with the opportunity to pursue my studies in this fabulous university (Go Illini!) and in a way which is very different from other groups doing circuit research in the U.S. He has a surprisingly vast reservoir of patience, which, I am sure, came in handy during the numerous times I had reported to him about my chip not starting in the lab or running into a wall with some design problem. He always had a suggestion worth trying, an untapped research question, a paper edit which had a clearer flow and figures which were always better than my multiple miserable attempts. And through him I came to know so many wonderful people who have also helped me immensely through out my graduate studies. I am thankful to Professor Robert Pilawa for being so patient with me during the initial period. He was always happy to answer my questions on basic principles of hybrid DC-DC converter. I am thankful to Professor Arijit Banerjee for his wonderful teaching in ECE464, which helped me a lot. In addition to everything else, Professor Pavan, Pilawa, and Banerjee also agreed to serve

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When I first came to the U.S., I had assumed it would be difficult to find friends here as people from a vastly different cultural backgrounds come to study here. But I was pleasantly surprised to make really good friends here. I would like to thank Charlie Zhu for his continuous help and support regarding my work and his friendship through which I discovered the wonderful world of Chinese cuisine over the numerous dinners in various Chinese joints here in Urbana-Champaign. I would like to thank Mostafa Ahmed and Amr Khashaba for their friendship and support throughout my time here, exchanging notes about the culture and politics of Egypt and India. I am grateful to Yongxin Li for inviting me to his lovely star-gazing sessions, to Kyu-Sang Park for helping me innumerable times in the lab with his superior soldering skills, to Tianyu Wang, Ahmed Abdelrahman, Mohamed Badr and Mahmoud Khalil for fun technical and non-technical discussions in CSL422.

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CHAPTER 1

INTRODUCTION

Power converters are integral components of all electronic systems. They are responsible for supplying power to the rest of the system at a preferred voltage level enabling them to perform their functions. For instance, all portable electronic devices have a converter interfacing between the 3 V Li-ion battery and the various subsystems such as the processor core, memory, display, etc., each requiring a different voltage level. Solar panels have a power converter which provides an interface between the solar cells, that generate a wide range of voltages, and the battery, which stores the power generated by the solar cells at a relatively fixed voltage. Since a significant portion, if not all of the system power, is processed through these converters, high power efficiency of these converters is absolutely essential to maintain an acceptable overall system power efficiency.

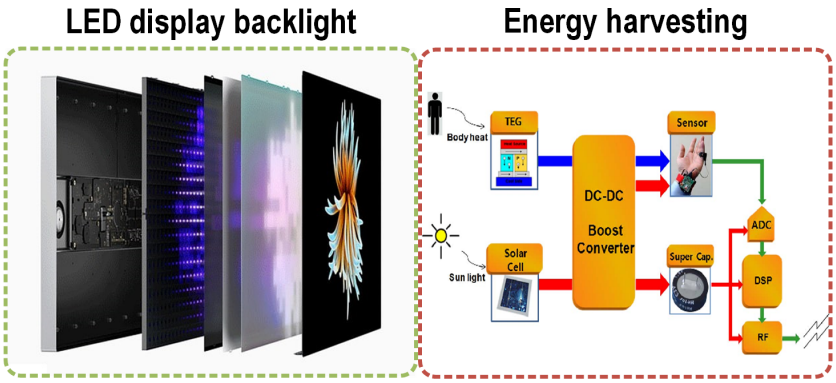

Figure 1.1: Boost converter use in LED display drivers and energy harvesting applications.

Table 1.1: Relationship between DCR and dimension for a 10 μH inductance from Coilcraft

DC resistance [mΩ]	Current rating [A]	L(mm)×W(mm)×H(mm)
69.5	3.9	4×4×3.1
200	1.25	3.9×3.9×1.8
440	0.75	2.95×2.95×1.5
611	0.66	2×1.9×1
180	0.18	1.8×1.12×0.91

1.1 Power converter architecture choices for better efficiency

Maintaining high power efficiency in a power converter traditionally meant use of large passive components and switches, as their sizes tended to have an inverse relationship with the losses of the power converter. This is especially true for inductors as shown in Table 1.1. As the size of the inductor reduces the series DC resistance increases steadily. However, relentless progress in semiconductor technology has resulted in diminishing sizes of almost all electronic systems. This has resulted in the constant shrinking of portable electronic systems—so much so that their size and efficiency are limited by the power supply systems they employ. This paved the way for integrated power converters that try to incorporate power-switches and control circuitry onto a single die, yielding highly compact solutions with impressive power density.

The desired power level decides the type of DC-DC power converter suitable for the application. For applications with power levels up to a few tens of milliwatts, the switched capacitor architecture is most suitable. For high-power applications beyond a few hundred milliwatts, inductive-based architecture is primarily used. Figure 1.2 shows the two types architectures.

Recently, hybrid architectures have been reported as alternatives to both these architectures in various applications [1]. These architectures try to leverage the use of lower-voltage rated switches from the switched-capacitor architecture but avoid high charge-sharing losses by using an inductor in series. The first technique presented in this thesis explores the possibility of a hybrid converter in the context of LED drivers for portable electronic device displays such as mobile and tablet screens. Existing inductive converter

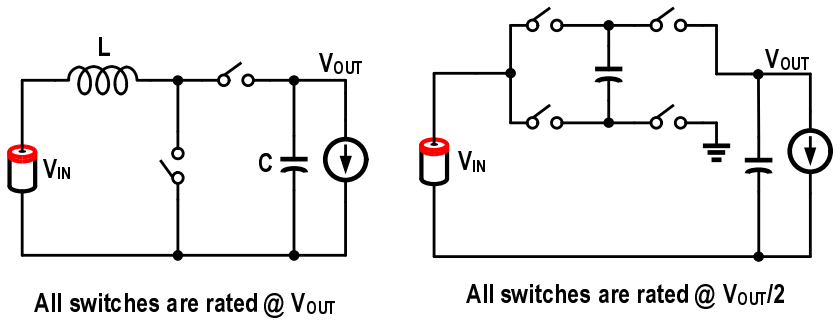

Figure 1.2: Inductive-based (left) and switched-capacitor-based (right) DC-DC power converter architectures.

based techniques dominate the solution space for mobile display LED-drivers. Due to their inherent architectural limitation of using output voltage rated switches, they cannot achieve good efficiency beyond 88% in the best reported LED-drivers at high voltage levels of about 30 V. The hybrid architecture presents an alternative solution with better efficiency at the cost of a slightly increased external component count on the PCB.

1.2 Current-sensing for better system efficiency

Extending battery life is crucial for portable electronic devices such as mobile phones (see Fig. 1.3). Knowledge of the current consumption is often a very useful information in this regard. For instance, embedded software of mobile phones can use this information to optimise its operation. Such optimisations include reducing system-clock frequency, shutting down unnecessary modules not required by the current operation, estimating precisely the remaining battery life of the system [2]. Current-sensing is also used in many regulation schemes for power converters [3] and over-current protection schemes. The accuracy and latency of the current sensing scheme depends on the system requirements. The software/processor based system optimisation application requires more accuracy and can relax on the latency specification. The over-current protection module requires very fast response, hence very low latency, but can be flexible on the accuracy.

In all these applications, the power-converter operating in the system is expected to provide the load-current information. Two principal approaches are used for current sensing in power converters, namely the sense-FET based

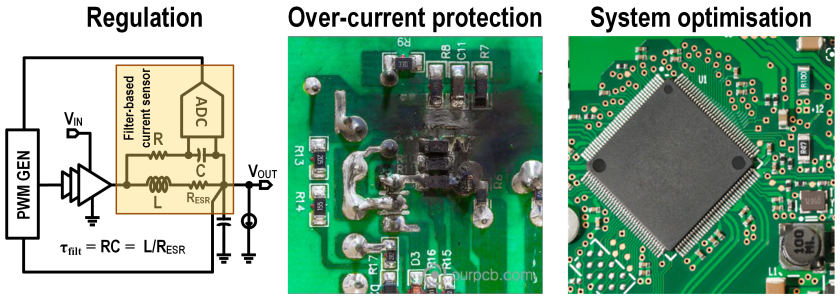

Figure 1.3: Different applications for current sensing in power converters.

and filter-based approaches, as shown in Fig. 1.4. The accuracy of sense-FET based approach is limited by the settling errors in the amplifier and the mismatch resulting from the large size-ratio between the power-FET and sense-FET. The filter-based approach is mainly used to sense AC current and its use is limited to current-mode control regulation schemes.

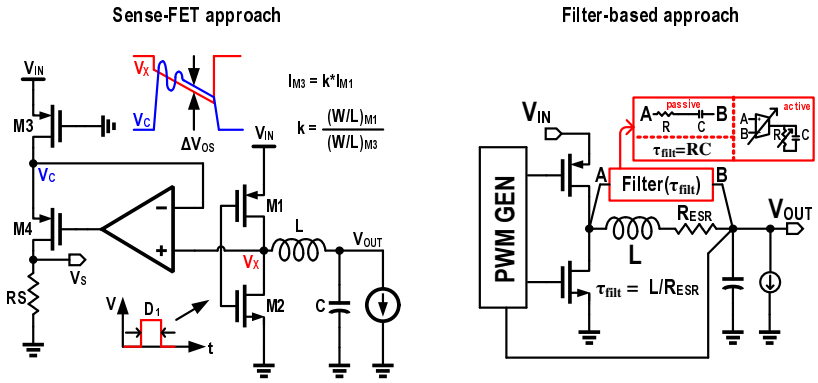

Figure 1.4: Sense-FET-based and filter-based approaches for current sensing in power converters.

In view of this, we seek to explore a duty-cycle based current sensing technique, leveraging on the fact that the duty-cycle of a regulated power converter changes with the load current.

1.3 Highly stable clock source for lower harmonic content in output voltage in power converters

For most power converters operating at frequencies less than 10 MHz, the clock source is a relaxation oscillator. While these are efficient clock sources

and well-suited for integration, their output frequency has a strong dependence on temperature and process. This is mainly due to the temperature and process dependence of the reference resistor. One way to approach this problem would be make very stable integrated resistors [4]. But, often it is very difficult to procure such a stable resistor in most of the technology nodes in prevalent use today. It is more likely that one can find resistors with opposite temperature coefficients in the popular processes. Simply cascading resistors of opposing temperature trends will not solve the problem as their proportion might vary heavily with process, thus resulting in imperfect cancellation. An array of such resistors with programmable trim settings also won't give good performance as the switches in the trim DACs degrade temperature performance. In view of this, we seek to explore a novel resistor DAC with minimal use of switches such that we can achieve very precise interpolation between the resistors in order to obtain an effectively zero-temperature coefficient resistance without significant degradation from the trimming switches.

1.4 Dissertation organisation

The focus of this dissertation is on developing techniques which improve system power efficiency of portable electronic systems by exploring different aspects of the power management module used in such devices. The dissertation is organised as follows:

Chapter 2 describes a new hybrid DC-DC boost converter for LED-driver application in mobile phones. It presents the proposed architecture, illustrating its properties and operating principle. This approach is then compared to the existing approach and the benefits are clearly explained. Measured results are obtained from the prototype power converter and the key contributions are summarized.

Chapter 3 describes a duty-cycle sensor for current-sensing applications in power converters. It presents the proposed architecture and its evolution. The circuit implementation details are discussed. The measured results from a prototype duty-cycle sensor are presented and the key contributions are summed up.

Chapter 4 describes a temperature compensated relaxation oscillator. The

proposed architecture is explained and an analysis is presented about the residual temperature error using this approach. The circuit details are explained clearly. Measured results from the prototype are shown and the principal contributions are highlighted.

Finally, Chapter 5 summarises the proposed design techniques for integrated energy-efficient power converters and some possible future work is outlined.

CHAPTER 2

A 91.15% EFFICIENT 2.3-5 V INPUT 10-35 V OUTPUT HYBRID BOOST CONVERTER FOR LED-DRIVER APPLICATIONS

2.1 Introduction

Rapid technological advances over the last decade have made the display module an integral part of modern portable electronic devices such as smartphones and tablets. While these developments have enhanced user experience significantly, they also made the displays by far the most power-hungry blocks in smartphones [6]. A typical display module comprises a back-light and an LCD panel. The back-light consists of strings of series-connected white light-emitting diodes (LEDs). Screen size and brightness requirements may mandate stacking of up to eight LEDs in each string. With each LED having a forward-bias voltage of about 3.3 V, the required supply voltage needed to drive the chain can be as high as 27 V. Tight volume constraints mandate that such a high output voltage be generated from a 2.3-5 V input voltage provided by a Li-ion battery. To this end, a boost converter is most commonly used to perform the desired DC-to-DC conversion. Since the display module consumes 30-40% [6] of the total available energy, the efficiency of such a boost converter significantly impacts system power efficiency. Traditionally, an inductor-based switching power converter depicted in Fig. 2.1 is used [7]. It consists of a pair of switches S_1, S_2, an inductor L, and an output capacitor C. Switches S_1 and S_2 are driven by complementary PWM signals with a duty-cycle of D and $(1 - D)$ and generates an output voltage given by Eq. 2.1:

$$V_{\text{OUT}} = \frac{V_{\text{IN}}}{1 - D}. \tag{2.1}$$

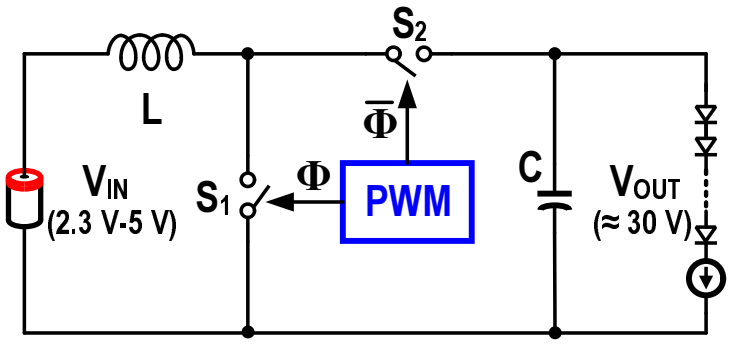

Figure 2.1: Conventional boost converter-based LED driver.

Even though this architecture requires very few off-chip components, its efficiency is fundamentally limited by the switches' high voltage rating. As will be described later, a high switch rating exacerbates both switching and conduction losses, thus limiting the achievable peak efficiency of state-of-the-art display drivers to about 88% [7, 8].

The impact of switch voltage rating on boost converter efficiency can be understood by plotting efficiency versus load current for different output voltages at a fixed input voltage (see Fig. 2.2). The power switch sizes were optimized for each output voltage. As the switch rating increases (to support the increased output voltage) from 6 V to 36 V, peak efficiency degrades by more than 5%. The reduction in the power switch quality increases both the switching and conduction losses, which causes the observed degradation in peak efficiency. One possible approach to overcome this problem would be to explore architectures that do not require such high voltage-rated switches. A class of switched capacitor (SC)-based converters can generate high output voltages using devices rated lower than the output voltage [9], [10]. But they incur a considerable amount of charge-sharing losses at typical LED driver's operating power levels. The large DC gain requirement increases the number of switches, which significantly increases conduction and switching losses.

Hybrid architectures have recently emerged as an alternative to the SC-based approaches mentioned above. By cascading a SC stage with an inductive stage [1] or by merely placing an inductor between the power source and a SC converter [11], [12], these architectures seek to combine the advantages of inductive- and SC-based converters. Placing the inductor in the path of the charging/discharging current of the flying capacitor reduces hard-charging losses to a great extent. Recent works have effectively used

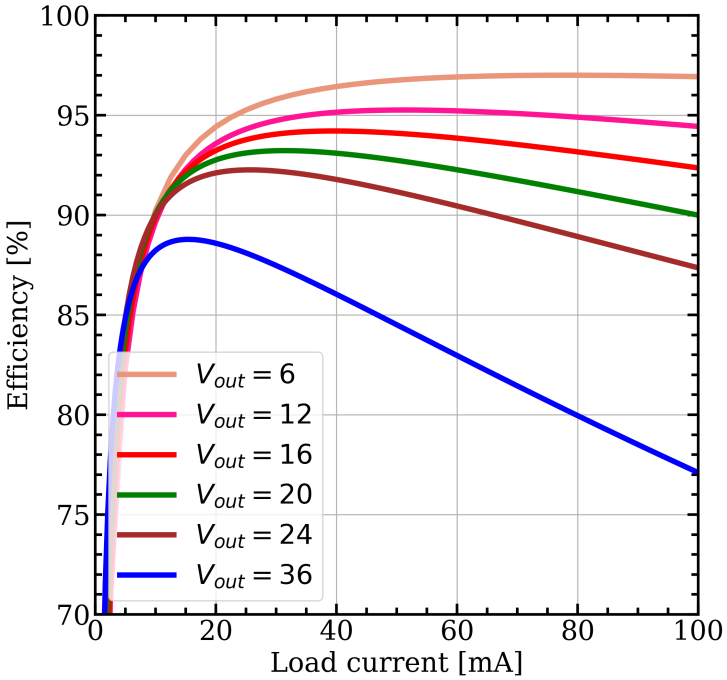

Figure 2.2: LED driver efficiency versus load current for different output voltages and fixed $V_{IN} = 3.7$ V.

this approach, but could not completely eliminate hard-charging losses [13] or output-voltage rated switches [14].

This paper presents a high-efficiency boost converter for LED driver applications with an input voltage range of 2.3-5 V, an output voltage range of 10-35 V, and a load range of 0-100 mA [15]. The prototype power converter was fabricated in 180 nm technology and occupies an active area of 2.3 mm by 1.2 mm, and operates at 1 MHz switching frequency. The power converter achieves an excellent peak power-efficiency of 91.15% at 3.7 V input, 30 V output with no external gate driver supplies, representing a 3% improvement in peak efficiency over the state-of-the-art. This paper supplements the information provided in [15] with a detailed elucidation of the architecture evolution, an in-depth analysis of the output impedance of hybrid architectures, a detailed description of the phase-by-phase operation of the converter, additional details of the zero-crossing detector for discontinuous conduction mode (DCM) operation, and new measurement results pertaining to the improvement in power efficiency in DCM compared to CCM.

The rest of the paper is organized as follows: Section 2.2 presents a breakdown of the losses in an inductive boost converter used in conventional LED drivers; Section 2.3 presents the proposed architecture; circuit implementation details of key building blocks are described in Section 2.4; experimental results from the test chip are presented in Section 2.5; key contributions of this paper are summarized in Section 2.6.

2.2 LED driver losses

Losses in a LED driver depend on the magnitude of input/output voltages, load current, and switching frequency. The typical range of input/output voltages and load current is 2.3-5 V/12-30 V and 0-100 mA, respectively. Losses can be broadly classified as conduction losses and switching losses. The current source used to set the LED current has to biased with about 200 mV across it, which also incurs an efficiency penalty. However, in LED drivers with V_{OUT} as high as 30 V, the efficiency hit is minimal. These loss mechanisms are investigated for the conventional inductive boost converter next and later extended to the proposed architecture.

Conduction losses are modeled using the below equation [16]:

$$P_{cond} = i_{IND,RMS}^2 \cdot (R_{DCR} + D \cdot R_{LS} + (1 - D) \cdot R_{HS} + R_{PCB}) \qquad (2.2)$$

where, $i_{IND,RMS}$ is the inductor RMS current, D is the duty-cycle of the low-side switch and R_{LS}, R_{HS} are the "on" resistances of the low- and high-side switches, respectively. The value of R_{DCR} depends on the size of the inductor and is typically in the range of 200-300 mΩs for inductors used in space-constrained mobile applications. Such a large R_{DCR} is a significant source of conduction loss, especially at higher load currents.

Switching losses have three components denoted by $P_{transition}$, P_{gate}, and P_{core}. Power switch losses incurred during transitions between "on" state and "off" state is represented by $P_{transition}$. This is a result of the current through the power device and the voltage across the power device being non-zero during the transition.

Using low-side switch M_{LS} voltage and current waveforms during a turn-ON event (see Fig. 2.3), $P_{transition}$ can be calculated using Eq. 2.3 [17, 18, 19, 20, 21, 22, 23, 24]:

$$P_{transition} = 0.5 \cdot F_{SW} \cdot V_{OUT} \cdot I_L \cdot (t_1 + t_2) \tag{2.3}$$

where V_{OUT} is the output voltage, F_{SW} is the inductor switching frequency. Times t_1 and t_2 are estimated using gate driver current I_{DR} and gate charges Q_{GS} and Q_{GD} as explained in [19]. At large load currents, $P_{transition}$ becomes a significant component of the switching losses. This transition loss equation can be modified to include the reverse recovery loss of the body diode of M_{HS} and that of the parasitic capacitance $C_{DS,LS}$ [25].

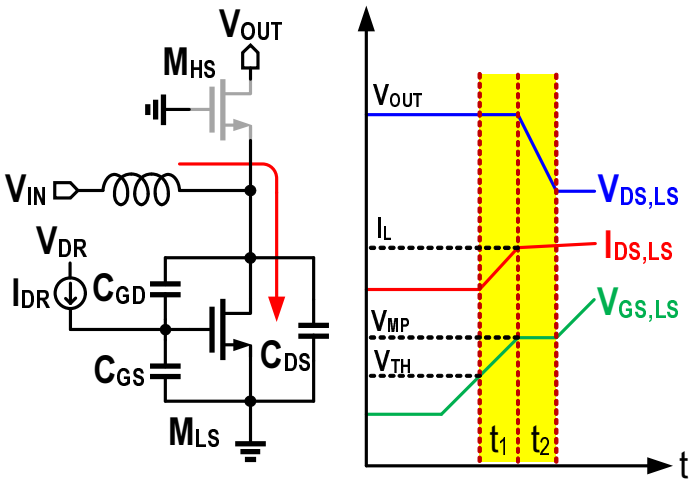

Figure 2.3: Transition loss modeling for turn-ON event of low-side switch.

P_{gate} represents the power lost during the charging/discharging of the gate terminal of the power switches and can be modeled by Eq. 2.4 [16]:

$$P_{gate} = C_{gate} \cdot V_{IN}^2 \cdot F_{SW} \tag{2.4}$$

where C_{gate} and V_{IN} is the gate capacitance of the power switch and input voltage to the power converter, respectively.

P_{core} represents the inductor's magnetic losses, and its magnitude depends on the inductor dimensions, with larger height inductors having lower core losses. Core losses can be calculated using Steinmetz expression in Eq. 2.5 [26]

$$P_{core} = K_{FIT} \cdot F_{SW}^{\alpha} \cdot (\Delta I_{IND})^{\beta} \tag{2.5}$$

where K_{FIT}, α and β are fitting parameters provided by manufacturers. ΔI_{IND} is inductor current ripple. In addition to the losses described above, other losses, such as dead-time losses, are also incurred during every switching cycle, but their contribution to the total loss is much smaller.

2.2.1 Simulated loss breakdown

The power converter's efficiency is typically optimized at the most probable load current, which is around 20-40 mA for LED drivers used in smartphones [27]. A 3.7 V input 30 V output conventional inductive boost power converter was designed to examine the relative contribution of each type of loss, and the simulated variation of conduction and switching losses as a function of the load current is plotted in Fig. 2.4. Switch sizes were chosen to minimize the total loss (switching + conduction) for a given load current and switching frequency. The pie-chart in Fig. 2.4 shows the relative contribution of each type of losses at 25 mA load current, incuding the current source losses (I_{SRC} losses). Both the switching and conduction losses contribute significant portions to the total loss at this load current. Because power switch size trades off conduction losses with switching losses, increasing the switch size beyond a certain point does not reduce the total loss. Architectures that allows switches with lower voltage rating ease this trade-off, thereby presenting a possibility for significantly reducing the losses.

2.3 Proposed Architecture

A simplified block diagram of the proposed hybrid boost converter architecture is shown in Fig. 2.5. It consists of an inductive boost stage (BST) followed by a switched-capacitor (SC) stage. The BST stage provides a DC gain of $M = 1/(1-D)$, where D is the PWM signal's duty-cycle while, SC

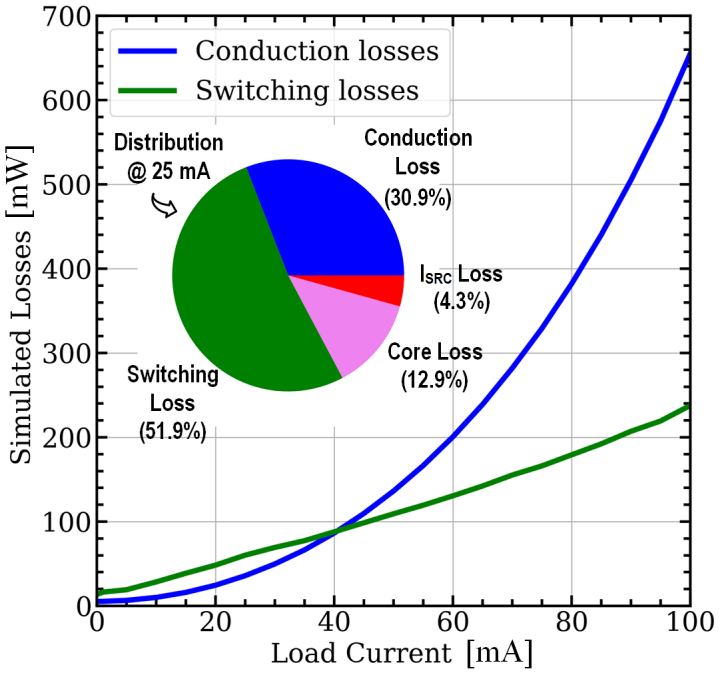

Figure 2.4: Electrical switching loss ($P_{transition} + P_{gate}$) and conduction loss variation with load current and loss breakdown at 25 mA load ($V_{IN} = 3.7$ V, $V_{OUT} = 30$ V) for a conventional inductive-boost power converter.

stage provides a DC gain of N. DC gains, M, N, must be chosen to meet the overall DC gain requirement, which in our application is about 10. Therefore, for instance, $M = 5$ and $N = 2$ would satisfy this requirement. With this choice, all the switches in BST and SC stages experience a maximum voltage of only half the output voltage across them. Thus, switches rated for only 15 V (as opposed to 30 V) can be used. While the proposed architecture has successfully reduced the power switches' voltage rating, the total number of switches has increased. However, with the appropriate choice of the SC stage architecture and its switching frequency, it is possible to achieve better efficiency, as described next.

2.3.1 SC-stage architecture selection

Two important considerations dictate the choice of SC-stage architecture. First, power losses must be low enough not to impact the overall converter

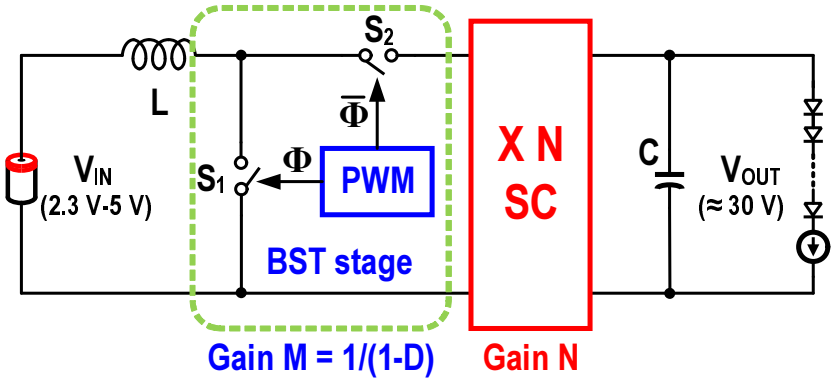

Figure 2.5: Hybrid boost converter.

efficiency. Second, the architecture must be amenable for simple circuit implementation and must obviate the need for auxiliary power supplies. A series-parallel architecture shown in Fig. 2.6 meets these criteria. The lowest output impedance is achieved across a wide range of DC gains when this architecture is operated in the fast-switching limit region where losses associated with switch resistance dominate [10]. The optimal distribution

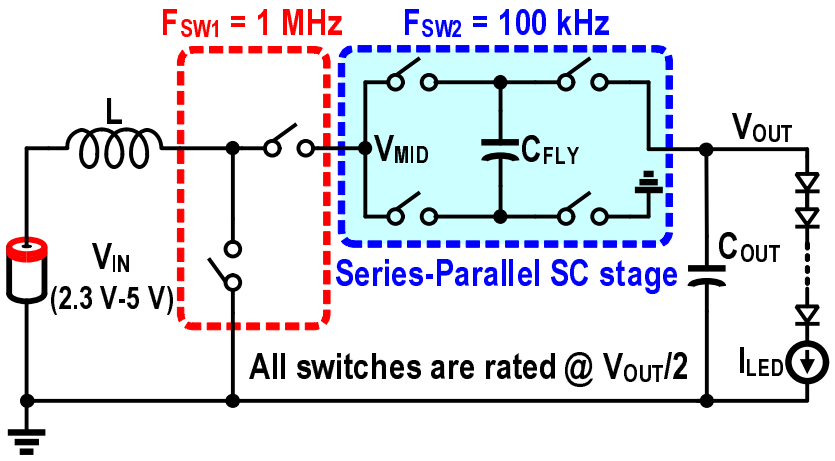

Figure 2.6: Proposed boost converter topology.

of the total DC gain between the inductive-boost and SC stages is determined using the approach described in [14]. In this analysis, output voltage and the conversion gain are set at 30 V and 10, respectively; SC stage was assumed to employ series-parallel architecture. The hybrid converter was optimized for each value of SC-stage gain (N) while keeping the area of the power converter, and the ratio of input/output voltages fixed to perform a

fair comparison. Conduction and switching losses normalized to the losses of a conventional inductive-based power-converter are plotted for different values of N, as shown in Fig. 2.7. Switching losses reduce as N (SC-stage gain) is increased. This is expected behavior since the dominant source of switching loss, namely switching losses in the inductive-boost stage, reduces with increasing N. This is because the rating of the switches in the BST-stage is inversely proportional to the SC stage gain N (V_{OUT}/N). But the same is not true for conduction losses, which reduce when N is changed from N = 1 to N = 2 but start increasing from N = 3. This shows that the increased number of switches offsets the advantage obtained in going to lower-rated switches as N is increased beyond 3. Therefore, N is chosen to be 2 in our implementation. This topology needs only four extra switches, all of which are rated at $V_{OUT}/2$. Their gate drivers can be implemented using internally available voltages, as described in section 2.4.

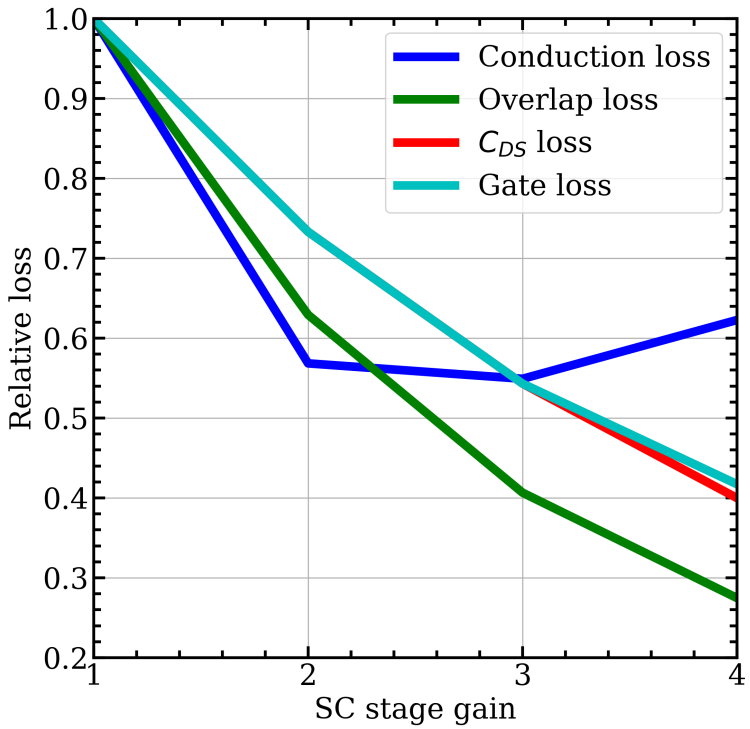

Figure 2.7: Relative loss of proposed architecture with SC-stage gain varying from 2 to 4, normalised to corresponding losses in conventional inductive-boost converter.

2.3.2 Choice of switching frequency for the BST and SC stages

The switching frequency of a conventional inductive boost converter is determined from the ripple requirement, allowed output capacitor, and the load current. Assuming typical parameters of 10 μF (400 nF after de-rating) output capacitor, 25 mA load current, and an output voltage ripple of 50 mV results in a switching frequency of 1 MHz for the BST stage.

For a typical switched-capacitor power converter with a voltage input, the switching frequency directly impacts the loss of the converter. This can be understood by modeling losses in the 1:2 SC converter with an ideal transformer and an output impedance R_{OUT} (see Fig. 2.8) [10] [28] [29] and plotting R_{OUT} as a function of switching frequency for two cases: $L = 0$ and $L \neq 0$ as shown in Fig. 2.9. For the case of $L = 0$, output impedance $R_{OUT,SC}$ is given by Eq. 2.6.

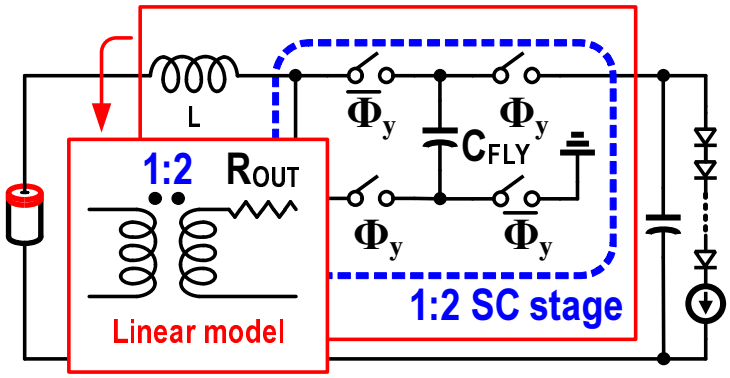

Figure 2.8: 1:2 switched-capacitor converter with inductor at input.

$$R_{\mathrm{OUT,SC}} = \frac{1}{C_{\mathrm{FLY}} F_{\mathrm{SW,SC}}} * \coth \frac{\beta_{\mathrm{SC}}}{4 F_{\mathrm{SW,SC}}} \tag{2.6}$$

where,

$$\beta_{\mathrm{SC}} = \frac{1}{R_{\mathrm{SW,TOT}} C_{\mathrm{FLY}}}$$

$$R_{\mathrm{SW,TOT}} = 2 * R_{\mathrm{SW}}$$

and $R_{\mathrm{SW,TOT}}$ is the total switch resistance in the charging/discharging path, R_{SW} is switch resistance and $F_{SW,SC}$ is the switching frequency. The converter operates in the slow-switching limit for switching frequencies below 1

MHz. In this region, charge sharing losses account for the increase in R_{OUT} with decreasing switching frequency. Beyond 1 MHz, losses associated with the switch resistance dominate, as indicated by the flattening of the curve.

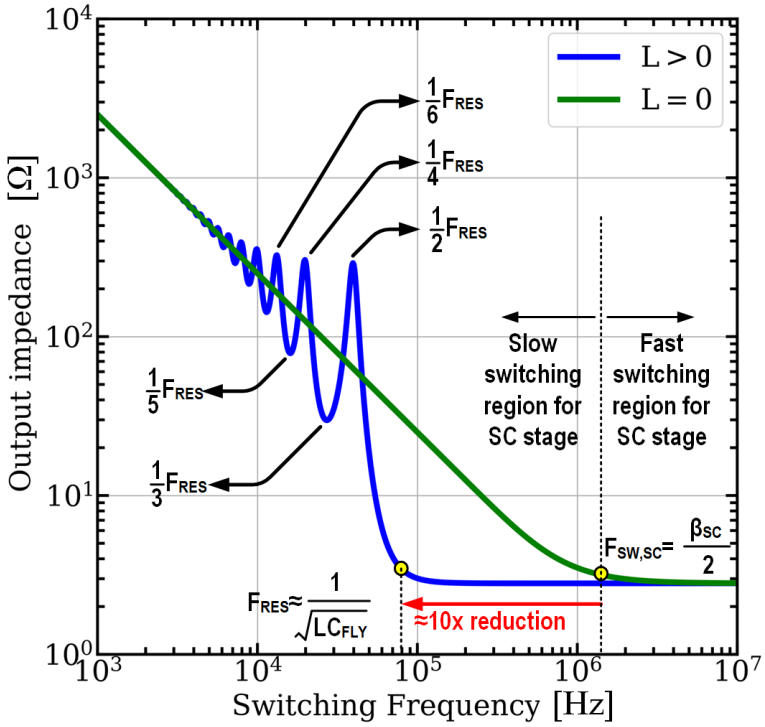

Figure 2.9: Comparison of output impedance of basic hybrid converter with that of the traditional switched-cap converter.

Inductance between the input voltage source and the converter fundamentally changes the relationship between output impedance and the switching frequency. Because inductor current cannot change instantaneously, sudden surges in capacitor-charging currents present when $L = 0$ are avoided, thus, significantly reducing the charge sharing losses. The output impedance of the hybrid converter is determined by calculating the ratio of average power dissipated $\langle P_{\mathrm{HYB}} \rangle_{T_{\mathrm{sw}}}$ and the average output current $\langle I_{\mathrm{OUT,HYB}} \rangle_{T_{\mathrm{sw}}}$ in each switching cycle as given by Eq. 2.7:

$$R_{\mathrm{OUT,HYB}} = \frac{\langle P_{\mathrm{HYB}} \rangle_{T_{\mathrm{sw}}}}{\langle I_{\mathrm{OUT,HYB}} \rangle^2_{T_{\mathrm{sw}}}} \tag{2.7}$$

where,

$$
\begin{aligned}
\langle P_{\mathrm{HYB}} \rangle_{T_{\mathrm{sw}}} &= 2F_{\mathrm{SW,SC}}(T_1 + T_2 + T_3) \\
T_1 &= 0.5(k_1^2 + k_2^2)R_{\mathrm{SW,TOT}} \frac{1 - e^{-\alpha T_{\mathrm{sw}}}}{2\alpha} \\
T_2 &= \frac{\alpha B + \beta_{\mathrm{HYB}} C}{2(\alpha^2 + \beta_{\mathrm{HYB}}^2)}(1 - e^{-\alpha T_{\mathrm{sw}}} \cos(\beta_{\mathrm{HYB}} T_{\mathrm{sw}})) \\
T_3 &= \frac{\beta_{\mathrm{HYB}} B - \alpha C}{2(\alpha^2 + \beta_{\mathrm{HYB}}^2)} e^{-\alpha T_{\mathrm{sw}}} \sin(\beta_{\mathrm{HYB}} T_{\mathrm{sw}}) \\
\langle I_{\mathrm{OUT,HYB}} \rangle_{T_{\mathrm{sw}}} &= F_{\mathrm{SW,SC}}(P_1 + P_2) \\
P_1 &= \frac{\beta_{\mathrm{HYB}} k_1 + \alpha k_2}{\alpha^2 + \beta_{\mathrm{HYB}}^2}(1 - e^{-\alpha T_{\mathrm{sw}}} \cos(\beta_{\mathrm{HYB}} T_{\mathrm{sw}})) \\
P_2 &= \frac{\beta_{\mathrm{HYB}} k_2 - \alpha k_1}{\alpha^2 + \beta_{\mathrm{HYB}}^2} e^{-\alpha T_{\mathrm{sw}}} \sin(\beta_{\mathrm{HYB}} T_{\mathrm{sw}}) \\
B &= 0.5(k_2^2 - k_1^2)R_{\mathrm{SW,TOT}} \\
C &= k_1 k_2 R_{\mathrm{SW,TOT}} \\
k_1 &= \frac{\alpha I_{\mathrm{LOAD}} + \Delta V / L}{\beta_{\mathrm{HYB}}} \\
k_2 &= I_{\mathrm{LOAD}} \\
\alpha &= \frac{R_{\mathrm{SW,TOT}}}{2L} \\
\beta_{\mathrm{HYB}} &= \sqrt{\frac{1}{LC_{\mathrm{FLY}}} - \left(\frac{R_{\mathrm{SW,TOT}}}{2L}\right)^2} \\
\Delta V &= \frac{0.5 I_{\mathrm{LOAD}} T_{\mathrm{sw}}}{C_{\mathrm{FLY}}}
\end{aligned}
$$

The relationship between $R_{\mathrm{OUT,HYB}}$ and the switching frequency is more complicated compared to the $L = 0$ case (see Fig. 2.9). At frequencies much lower than the LC-resonant frequency ($F_{RES} = \sqrt{LC_{\mathrm{FLY}}}/(2\pi)$), the current transient settles down well within the duration of each phase, thereby having no impact on R_{OUT}. As the switching frequency approaches F_{RES}, R_{OUT} exhibits a non-monotonic behavior with peaks at $F_{RES}/2$, $F_{RES}/4$, $F_{RES}/6$ and so on, and troughs at $F_{RES}/3$, $F_{RES}/5$, $F_{RES}/7$ and so on. Beyond F_{RES}, charge-sharing losses again fall below the resistive losses of the switches. With proper choice of L and C, F_{RES} can be reduced to be much lower than transition frequency for the $L = 0$ case.

In this work, C_{FLY} was set equal to the expected output capacitance

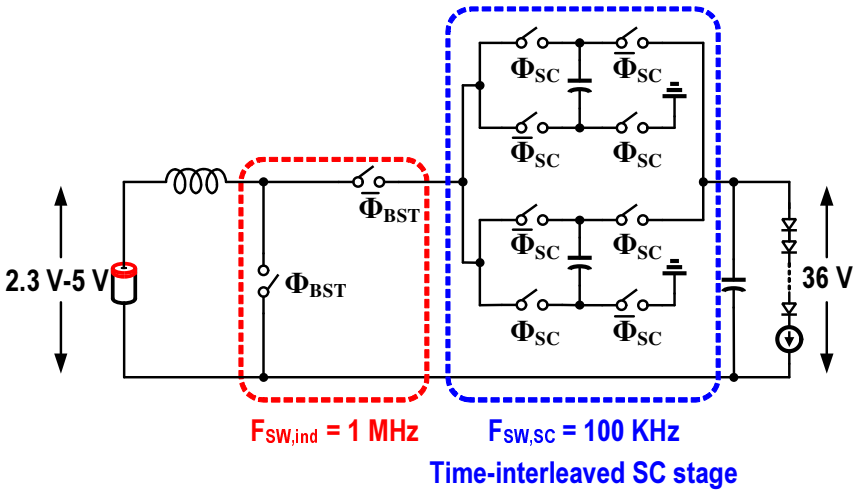

Figure 2.10: Time-interleaving of the SC stage to mitigate large output voltage ripple.

of 400 nF (de-rated) and the inductance is equal to 10 μH. Figure 2.9 shows F_{RES} is 10x lower compared to the L=0 case. It is worth noting that the resonance frequency will be much lower than what is predicted by the above analysis because the inductor is switched and will be equal to $F_{RES,SWITCHED} = F_{RES} * (1 - D)$, where D is the duty cycle with which the inductor is switched. Consequently, it would seem like the SC-stage can be switched at much lower frequency than 70 kHz. But, lowering the switching frequency increases the inductor RMS current significantly, which increases the conduction losses. Because of this tradeoff, losses due to inductor RMS current and the switching losses in the SC-stage are better balanced when $F_{SW,SC} = F_{RES}$. Another practical consideration in choosing $F_{SW,SC}$ involves preventing the inductor from being connected to the SC stage when the flying capacitors are changing phases. This can be guaranteed if $F_{SW,SC}$ is made an integer sub-multiple of $F_{SW,BST}$. Thus, considering the above, $F_{SW,SC}$ was chosen to be 100 kHz, which is the closest sub-multiple of $F_{SW,BST}$ (1 MHz).

2.3.3 Time-interleaved SC stage

While operating the SC-stage at 100 kHz can potentially reduce its switching losses, it has a detrimental effect on the output ripple. For instance, a 50% duty cycle 100 kHz clock for the SC stage results in the output capacitor floating for a duration of 5 μs, which results in an unacceptably large peak-

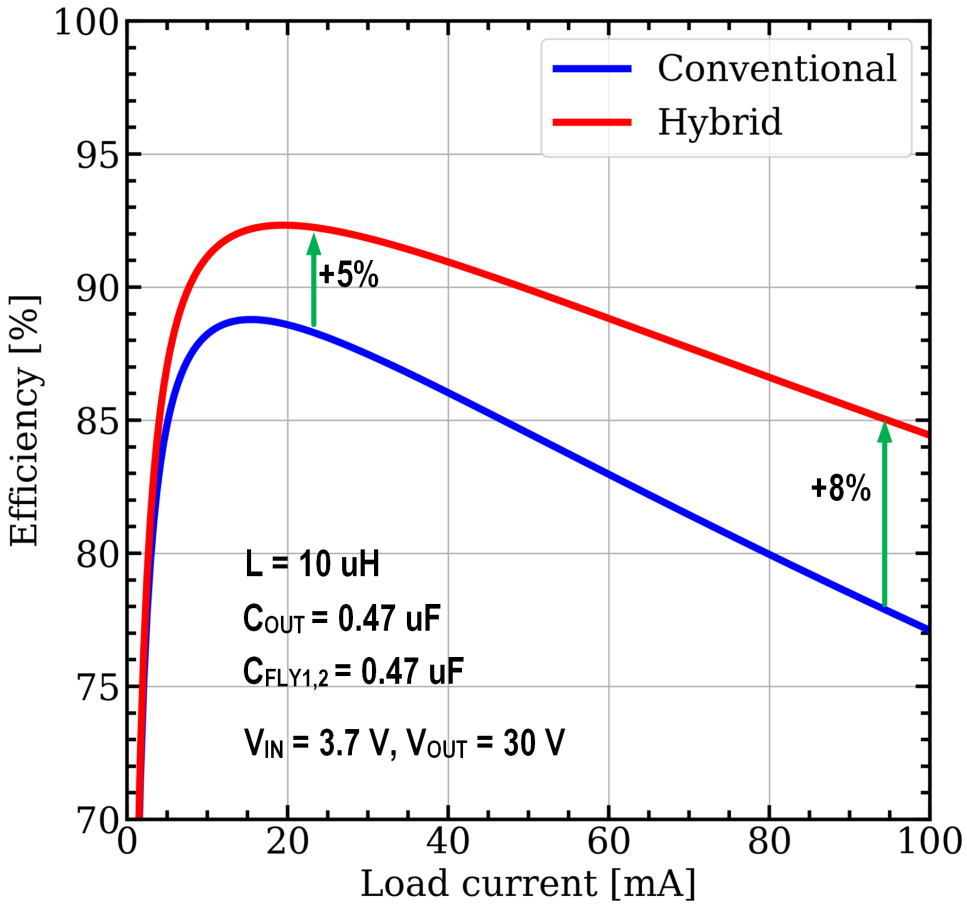

Figure 2.11: Efficiency plots of the hybrid and conventional architectures.

to-peak ripple of 0.25 V at a typical load of 25 mA and a worst-case ripple of 1 V at 100 mA load with 0.5 μF output capacitance. In conventional boost converters, the headroom of the LED bias current source must be increased ($V_{HR} = V_{D,SAT} + V_{RIPPLE}$) to absorb the excessive ripple and prevent it from affecting the backlight quality. However, this degrades LED driver power efficiency and causes perceivable flicker in the backlight. One possible way to avoid this large ripple is to ensure the lost charge in the output capacitor is replenished faster. This can be achieved by splitting the single SC-stage into two time-interleaved sections that alternately connect to the output capacitor. The operation of the converter is described in detail in section 2.3.5. The final architecture of the proposed boost converter is shown

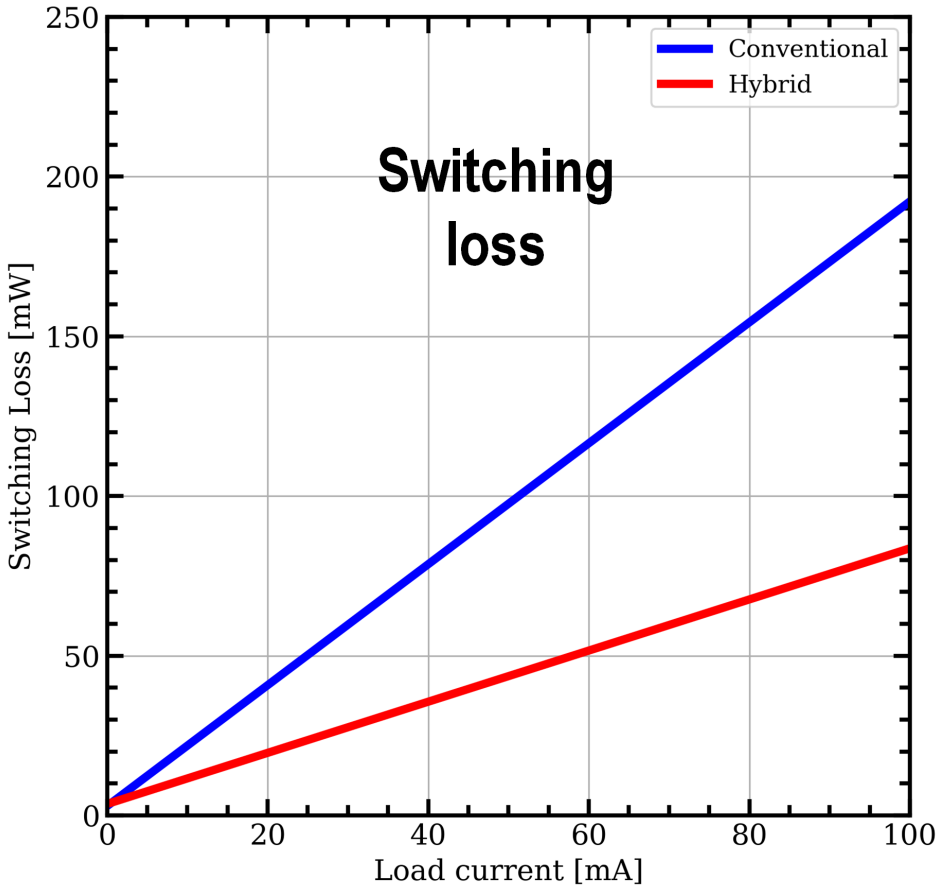

Figure 2.12: Switching loss comparison.

in Fig. 2.10. It consists of 10 power switches, all rated at $V_{OUT}/2$, and two additional external flying capacitors C_{FLY}.

2.3.4 Efficiency and loss breakdown

Theoretical power efficiency plots comparing the proposed hybrid boost converter with the conventional boost converter are shown in Fig. 2.11(a). These plots show a marked improvement in efficiency across the entire load range with about 5% and 8% peak efficiency improvement at nominal and high loads, respectively. The improvement in conduction and switching losses are captured in Figs. 2.11(b) and (c). They show a significant reduction in

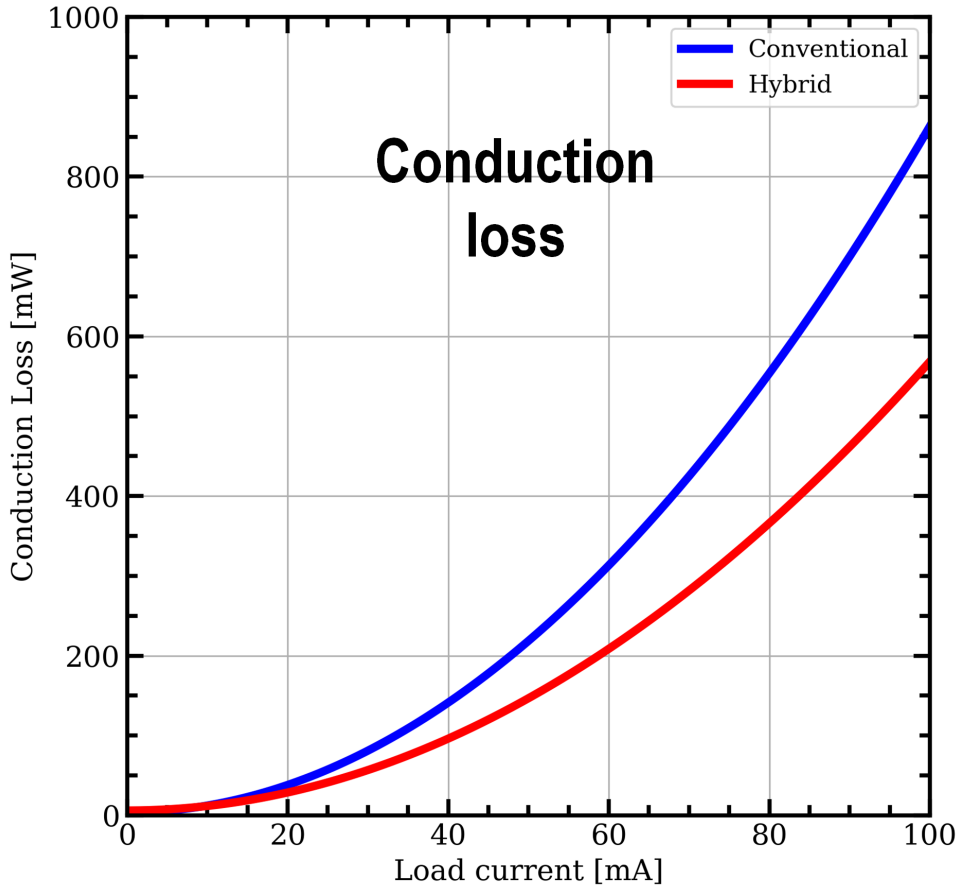

Figure 2.13: Conduction loss comparison.

switching losses and modest improvement in conduction losses, both of which illustrate that higher quality switches and the SC stage's low switching frequency indeed help improve efficiency. The simulated power loss breakdown for the proposed converter at 25 mA load is depicted in Fig. 2.14, and the percentage reduction in losses normalized to those of a conventional inductive boost converter is shown in Table 2.1.

2.3.5 Phase operation

The converter operates in four phases, Φ_1, Φ_2, Φ_3, and Φ_4 (see Fig. 2.15 and 2.16).

Table 2.1: Percentage reduction in losses with respect to conventional inductive boost converter

Loss	% Reduction	Cause
Conduction	30	Device rating
Switching	52	Device rating+low $F_{SW,SC}$
Core	22.6	Inductor current ripple reduced

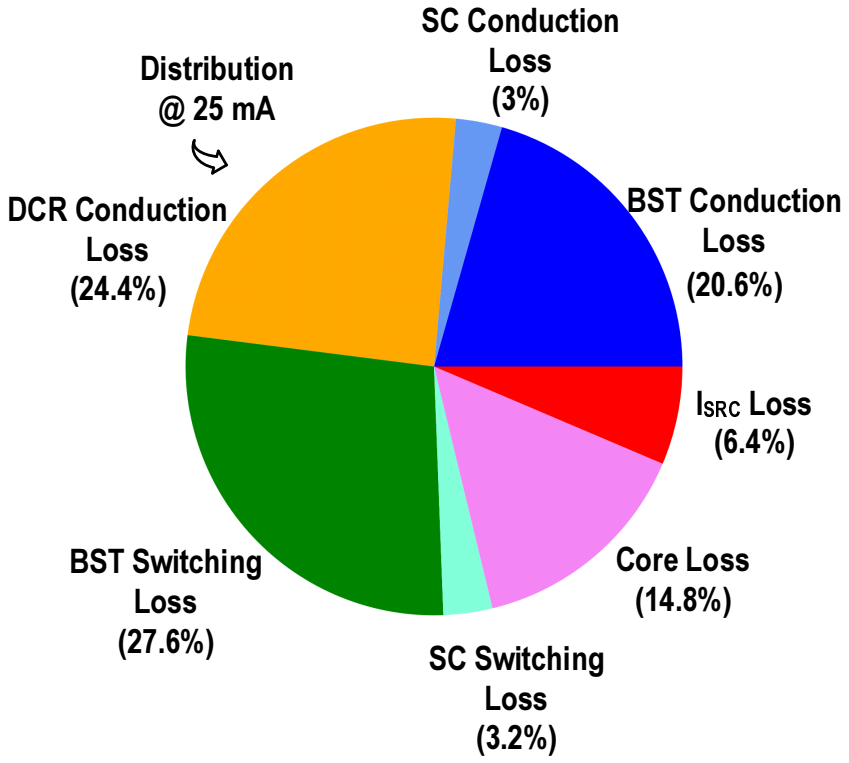

Figure 2.14: Simulated power loss breakdown at 25 mA load for the proposed converter.

We describe the operation starting with phase Φ_1 in which both the boost- and SC-stage clocks ϕ_{BST} and ϕ_{SC} are high. During this phase, inductor and C_{FLY2} are connected to the ground while C_{FLY1} is connected to the output. The duration of this phase is equal to $D * T_{\mathrm{BST}}$ where D is the duty-cycle of the clock ϕ_{BST}, and T_{BST} is the period of ϕ_{BST}. Because the inductor is disconnected from the load, the LED current source discharges the output capacitor. When ϕ_{BST} goes low, the converter enters Φ_2 phase during which inductor is connected to the SC stage. As $V_{\mathrm{OUT}} = 2 * V_{\mathrm{MID}}$, half the inductor current flows through the output capacitor through C_{FLY1} and the other half flows through C_{FLY2}. This causes V_{MID} voltage to ramp-up as shown in the

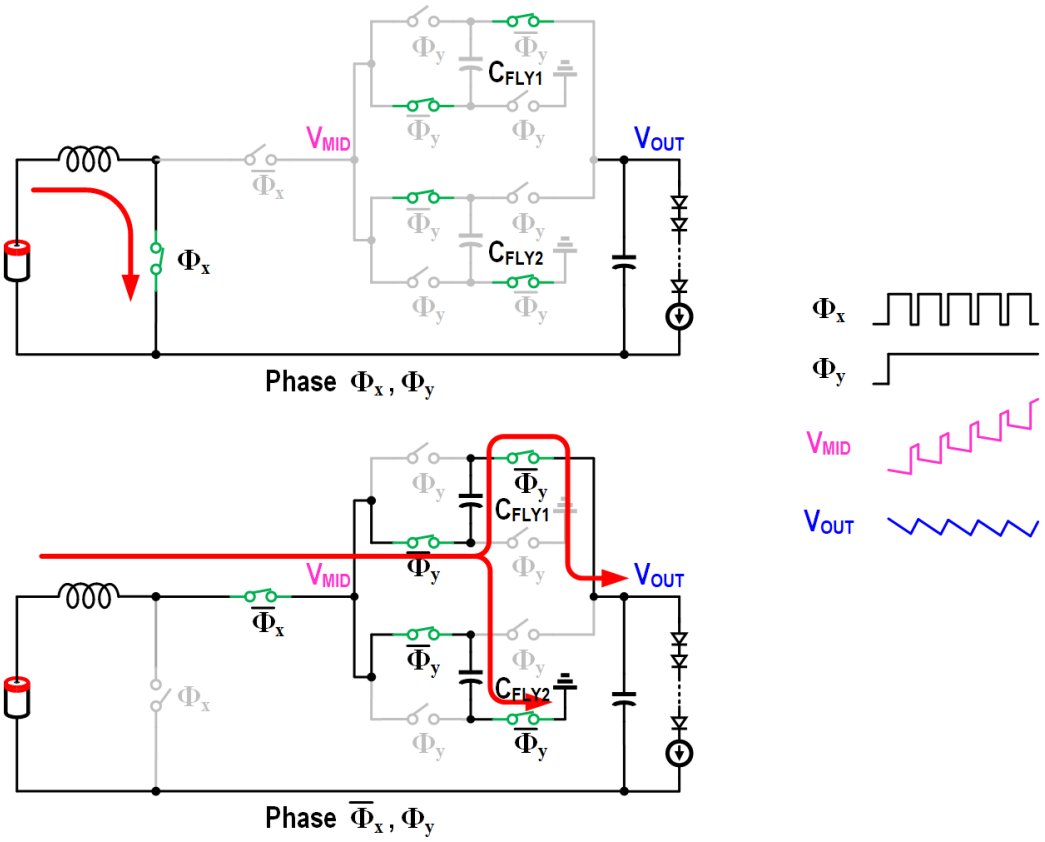

Figure 2.15: Phase-by-phase operation and associated waveforms for phase ϕ_y.

waveforms on the right in Fig. 2.15 and Fig. 2.16. The kink in the ramp is caused by the voltage drop across the power devices in the SC stages. Since switching frequency of the SC stage is much smaller than the BST stage, ϕ_{BST} changes its phase five times in one half of ϕ_{SC}. Consequently C_{FLY1} and C_{FLY2} gets discharged and charged, respectively five times during Φ_2.

In Φ_3 phase, C_{FLY1} and C_{FLY2} exchange positions. Since the voltages across C_{FLY1} and C_{FLY2} always add up-to V_{OUT}, this change in positions of the flying capacitors do not affect the output voltage. The voltage at V_{MID} on the other hand always reflects voltage across C_{FLY2} in ϕ_{SC} and across C_{FLY1} in $\overline{\phi_{\text{SC}}}$. This node experiences a voltage jump when the flying capacitors exchange their positions because the inductor current cannot change suddenly. The voltage jump's magnitude is equal to the voltage difference between the voltages across C_{FLY1} and C_{FLY2} at the end of Φ_2. After this change in flying capacitor positions, rest of the operation is exactly same as described before, except now for the next five cycles of ϕ_{BST}, C_{FLY1} is

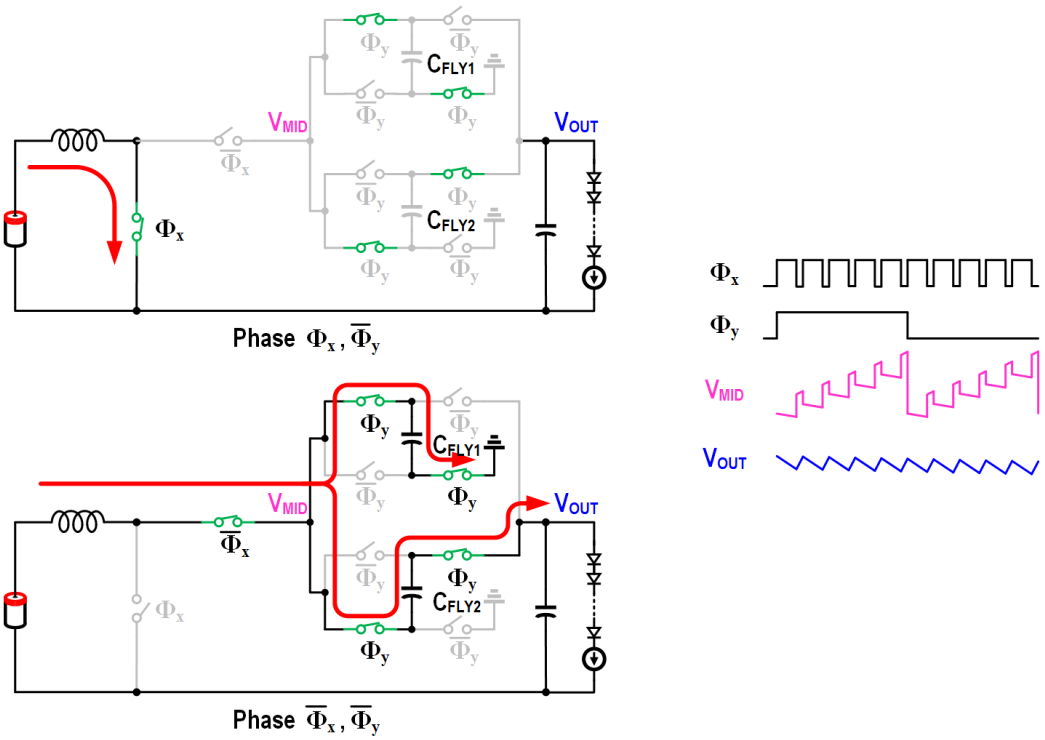

Figure 2.16: Phase-by-phase operation and associated waveforms for phase $\overline{\phi_y}$.

charged and the inductor current discharges C_{FLY2}. This marks the end of one complete cycle of ϕ_{SC}. The BST stage provides a DC gain of $1/(1-D)$, and the SC stage provides a gain of two. Therefore the relation between the output voltage and the BST stage's duty cycle is given by $2/(1-D)$.

2.4 Circuit Implementation

The complete schematic of the proposed converter is shown in Fig. 2.17 and 2.18. It consists of three main components: the power devices used in the BST and SC stages, the gate drivers for these power devices, and circuitry to regulate the converter's output voltage.

2.4.1 Power switches

All the power devices in this architecture are rated at 20 V. The maximum voltage-stress seen by each switch is given by $V_{OUT,max}/2 + I_{OUT,max} * 0.25 *$

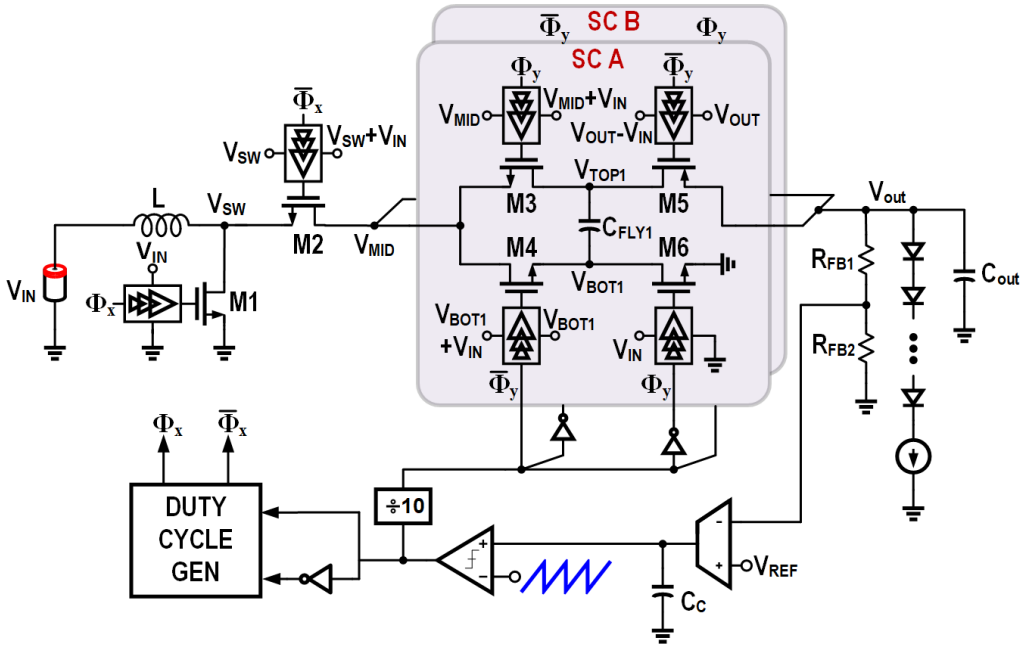

Figure 2.17: Full circuit schematic.

$T_{SW,SC}/C_{FLY}$, and is equal to 18.6 V. $T_{SW,SC}$ $(1/F_{SW,SC})$ is the switching period of the SC-stage. Switch sizing was optimized to achieve peak efficiency at $I_{LOAD} = 25$ mA. The BST stage's low-side switch is sized for an $r_{DS,ON}$ of 123 mΩ, while the rest of the switches are sized for an $r_{DS,ON}$ of 350 mΩ. The power devices occupy an area of 2.76 mm^2. Flip-chip packaging and careful routing of the power rails at both the chip and the PCB level were employed to reduce parasitic resistance and inductance.

2.4.2 Gate drivers

The interleaved SC stage limits the maximum voltage across the power switches to $V_{OUT}/2$, enabling the use of devices rated at $V_{OUT}/2$ with lower $R_{DS,ON}$ and smaller parasitic capacitance. Leveraging this topological benefit for improving efficiency without affecting device reliability requires carefully-designed gate driver circuits. Figure 2.17 and Fig. 2.18 shows these circuits used for driving power devices, M_2, $M_{3A/B}$, $M_{4A/B}$, $M_{5A/B}$ and $M_{6A/B}$, with the desired voltage levels of V_{SW}-to-$(V_{SW} + V_{IN})$, V_{MID}-to-$(V_{MID} + V_{IN})$, $V_{BOTA/B}$-to-$(V_{BOTA/B} + V_{IN})$, $(V_{OUT} - V_{IN})$-to-V_{OUT} and 0-to-V_{IN}, respectively. Drivers for M_1 and M_6 are implemented using tapered buffers oper-

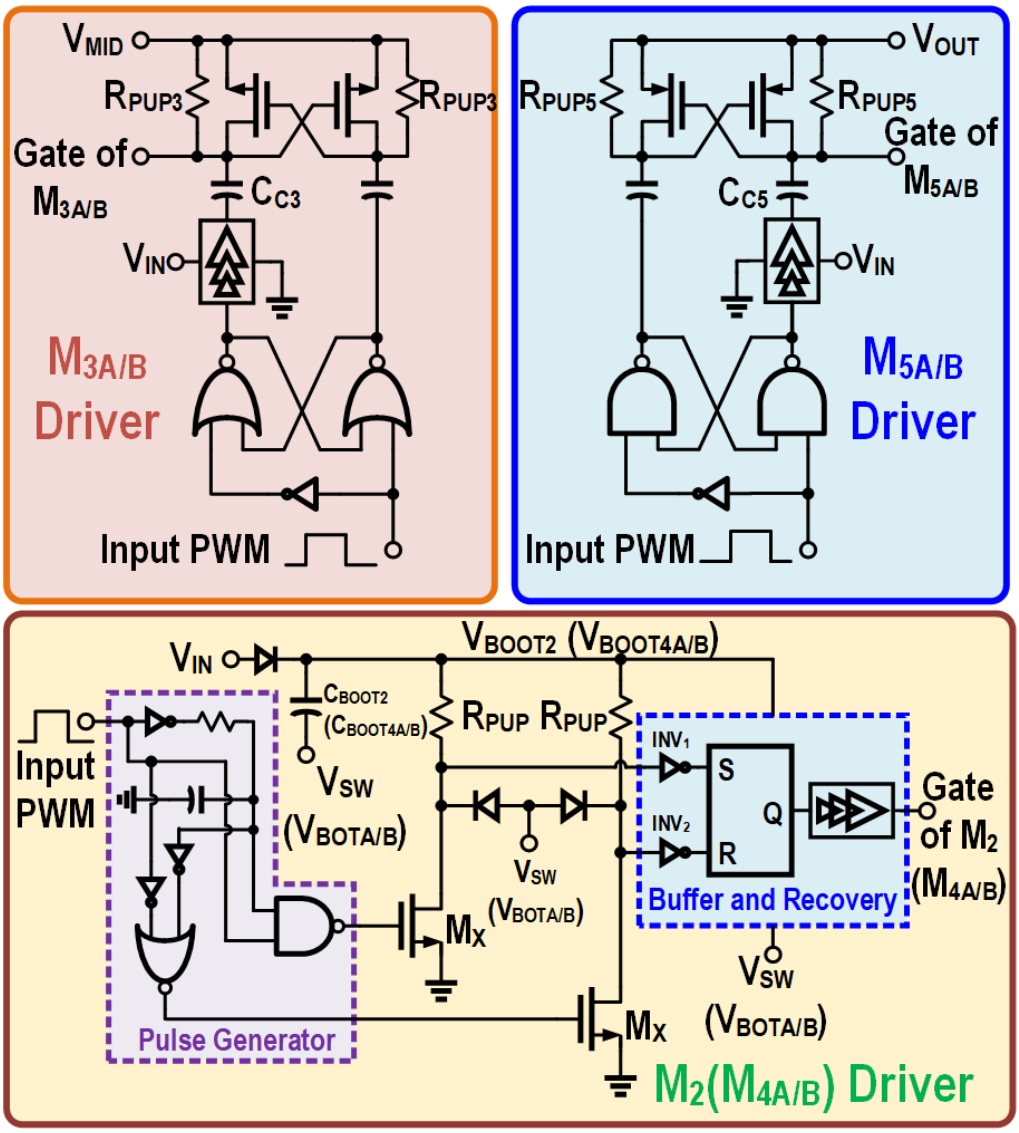

Figure 2.18: Gate-driver details for power devices.

ating with V_{IN} as their supply. M_2 ($M_{4A/B}$) driver is implemented using a dynamic level-shifter [30] with bottom-plate of the boot-strapping capacitor C_{BOOT2} ($C_{BOOT4A/B}$) connected to V_{SW} ($V_{BOT1/2}$). Transistor M_X (rated at $V_{IN} + V_{OUT}/2$) and pull-up resistor R_{PU} are sized such that swing at the inverter ($INV_{1/2}$) input is about V_{IN}. To minimize static power, input PWM signal is converted into two narrow pulses and recovered using an SR latch. M_3 and M_5 drivers are implemented using capacitively-coupled level-shifters [30] wherein coupling capacitors C_{C3} and C_{C5} hold voltages V_{MID} and V_{OUT}, respectively. Pull-up resistors pre-charge capacitors ($C_{C3/5}$) to the

required voltage levels before the start of each switching cycle. The coupling capacitors C_{C3}, C_{C5} and the boot-strap capacitors C_{BOOT2} ($C_{BOOT4A/B}$) are off-chip as they needed to be about 10 times the gate capacitance of the power device they were driving. Both the bootstrap and coupling capacitors are implemented using 1.5 nF 0201 packaged surface-mount capacitors (0.02 in. X 0.01 in.).

2.4.3 Regulation loop

A voltage-mode integral-control loop is used for regulating the output voltage. Note that a current source sets the LED current, and as a result, using a voltage-mode compensator has no bearing on the LED bias current as long as the output voltage is sufficiently high to forward bias all the LEDs and guarantee the desired voltage headroom for the current source. A transconductance-C stage integrates the difference between the converter output voltage and the reference voltage and generates a control voltage (V_{CTRL}). The value of compensation capacitor C_C is equal to 20 nF and it is implemented off-chip. PWM comparator compares V_{CTRL} with an externally fed 1 MHz saw-tooth signal and produces a duty-cycle for the low-side device of the BST stage. The loop bandwidth is about 1 kHz. The clock for the SC stage is generated by dividing the BST stage PWM signal by 10. A ring counter that generates a divide-by-five clock followed by a divide-by-two stage produces the divided-by-10 signal(100 kHz) with 50% duty-cycle. The small-signal model for the proposed architecture has been derived based on the procedure in [16] and is shown below in Fig. 2.19. The duty-cycle to V_{OUT} transfer function is given by Eq. 2.8:

$$G_{vd} = \frac{V_{OUT,DC}}{2D'} \frac{1 - s\frac{4L}{D'^2 R_L}}{1 + s(\frac{4L}{D'^2 R_L} + \frac{4C_{OUT}R_{eq}}{D'^2}) + s^2\frac{4LC_{OUT}}{D'^2}} \tag{2.8}$$

where, D'=1-D, D being the duty-cycle of the low-side switch of the BST stage.

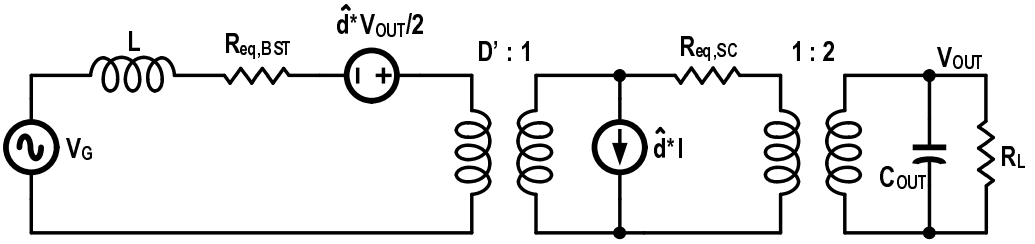

Figure 2.19: Small-signal model for the proposed architecture in continuous conduction mode.

2.4.4 Discontinuous conduction mode

The converter was operated in the discontinuous conduction mode to improve the efficiency under light-load conditions (less than 5 mA). A zero-crossing

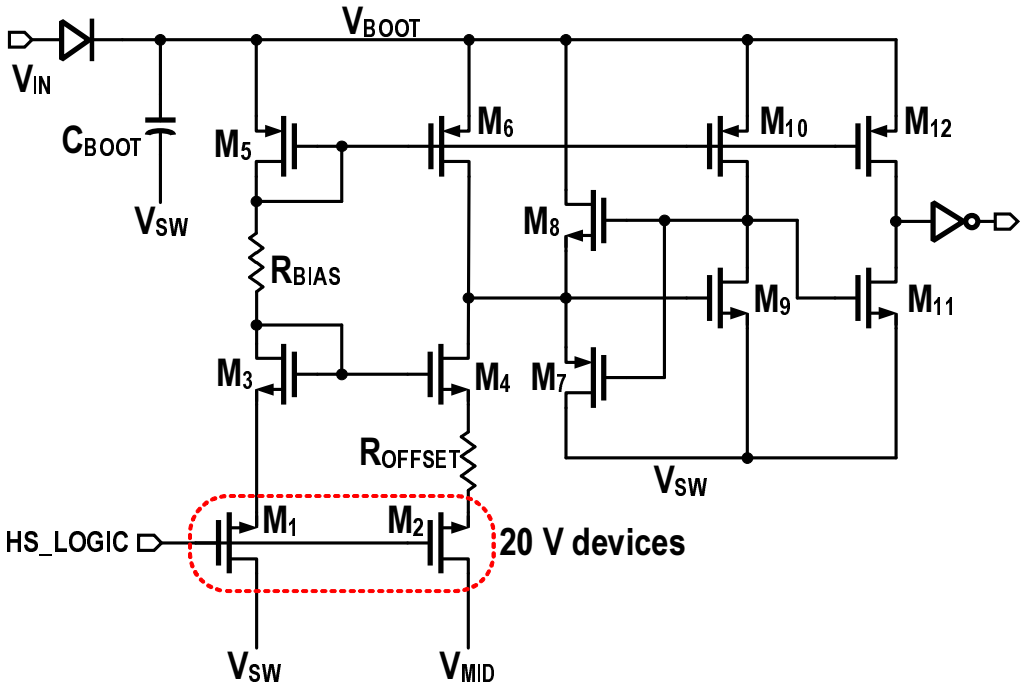

Figure 2.20: Zero-crossing detector circuit used in the discontinuous conduction mode.

detector circuit shown in Fig. 2.20 detects the voltage drop across the high-side power device and translates it to current. This voltage drop appears as difference in V_{GS} of M_3 and M_4 which is then converted into a current equal to $i_{SENSE} = g_{M3,4}\Delta V_{GS}$. Trans-impedance amplifier (TIA) implemented using M_7,M_8,M_9 and M_{10} transistors along with the post amplifier (M_{11} and M_{12})

convert i_{SENSE} into a rail-to-rail voltage output. R_{BIAS} is used to generate an internal bias current, and R_{OFFSET} is used to create an intentional offset to account for the delay in the zero-crossing detector. M_1 and M_2 act as shielding devices to protect rest of the 5 V devices when the V_{SW} node goes to ground potential. The DCM mode improves efficiency by about 10% over the CCM mode at loads near 1 mA.

2.5 Measurement Results

A prototype converter was fabricated in a 180 nm process and attached to the test board using a flip-chip package (see Fig. 2.21). Active area is 2.8 mm^2.

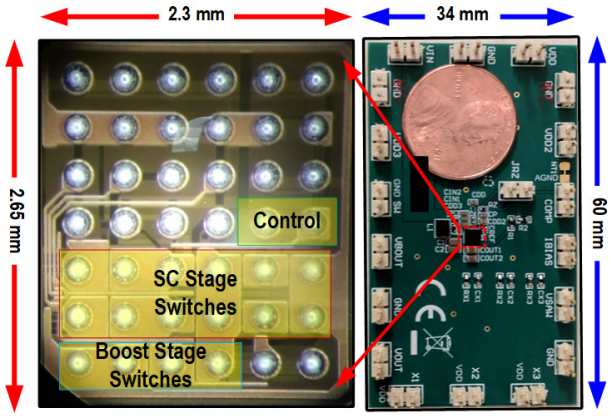

Figure 2.21: Die micrograph and evaluation board.

Flying capacitors (C_{FLY1} and C_{FLY2}) were placed very close to the chip. During start-up, since all the initial flying-capacitor voltages are much lower than their steady-state values, the inductor current increases in both its switching phases, resulting in huge initial inductor current of the order of 2 A (see Fig. 2.25). Since the voltage at V_{MID} toggles between the two flying capacitor voltages, the initial inductor current surge can cause voltage at node V_{MID} to exceed the device rating. To avoid this, the SC-stage switching frequency is initially increased to 500 kHz, which is five times the steady-state switching frequency and reduced back to 100 kHz after $C_{FLY,1}$ and $C_{FLY,2}$ are charged to $V_{OUT}/2$ and the output capacitor is charged to V_{OUT}. In addition to the fast SC-stage switching during start-up, it would also be beneficial to employ an over-current protection scheme to limit the inductor current under

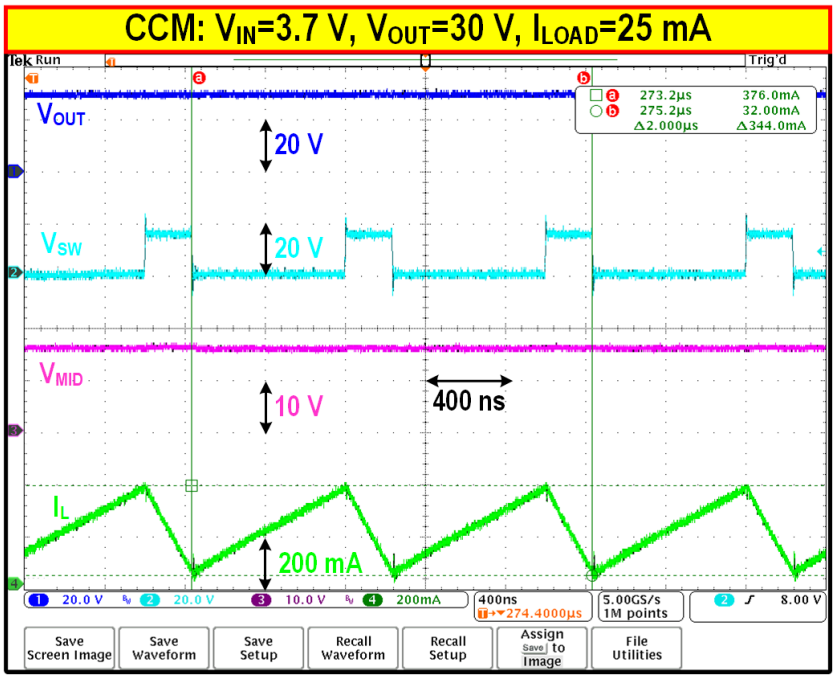

Figure 2.22: Steady-state waveforms in CCM.

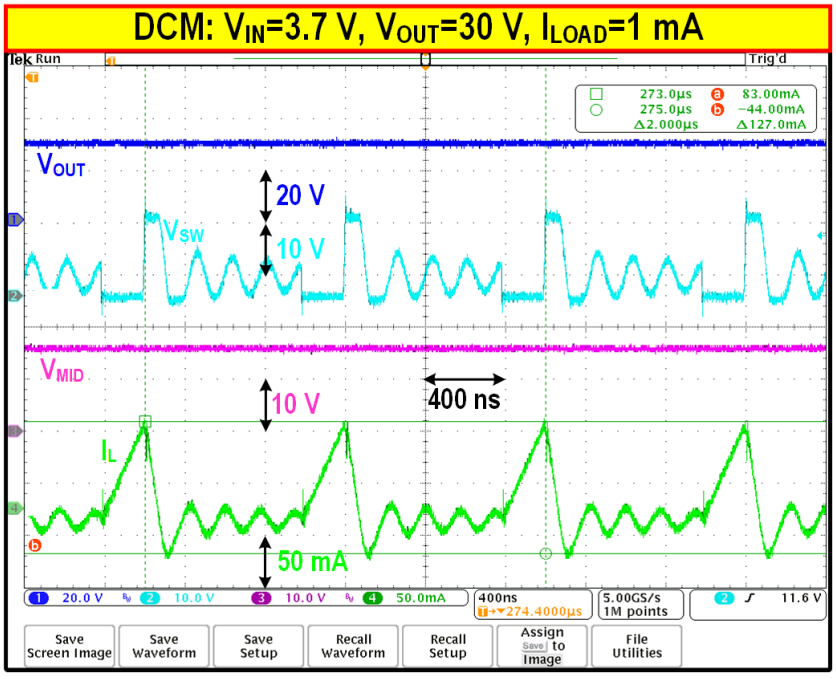

Figure 2.23: Steady-state waveforms in DCM.

a safe value. To this end, a simple over-current protection scheme based on a conventional resistor-based current sensing at the LS power-FET of the BST stage [31] can be employed. Current sensing can also be performed

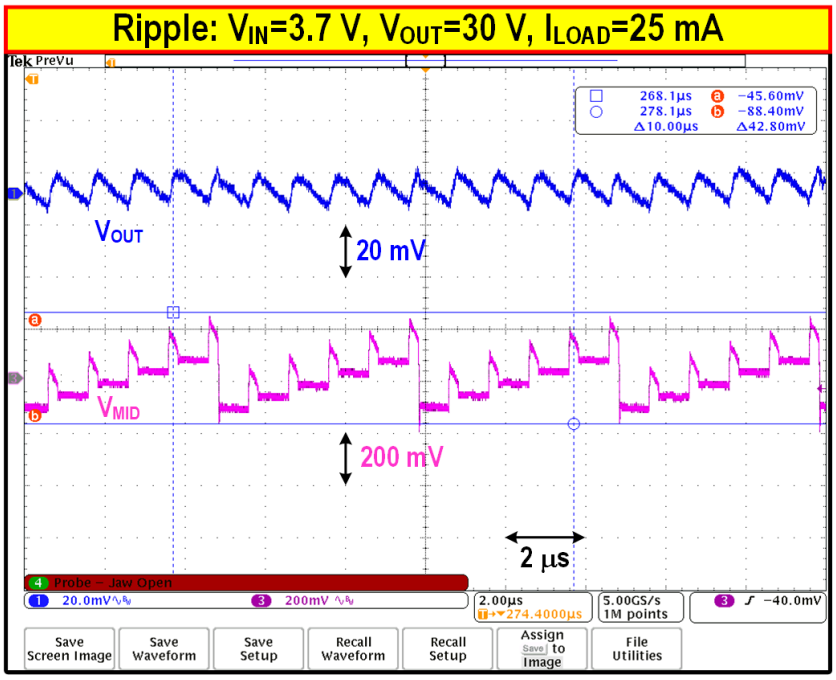

Figure 2.24: Steady-state ripple in CCM at 25 mA load.

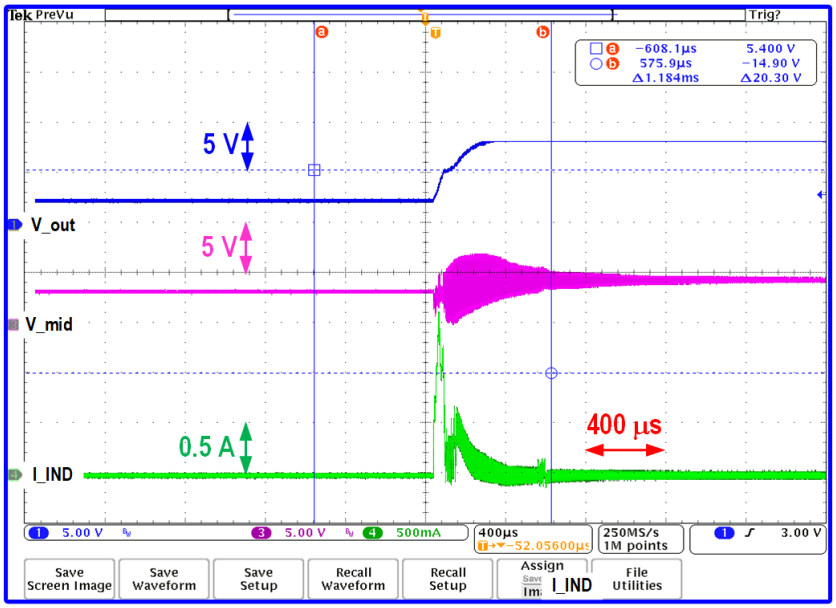

Figure 2.25: Start-up waveforms for V_{OUT}, V_{MID} and I_{IND}.

by a sense-FET based current sensor [32] by placing the sense-FET across the LS power-FET of the BST stage. Relevant steady-state voltages of the converter with $V_{IN} = 3.7$ V, $V_{OUT} = 30$ V and $I_{LED} = 25$ mA in both CCM and DCM modes are shown in Fig. 2.22 and Fig. 2.23, respectively.

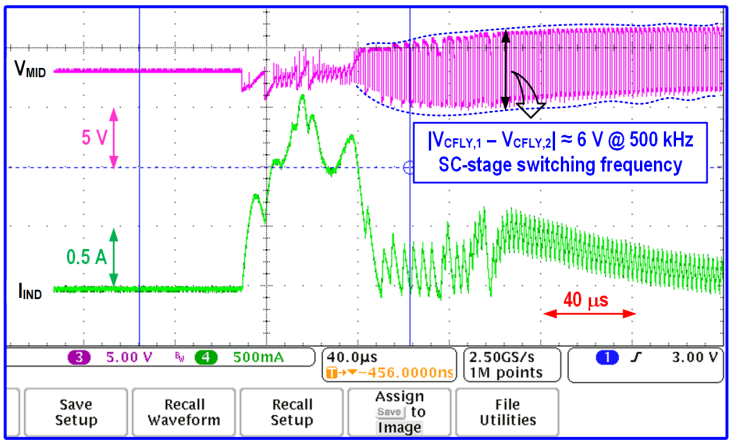

Figure 2.26: Start-up waveforms for V_{OUT}, V_{MID} and I_{IND}, zoomed.

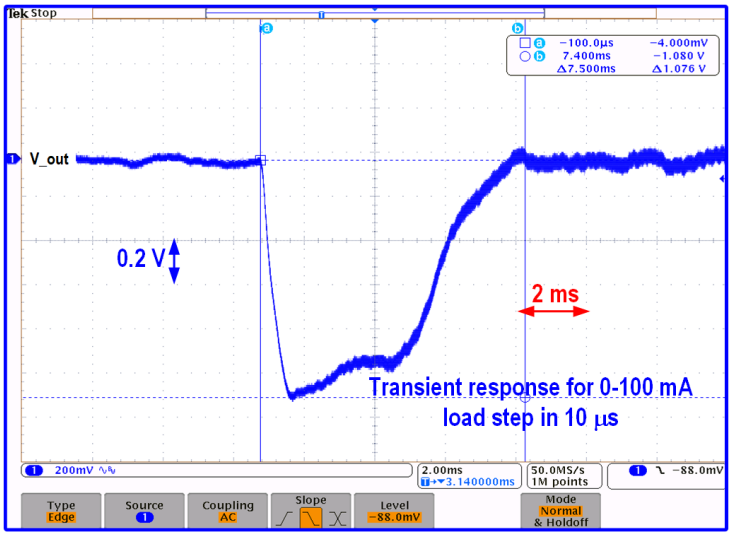

Figure 2.27: Transient response waveforms for V_{OUT}.

Output voltage (V_{OUT}), switching node of the BST stage (V_{SW}), voltage at the intermediate node between the BST and the SC stages (V_{MID}) along with the inductor current (I_{L}) waveforms are shown. V_{OUT} and V_{MID} have settled at 30 V and 15 V respectively for both CCM and DCM operations. In the DCM operation, the ZCD circuit cuts off the high-side switch when the current through it crosses zero. This results in oscillations in V_{SW} and I_{L} as shown in Fig. 2.23, because the parasitic capacitance at V_{SW} node was still charged to V_{OUT} after the high side switch was turned-off. This provided a non-zero initial condition to the LC tank formed by the parasitic capacitance at V_{SW} and inductor L. This results in a small undershoot below zero, in the inductor current.

Table 2.2: Performance summary and comparison to state-of-the-art LED drivers.

	This Work		LM36274 [33]	LM36923 [7]	JSSC '20 [14]	TPE '19 [13]	TPS6118 [8]
Technology	180 nm BCD		180 nm BCD	180 nm BCD	350 nm CMOS	–	–
Input Volt. [V]	2.3–5		2.7–5	2.7–5	2–4.4	6–18	5–24
Max Output Volt. [V]	35		29	28	20	50	40
Load Range [mA]	0–100		0–100	0–100	10–250	70–100	0–120
Conversion Ratio	2/(1-D)		1/(1-D)	1/(1-D)	2/(1-D)	(3-D)/(1-D)	1/(1-D)
Switching Freq.[Hz]	1 M/100 K		1 M	1 M	2 M	$\leq$ 0.82 M	1 M
Output capacitor [μF]	20*		10	10	10	10	4.7
Flying Capacitor [μF]	2×2.2		–	–	2×0.47	2×260	–
Inductor [μH]	10		10	10	2×3.3	18	10
DCR [mΩ]	140	350	140	230	166	–	75
Inductor Vol. [mm^3]	$5 \times 4 \times 1.5$	$2.5 \times 2 \times 1$	$5 \times 4 \times 1.5$	$4 \times 3.2 \times 1.2$	–	–	$5.2 \times 5.2 \times 3$
Efficiency [%]	91.15 (93.6)	90.33	88	88	93.5	89.5	93
Load @ peak eff.[mA]	30 (50)	25	55	40	100	100	100
V_{IN} @ peak eff.[V]	3.7 (5)	3.7	3.7	3.7	4.2	6	11
V_{OUT} @ peak eff.[V]	30 (20)	30	28	28	18.9	30	28.8
Control	Voltage		Current	Current	Voltage	External	Current
Active area [mm^2]	2.76		3.95	2.27	0.89	8	–

* Unfortunately, a larger capacitor was used due to an oversight/error during the PCB design. There is no degradation in efficiency in using a smaller output capacitor.

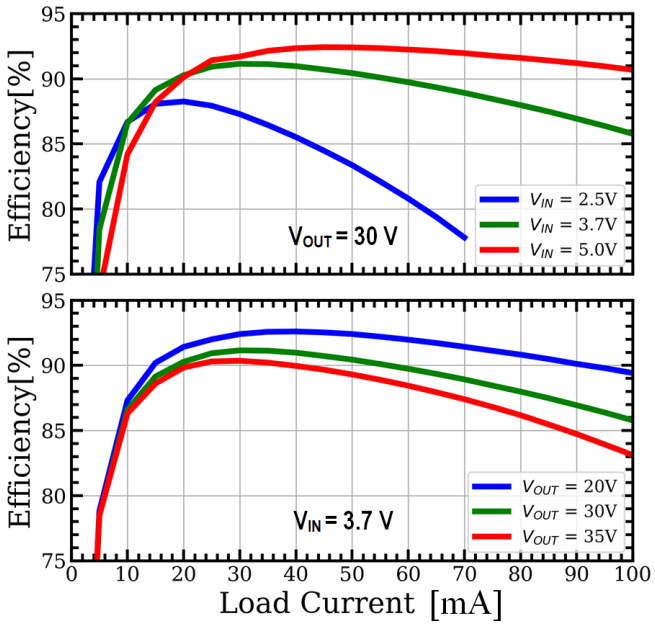

Figure 2.28: Measured efficiencies at different input and output voltages.

Figure 2.24 shows the small-signal ripple on the V_{OUT} and V_{MID} nodes. The expected shapes of ripple on V_{MID} and V_{OUT}, as explained in Sec. 2.3 E, proves the effectiveness of the time-interleaving approach to avoid large ripple on the output voltage. Even though V_{MID} experiences large voltage jumps ($\sim$ 200 mV at I_{LED} = 25 mA) caused by the flying capacitors exchanging positions, thanks to interleaving of the SC-stage, output voltage ripple remains less than 20 mV. Figure 2.25 shows the start-up transients for V_{OUT}, V_{MID} and inductor current I_{IND}. Figure 2.27 shows a full-load step of 0-100 mA causing about a 1 V droop. This is primarily because of the low-bandwidth voltage-mode control loop. Efficiency over a load current range of 0.5 mA-100 mA was measured under different V_{IN}, V_{OUT}, and the results are plotted in Fig. 2.28. These results were obtained by using a 504015 casing (5.0 mmx4.0 mmx1.5 mm) 10 μH inductor (DCR = 140 mΩ). Efficiency curves plotted with V_{OUT} = 30 V and V_{IN} = 2.5 V, 3.7 V and 5 V show peak efficiency of 91.15% at V_{IN} = 3.7 V/I_{LED} = 30 mA and 92.42% at V_{IN} = 5 V/I_{LED} = 45 mA. The converter is functional at V_{IN} = 2.5 V to guarantee overall system functionality even when the battery is almost fully discharged. Efficiency curves measured across three temperatures ($0°C$, $25°C$ and $85°C$),

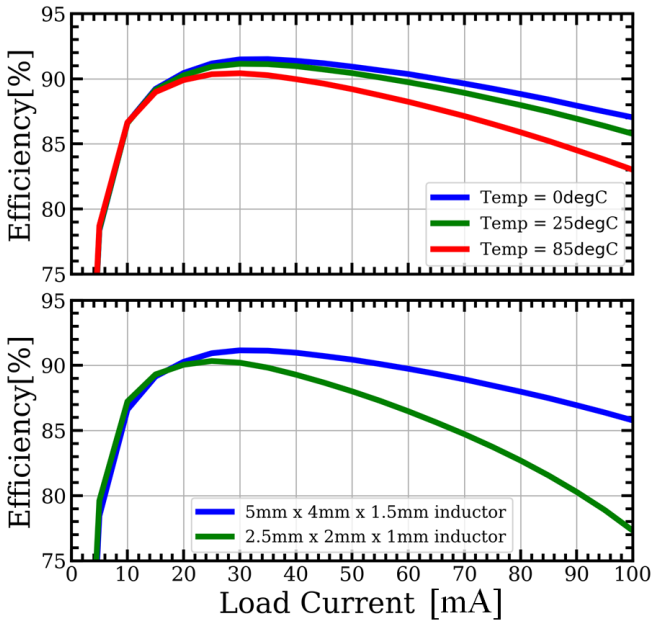

Figure 2.29: Measured efficiencies with different temperature and external inductance at V_{IN}=3.7 V and V_{OUT}=30 V.

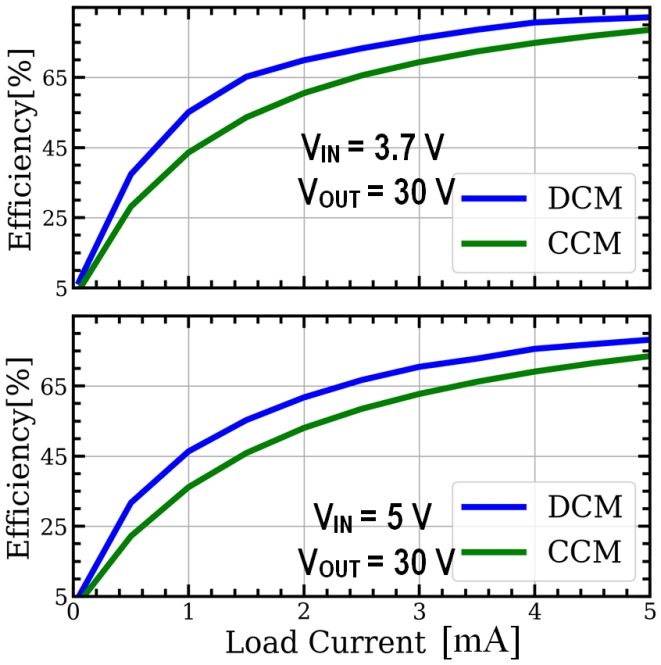

Figure 2.30: DCM efficiency at loads less than 5 mA.

shown in Fig. 2.29, indicate efficiency degrades by less than 2% across the temperature range.

Peak efficiency greater than 90% at $I_{LED} = 30mA$ was obtained even when a smaller volume inductor (25201 casing with DCR = 350 mΩ) is used (see Fig. 2.29). The efficiency in DCM- and CCM-modes is shown in Fig. 2.30. Efficiency is improved by 10% at 1 mA load current in the DCM mode, thus proving the effectiveness of the zero-current detector. Summary of the achieved performance and comparison with state-of-the-art high efficiency LED drivers is shown in Table 2.2. This work achieves more than 3% efficiency improvement compared to [33], [7] which have comparable input and output voltages. Compared to [14], the proposed converter's output voltage is 1.7x larger and doesn't require an extra inductor. In an attempt to have some comparison data, we measured the performance of our converter at V_{IN}/V_{OUT} of 5 V/20 V and 50 mA load current. The peak efficiency was 93.6% when using the 140 mΩ 10 μH inductor. It is difficult to fairly compare this work with [14] because of the differences in the conversion gain (4.5 versus 10), output voltage (20 V versus 35 V), load current (100 mA versus 25 mA), switch ratings (10 V versus 20 V). However, comparing [14] and this work at a conversion gain of 4.5 and load current of 25 mA (after downscaling the losses reported at 100 mA in [14] and keeping the area equal) shows that the total losses in this works are 18% less compared to [14].

2.6 Conclusion

We presented a new hybrid boost converter architecture for improving the efficiency of LED drivers used in mobile applications. By cascading a low-switching frequency time-interleaved series-parallel SC-stage with an inductive boost converter, we demonstrated that switching losses can be greatly reduced. Charge-sharing losses of the SC stage are minimized by soft-charging flying capacitors with the inductor of the boost stage. Fabricated in 180 nm BCD process, the prototype converter generates 30 V output voltage from a Li-ion battery source and can provide a load current in the range of 0 to 100 mA with an excellent peak power efficiency of 91.15% at 30 mA. Compared to state-of-the-art designs, the proposed converter achieves a 3% improvement in peak power efficiency.

CHAPTER 3

A 1% LINEAR DUTY-CYCLE SENSOR FOR CURRENT SENSING APPLICATIONS IN BUCK CONVERTERS

3.1 Introduction

Current sensing in DC-DC power converters is required for several reasons. Most common applications include filter based inductor-current sensor used in current mode control schemes [34],[3]. Embedded software of portable devices such as mobile phones and tablets, need the DC load current information to optimise their operation, enhancing battery life [35] [2]. Such optimisations include reducing system clock frequency, shutting down modules not required by the currently operations and estimating available battery life for portable devices. Output current sensing is needed in over-current detection modules which protect the DC-DC converter and the PCB from excessive currents [36]. Even though the sensing accuracy requirement is driven by the application, higher accuracy leads to lesser overhead in design. For instance, a 10 A over-current sensor with 20% inaccuracy can trip anywhere between 8 A and 12 A. For applications requiring 8 A current limit, the system must handle up-to 12 A resulting in significant overhead in design.

Reported current-sensing schemes can be broadly divided into two categories: filter-based and current-mirror based approaches. The filter based approach, primarily used in current-mode control schemes, essentially emulates the inductor-ESR time constant with an RC-filter placed in parallel with the inductor as shown in Fig. 3.1 [34]. The time-constant matching requirement, makes this approach very sensitive to temperature variation and manufacturing tolerances of passive components, resulting in a large sensing error of $\pm 25\%$. Replacing the passive filter with an active filter and calibrating its time constant leads to a reduced error of $\pm 18\%$ [37], but remains sensitive to inductor variation across the load range.

The current-mirror based approach produces a scaled copy of the current

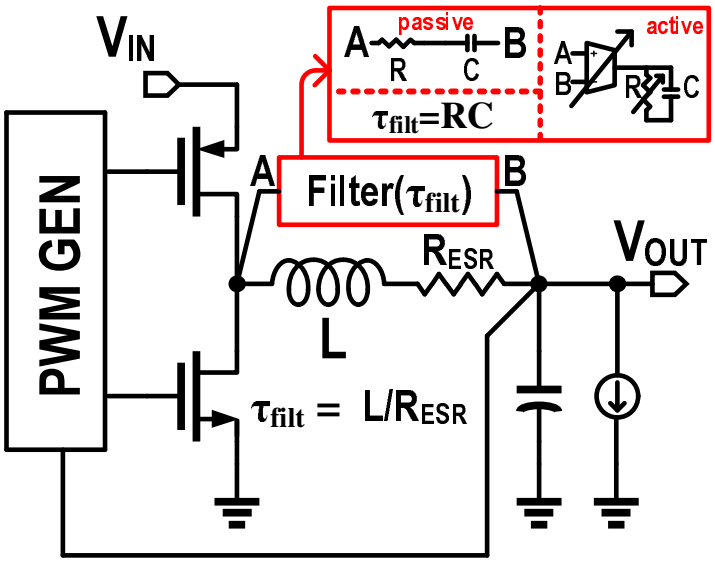

Figure 3.1: Filter-based current sensing.

through the high-side(or low-side) FET, M1, using a replica FET, M3, as shown in Fig. 3.2. This approach achieves a better performance of ±4% [38][39]. It is primarily limited by matching errors in the replica MOSFET and offset and settling errors in the amplifier used for matching drain voltages for both the main and the replica MOSFETs.

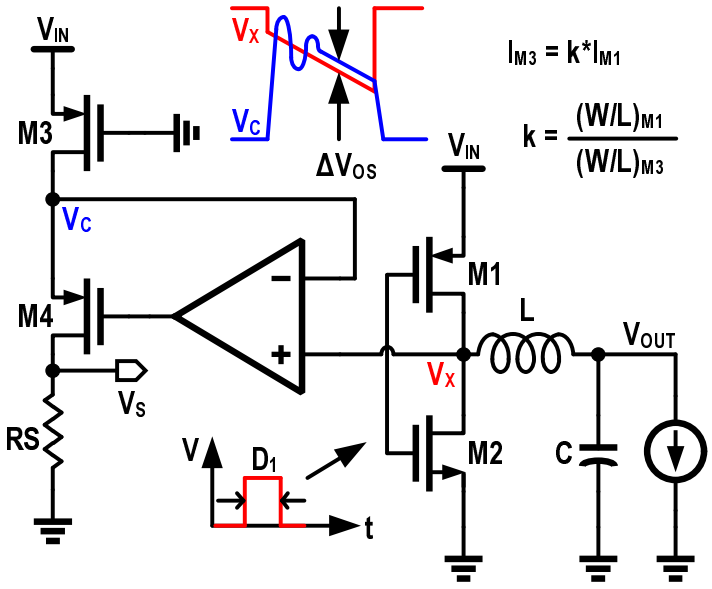

Figure 3.2: Replica current based current-sensing.

We observe that the duty-cycle of a well-regulated DC-DC power converter

carries the load current information and hence can be used for current sensing. This paper explores an alternative approach that uses duty-cycle as a sensing variable for load current. As will be discussed later, duty-cycle exhibits a linear proportionality with load-current of regulated inductive buck converter. Hence the converter output voltage and the PWM control signal are assumed to be available from outside for the validation of this work.

Rest of the paper is organized as follows. Section 3.3 presents the proposed architecture. Circuit implementation details of key building blocks are described in Section 3.4. Experimental results from the test chip are presented in Section 3.5. Key contributions of this paper are summarized in Section 3.6.

3.2 Duty-cycle as sensing variable

In a regulated DC-DC buck converter, the duty-cycle of the power switches change to maintain the desired output voltage across the output current range. This can be understood by using the average model of the power converter as shown in Fig. 3.3. In the model, R_{out} represents the effective resistance along the output current path and is expressed by Eq. 3.1.

$$R_{out} = D * R_{on,M1} + (1 - D) * R_{on,M2} + R_{ESR} \tag{3.1}$$

where, D is the duty-cycle of the buck converter.

Under no-load condition, the duty-cycle of the low-side FET is given by Eq. 3.2. When the buck converter is placed under a non-zero load condition, the PWM controller compensates for the voltage drop across this resistor by increasing the duty-cycle of the buck converter. Let the duty-cycle with no load and some non-zero I_{LOAD} be D_1 and D_2 respectively. Then from the average model it follows that,

$$V_{OUT} = D_1 * V_{IN} \tag{3.2}$$

$$V_{OUT} = D_2 * V_{IN} - I_{LOAD} * R_{OUT} \tag{3.3}$$

Subtracting Eq. 3.2 from Eq. 3.3, we get the following expression.

$$\Delta D = I_{LOAD} * R_{OUT}/V_{IN} \tag{3.4}$$

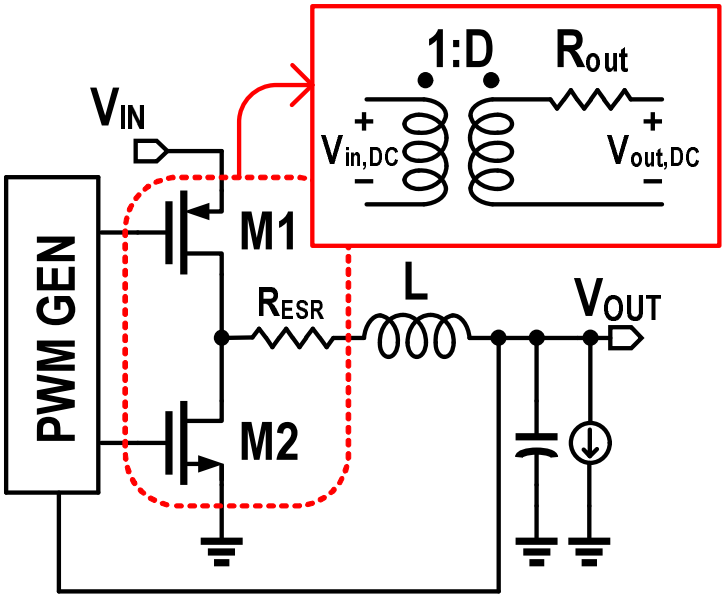

Figure 3.3: Average model for buck converter.

Eq. 3.4 shows that, for a fixed R_{OUT} and V_{IN} the excess duty-cycle from the PWM controller with respect to the no-load duty-cycle has a linear relationship with the load current as shown in Fig. 3.4.

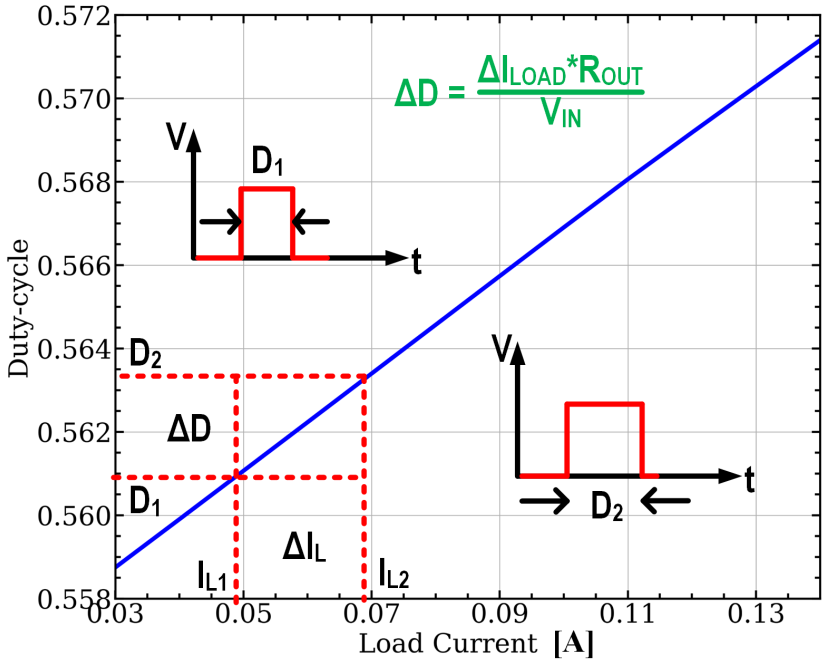

Figure 3.4: Load current information in duty-cycle.

3.2.1 Sources of error

Since slight changes in D also changes R_{OUT}, the assumption of R_{OUT} being fixed across the output current range needs to be reconsidered. But for high-efficiency buck converters with low R_{out} values, the change in R_{out} is much less than the change in duty-cycle and results in a very small linearity error. For instance, 1.8 V V_{IN}, 1 V V_{OUT} with a load range of 0 to 16 A and $R_{ON,HS}$, $R_{ON,LS}$ being 10 mΩ and 4 mΩ respectively, results in only 0.8% change in the output impedance from no-load to full-load, as shown in Fig. 3.5.

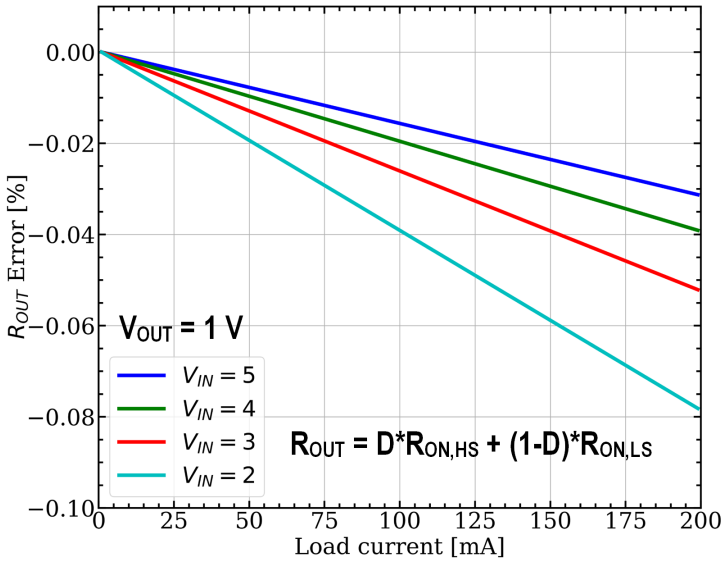

Figure 3.5: Percentage R_{OUT} variation with load current for a DC-DC buck converter.

Another source of error non-zero dead-times in the switching cycle. This leads to excess voltage drop due to the load-current dependent reverse-bias diode drop of the power switches. As the load current increases, the reverse-bias of the body diode increases during the dead-time. This results in excess duty-cycle from the PWM controller in order to account for this voltage drop and maintain the required output voltage. This is shown Fig. 3.6, where a 1.8 V/1 V V_{IN}/V_{OUT} DC-DC buck converter was simulated and the duty-cycle obtained through simulation is compared the duty-cycle derived from Eq. 3.3. The difference in slope is attributed to the dead-time dependent duty-cycle changes.

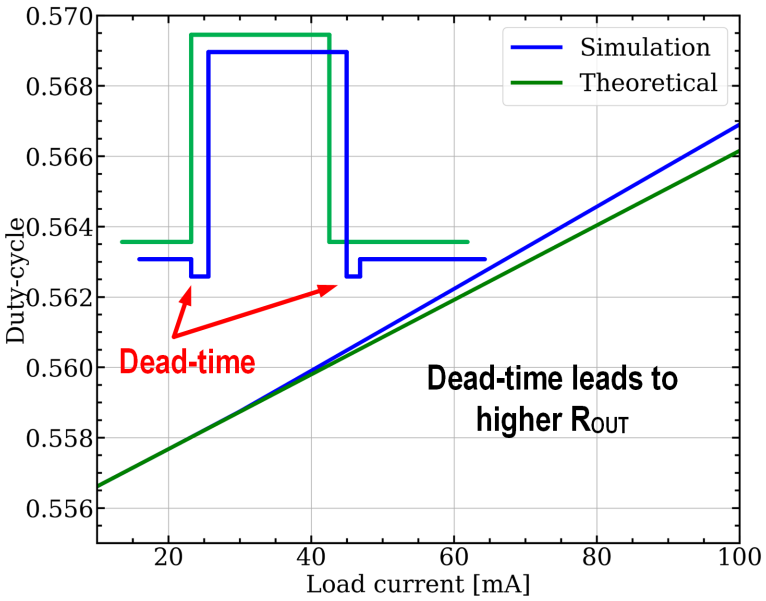

Figure 3.6: Comparison of theoretical and simulated duty-cycle variation for 1.8 V/1 V V_{IN}/V_{OUT}.

The third type of error is due to the varying input voltage. The input voltage can change during operation, which will also produce very large changes in duty-cycle. Therefore, a reference current might be required to calibrate the sensor periodically. This reference current can be generated by a band-gap reference and external resistor. The excess duty-cycle due to this known reference current can be used as a reference for measuring the actual load current.

Other errors include self-heating induced changes in LDMOS ON resistance variation, finite rise and fall times of the gate driver output signals driving the gates of LDMOS, causing non-linearity in the measured current value. The measured current value therefore needs to calibrated to account for these errors and also digitised in order to be easily used by the microprocessors which will use this information to optimise their operation. Hence we propose a time-based ADC for digitising the duty-cycle of the power converter. In this prototype, an externally fed PWM signal is digitised without actually implementing the power converter.

3.3 Proposed Architecture

This section introduces the proposed duty-cycle sensor architecture and the analysis required to describe it's operation.

3.3.1 Duty-cycle sensor architecture

The basic idea of the sensor architecture is illustrated in Fig. 3.7. It consists of an analog integrator ($G_m - C$), analog duty-cycle subtractor, an inverter (M1,M2) and an RC-filter to extract the DC output of the inverter. The objective of the loop is to extract the duty-cycle difference between a loaded and an unloaded buck-converter. M1 and M2 make up the replica unloaded converter. Since it carries no DC current, M1, M2 resistances are not important. This avoids any matching requirement with the main buck power stage. Because a no-load buck converter would require smaller duty-cycle to get the same output voltage as a loaded buck-converter, a duty-cycle subtractor consisting of an analog controlled delay generator and an AND gate is used. The analog delay block generates a delay proportional to the integrator output voltage($K_\tau V_{CTRL}$), which is subtracted from the duty-cycle of the loaded converter(D) and the resultant duty-cycle(D') is applied to the replica buck-converter. The output of this replica converter(D'V_{IN}) is low-pass filtered and fed back into the intergrator, closing the loop. The negative feedback forces the replica converter output(D'V_{IN}) to be the same as the buck-converter output voltage(V_{OUT}). This in-turn forces the integrator output voltage(V_{CTRL}) to be linearly proportional to the duty-cycle difference(ΔD) between the loaded buck-converter and the unloaded replica converter. The accuracy with which the integrator output represents ΔD depends on the loop gain, which is defined by Eq. 3.5. Here K_τ is the gain of the analog delay generator with units of s/V and T_s is the period of the power converter PWM signal, which for this work is 1 MHz.

$$LG(s) = \frac{G_m R_{out}}{(1 + sR_{out}C_{comp})(1 + sR_{LPF}C_{LPF})} * \frac{K_\tau}{T_{PWM}} \tag{3.5}$$

The variation in duty-cycle depends on the load range, R_{OUT} and V_{IN}, as seen in Eq. 3.4. For this work, Fig. 3.4 shows the duty-cycle variation. This is for a 1.8 V_{IN}, 1 V_{OUT} DC-DC buck converter over a load range of

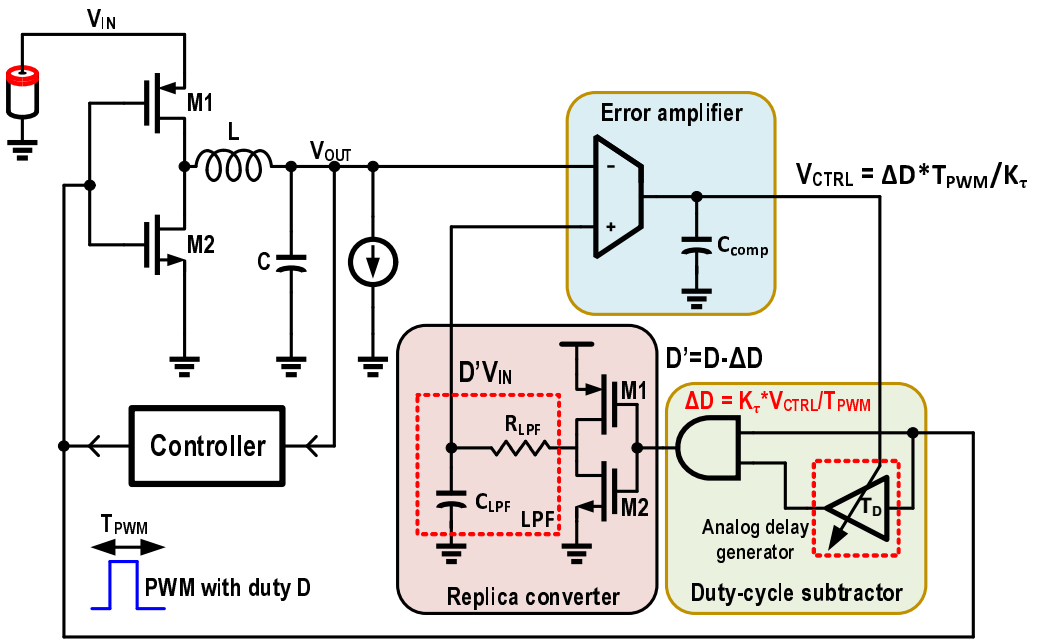

Figure 3.7: Conceptual duty-cycle analog loop.

30 mA-140 mA. The output impedance for this converter is about 200 mΩ. Such a choice was made keeping in mind the 1 V supply voltage for the microcontroller and the 1.8 V input for the buck converter supply. Since the maximum duty-cycle to be measured is about 20 m at 1 MHz switching, the analog delay generator needs to produce a linearly controlled delay in the range of several nano-seconds, which is difficult to achieve in an analog implementation. In order to circumvent this issue, a 1-bit delay DAC was used as shown in Fig. 3.8. This 1-bit delay DAC consists of a single delay element and a digital multiplexer which selects between the delayed and undelayed PWM input. The select bit of the multiplexer is derived from a 1-bit voltage quantizer implemented as a clocked comparator at the output of the error amplifier. The sampling clock of the comparator can be the same as the PWM clock of the converter. Since a 1-bit delay DAC is inherently linear, the average value of the bit-stream at the select bit of the multiplexer represents the ΔD required to produce the output voltage from the replica converter. The quantisation noise in the bit-stream has a large harmonic content due to the DC nature of the ΔD input, as shown in Fig. 3.9. This results in poor SQNR within the signal bandwidth.

In order to improve SQNR and reduce the harmonic content in the quantisation noise, a VCO-based quantiser [40] is used instead of the comparator,

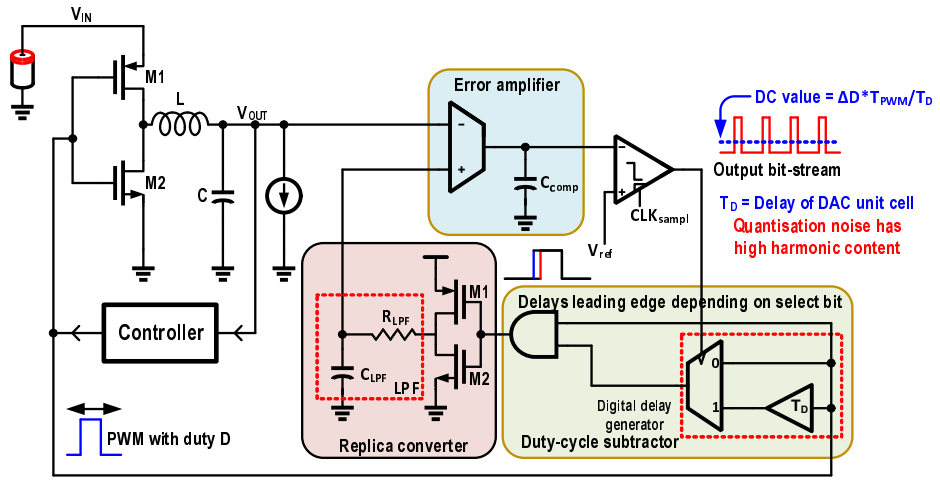

Figure 3.8: Digital loop implementation with 1-bit delay-DAC and clocked comparator.

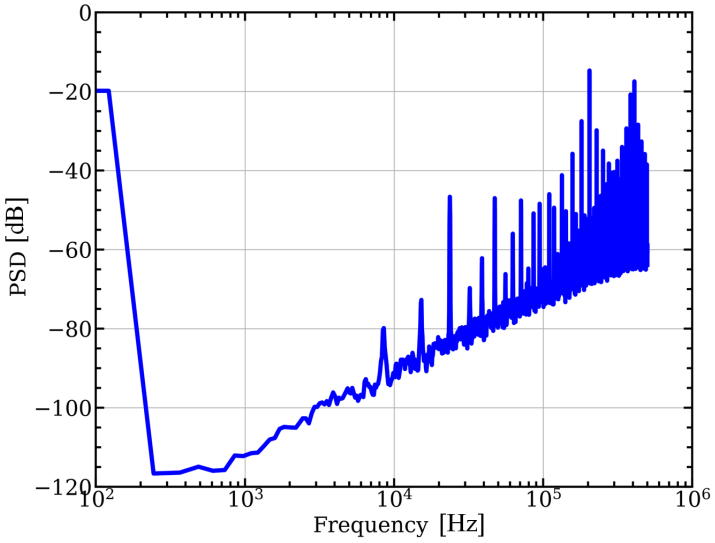

Figure 3.9: Power spectral density at the output of the clocked comparator.

as shown in Fig. 3.10. This results in second-order noise-shaping within the loop bandwidth and first-order noise-shaping beyond the loop-bandwidth, with significant reduction in low-frequency harmonic content. The PSD of the output bit-stream is shown in Fig. 3.11. The loop gain transfer function with the VCO-based quantiser is shown in Eq. 3.6, where T_{vco} is the vco output period and $\Delta D_{max} * T_s$ is the delay provided the 1-bit delay DAC.

$$LG(s) = \frac{G_m R_{out} * \Delta D_{max}}{(1 + sR_{out}C_{comp})(1 + sR_{LPF}C_{LPF})} * \frac{2T_s}{T_{vco}} \tag{3.6}$$

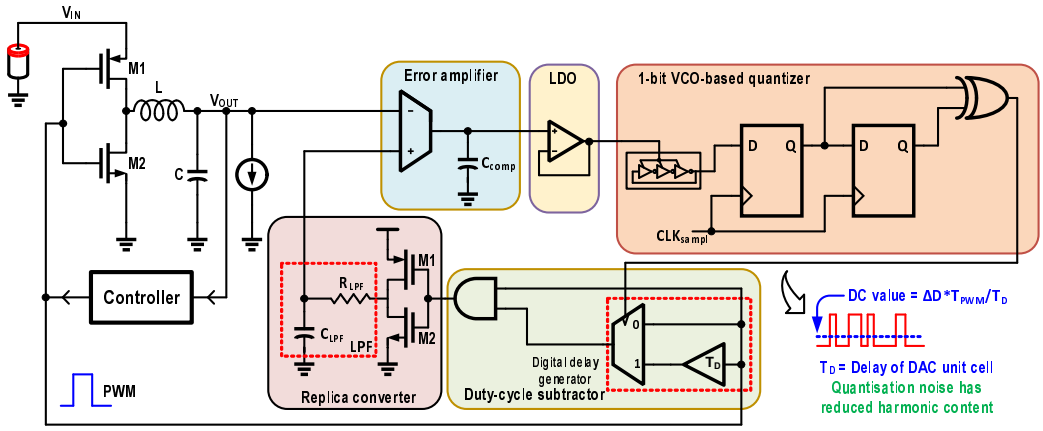

Figure 3.10: Digital loop implementation with VCO-based quantiser for second-order noise shaping.

Figure 3.11 shows the simulated PSD of the output bit-stream for a DC ΔD input of 4 m with a sampling frequency of 1 MHz. The vertical lines represent cut-off frequency for an ideal filter with the corresponding OSR and SQNR numbers in their respective boxes. Thanks to the extra-order of noise-shaping from the VCO-based quantiser, low frequency harmonic content is negligible, while the higher frequencies display significant tonal behaviour. The loop-bandwidth was designed to be 1 KHz. The VCO phase-noise and input noise from the buck-converter output fills up the low-frequency noise floor. Beyond the loop-bandwidth, 20 dB/decade noise shaping comes from the VCO-based quantiser.

In addition to the change in R_{out}, finite loop gain of the PWM control also contributes to the error in ΔD at a given load current. Minimum ΔD to be measured and the accuracy requirement dictates the loop gain necessary to meet the desired specifications. This minimum ΔD needs to be fixed based on the load range and R_{out} of the power converter which varies widely with applications. The minimum voltage $I_{load}R_{out}$(directly proportional to ΔD) which a current sensing scheme can measure, is a more convenient way of comparing existing current sensing architectures with the proposed approach. The conventional scheme(see 3.2) can measure $I_{load}R_{out}$ as low as 12 mV [38]. This work targets to measure a minimum $i_{load}R_{out}$ of about 5 mV(R_{out} = 200 mΩ, V_{IN} = 1.8 V, ΔD_{min} = 3 m) with at-most 1% error which translates to a PWM control loop gain of at-least -20*log(0.01*0.005)=86 dB.

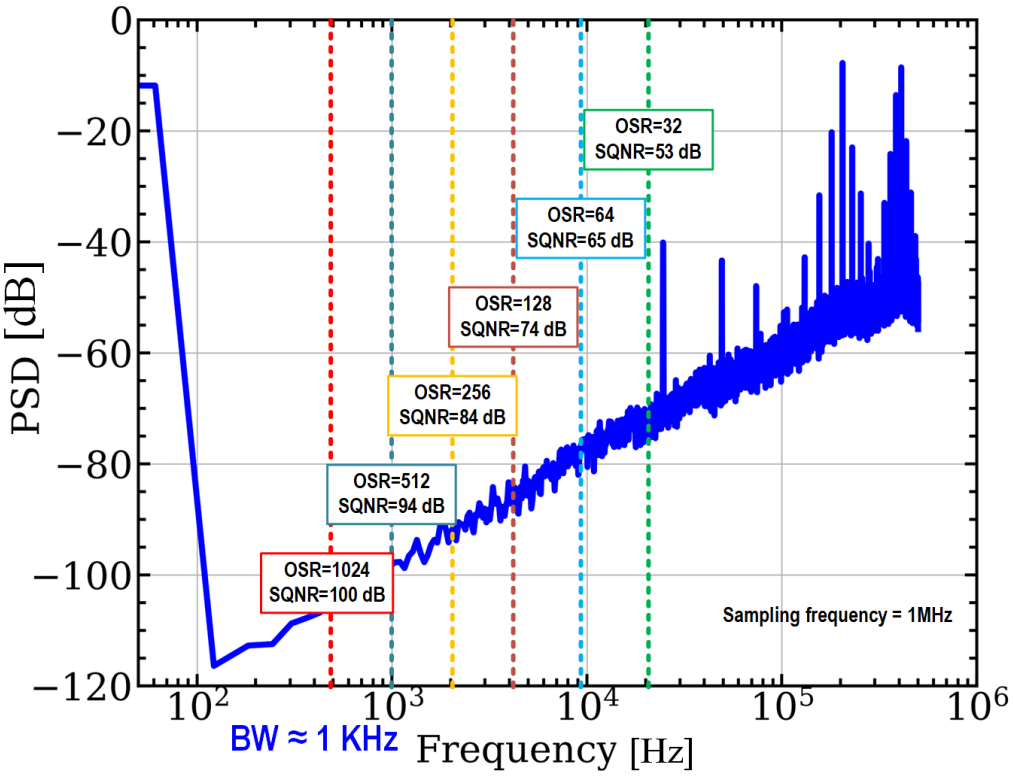

Figure 3.11: Power spectral density for a fixed duty-cycle input.

3.4 Circuit Implementation

The key building of the duty-cycle sensor loop is discussed in this section.

3.4.1 Error amplifier

The error amplifier gain is critical to maintain the overall loop gain of the duty-cycle sensing loop. Figure 3.12 shows a two-stage amplifier with an overall gain of 100 dB was used with the miller capapcitor forming the dominant pole in the loop transfer function. Chopping switchs are placed at the input and de-chopping switches are placed at the output of the folded-cascode stage of the amplifier in order to reduce flicker noise and offset-errors.

3.4.2 Delay cell and replica buck converter

Provided a certain switching frequency, the delay-cell specifies the maximum duty-cycle difference the sensor loop will detect. For a 1 MHz switching

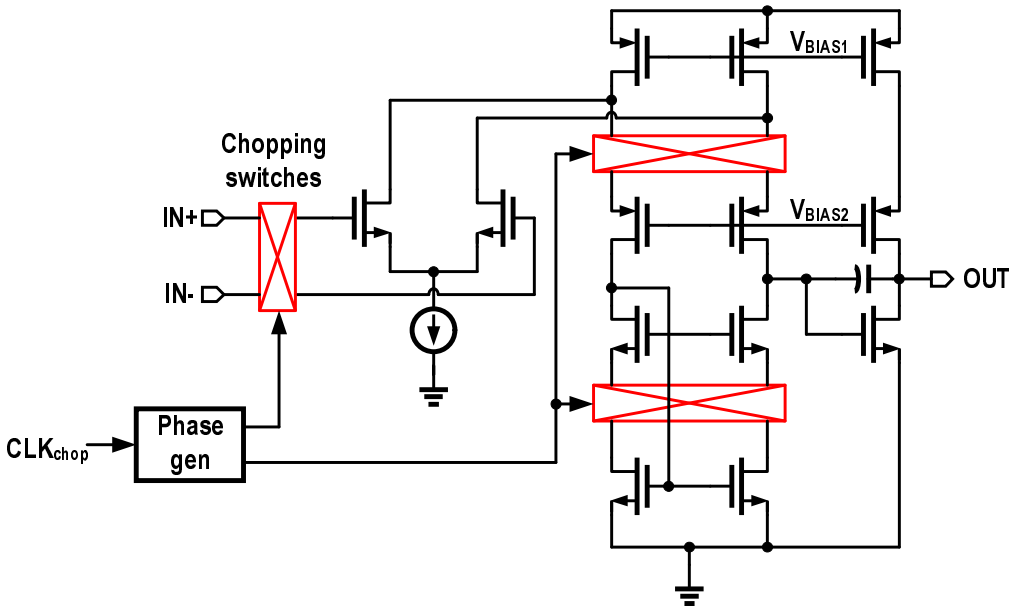

Figure 3.12: Error amplifier.

frequency, detecting a ΔD up-to 16 m requires the delay cell to produce at-least 16 ns of time-delay. In this work, the inverter-chain delay-cell produces a maximum delay of 26 ns, comfortably covering the required range of delays needed to detect the required ΔD range. The replica converter is composed of minimum sized 1.8 V devices followed by a low-pass filter with a 3 dB cut-off frequency at 160 KHz. To minimize its effect on loop stability, the filter cut-off frequency was selected to be low enough to minimize the output ripple, but above the unity-gain frequency of the sensor control loop.

3.4.3 VCO-based quantiser

The VCO-based quantiser [40] is composed of a voltage-controlled oscillator (VCO) and a digital 1-bit subtractor formed by two flip-flops and an EXOR gate. The sampling clock for the flip-flops can be the power converter PWM signal. The output of the VCO-based quantiser is a 1-bit measure of the number of the VCO output clock edges in one period of the sampling clock. Even though the integrator suppresses any VCO non-linearity, a supply-controlled VCO is used in order to reduce VCO control-voltage to output frequency non-linearity in the first place.

3.5 Measurement Results

A prototype duty-cycle sensor was fabricated in an 65 nm process tested with externally provided duty-cycle and voltage to mimic the signals coming from a real power-converter (see Fig. 3.13). Active area is 0.3 mm^2.

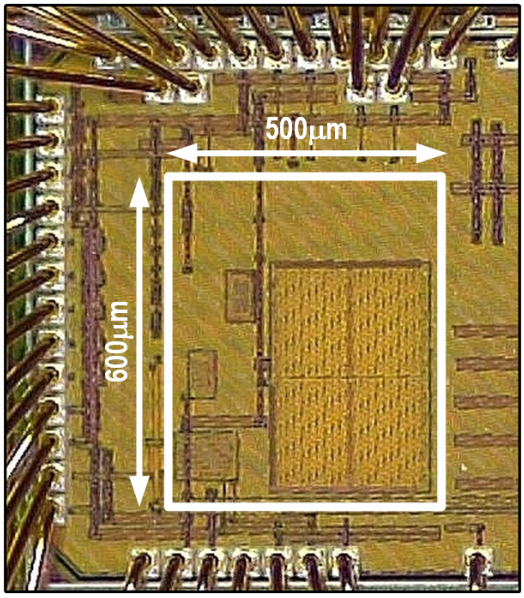

Figure 3.13: Die micrograph.

The output bit-stream was recorded in Tektronics Logic Analyser and passed through a digital low-pass filter and averaged in MATLAB to obtain the DC value. The PSD of the output bit-stream of the tested prototype is plotted in Fig. 3.14 for different duty-cycle inputs. There is high tonal behaviour at higher frequencies, as seen in the simulated PSD, but there is an increase in low-frequency noise floor which degrades the SQNR at high oversampling rates. Noise in DC voltage input emulating the buck converter output has a significant impact on the noise PSD of the output bit-stream. Because any noise in the DC voltage source is construed as noise in the duty-cycle by the sensor loop, this can be observed by the increased low-frequency noise floor in the output bit-stream PSD. Figure 3.15 plots the bit-stream average value vs the input duty-cycle and the residual error obtained from the difference between the measured bit-stream average and function obtained using linear regression fitting. A maximum error in linearity of 1% is observed.

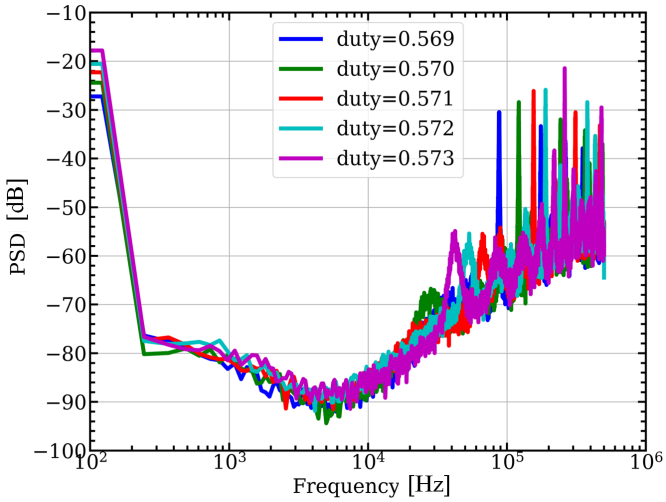

Figure 3.14: Prototype output bit-stream PSD.

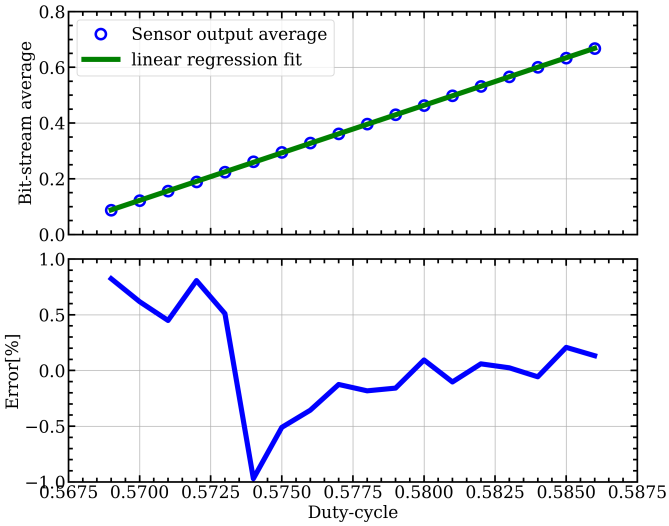

Figure 3.15: Sensor output with residual error plot after linear regression fit.

3.6 Conclusion

We presented a new duty-cycle sensing technique achieving 1% linearity over a duty-cycle change ranging from 3 m to 16 m, which makes it suitable for detecting small changes induced by load current in the duty-cycle of a buck converter. This technique does not require any extra resistive sense element in the power stage, nor does it require any matching between the power devices and the replica converter devices and has negligible power penalty. Combined with a power converter, this technique can achieve good DC current sensing performance.

CHAPTER 4

A 400 KHZ RC RELAXATION OSCILLATOR WITH 16 PPM/^{O} C INACCURACY AND 2.5 PPM/MV SUPPLY SENSITIVITY

4.1 Introduction

RC relaxation oscillators (RCOs) serve as efficient integrated clock sources in low power bio-medical and wearable applications and as real-time clocks to implement calendar functions. While they are area/power-efficient and well suited for integration in standard CMOS processes, their performance is degraded by temperature and supply variations. Specifically, the temperature dependence of the resistor and comparator offset/delay severely deteriorate their frequency stability. The problem of comparator offset/delay variation has been addressed extensively in prior art. For example, making the comparator delay much smaller than the entire period and chopping its input alleviates the comparator delay part of the frequency variation to a large extent [4]. But such techniques are difficult to implement when the required oscillation frequency increases beyond a few megahertz. At such frequencies, sampling the comparator delay and integrating it [41] or integrating the whole RC settling waveform to derive the period information [42], or generating a reference pulse free from comparator delays using a replica comparator [43] have proven useful. While the impact of comparator imperfections can be alleviated by circuit techniques, addressing the TC of the resistor is a lot more challenging. One way to address the resistor temperature variation issue is at the fabrication level. It has been shown recently that it is possible to make zero temperature coefficient resistors which provide decent references for RCOs [4], [44]. But these resistors have zero temperature dependence only to the first order and their comparatively large second order temperature dependence has a degrading effect on the temperature stability of the oscillator. Another more popular way to approach this problem is to use composite resistors made of a combination of resistors having different

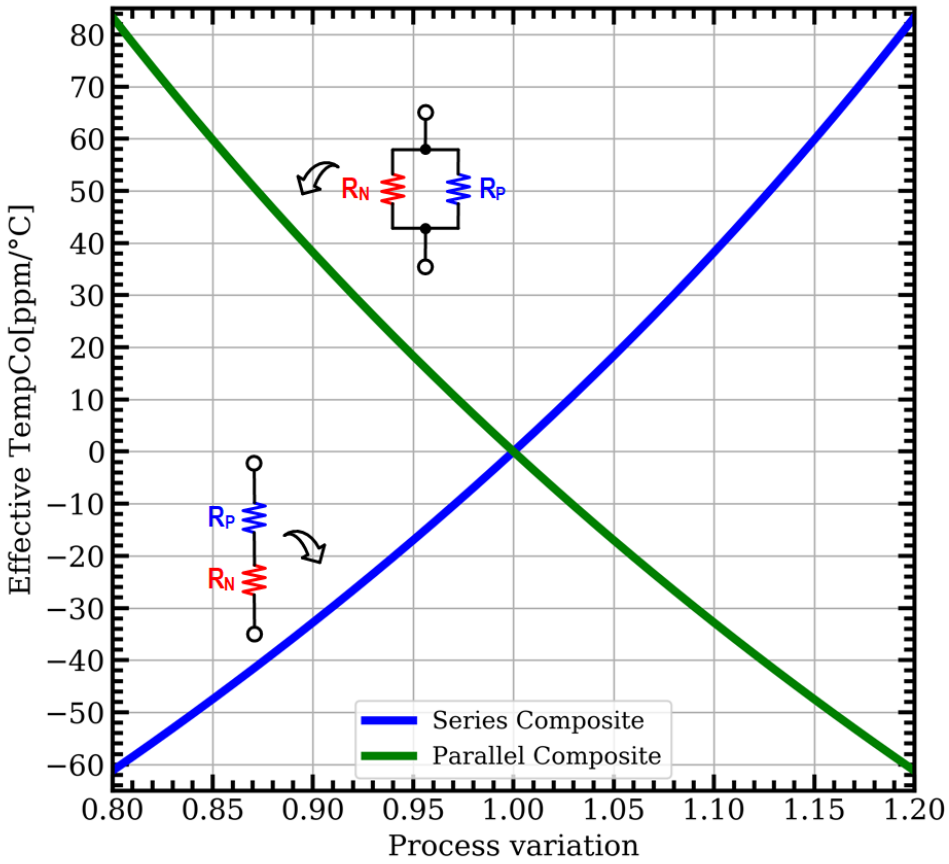

Figure 4.1: Temperature coefficient variation under process variation.

temperature coefficients. But these composite resistors have temperature coefficients which heavily depend on process variations [45].

For instance, consider two resistors with temperature coefficients 1500 ppm/^{o} C and -200 ppm/^{o} C. After combining these resistors in the required proportion so that the combination gives 0 ppm/^{o} C in series and parallel combination, the temperature coefficient variation under process variation is plotted in Fig. 4.1. Implementing the resistor by using combinations of resistors with opposing temperature coefficients (TCs) can lower the frequency inaccuracy to about 5000 ppm [46]. However, improving it further is challenging because it requires large trimming range. Secondary effects introduced by the trimming switches such as their on-resistance and leakage

further degrade the temperature characteristics of the resistor.

In view of these drawbacks, this paper describes a method for improving the frequency inaccuracy of RCOs by interpolating between resistors with opposing temperature coefficients. Fabricated in a 65 nm CMOS process, the prototype 400 kHz RC relaxation oscillator achieves an inaccuracy of $\pm$1000 ppm (16 ppm/^{o} C) across temperature range of -40^o C to 85^o C, 2.5 ppm/mV voltage sensitivity, and 5.7 ppm one second Allan deviation.

Rest of the paper is organized as follows. Section 4.2 and 4.3 introduces the proposed architecture and discusses the calibration procedure, section 4.4 deals with the circuit implementation details, section 4.5 shows measured results from the fabricated prototype and section 4.6 summarizes the findings.

4.2 Proposed Architecture

The key concept behind the proposed RCO is illustrated in Fig. 4.2. Consider the two RC relaxation oscillators, RCO_N, and RCO_P, that use different resistors, R_N and R_P, to implement the reference time constant, but are identical otherwise. Assuming the temperature coefficient of R_N (TC_N) and R_P (TC_P) have opposite signs, the frequency (F_N/F_P) of the output clocks (CK_N/CK_P) generated by RCO_N and RCO_P exhibit opposing dependencies on temperature. Therefore, we postulate that near-zero TC can be achieved by producing an output clock (CK_{OUT}) whose frequency, F_{OUT}, is a weighted sum of F_N and F_P. To this end, we propose to generate CK_{OUT} by selecting between CK_N and CK_P using a simple 2-to-1 multiplexer controlled by a select signal, SEL. The duty cycle, D, of the SEL signal is chosen such that the TC of CK_N is cancelled with that of CK_P at least to the first order, as shown in Eq. 4.1.

$$F_{OUT} = D * F_N + (1 - D) * F_P \tag{4.1}$$

While this approach provides a precise and straightforward way for canceling first-order TCs, it suffers from two critical drawbacks. First, switching between two asynchronous clocks (CK_N and CK_P) produces glitches that can degrade frequency accuracy significantly (see Fig. 4.2). Second, using two RCOs doubles the area and power, which is unacceptable in many applications. We address these two drawbacks by generating F_P and F_N using

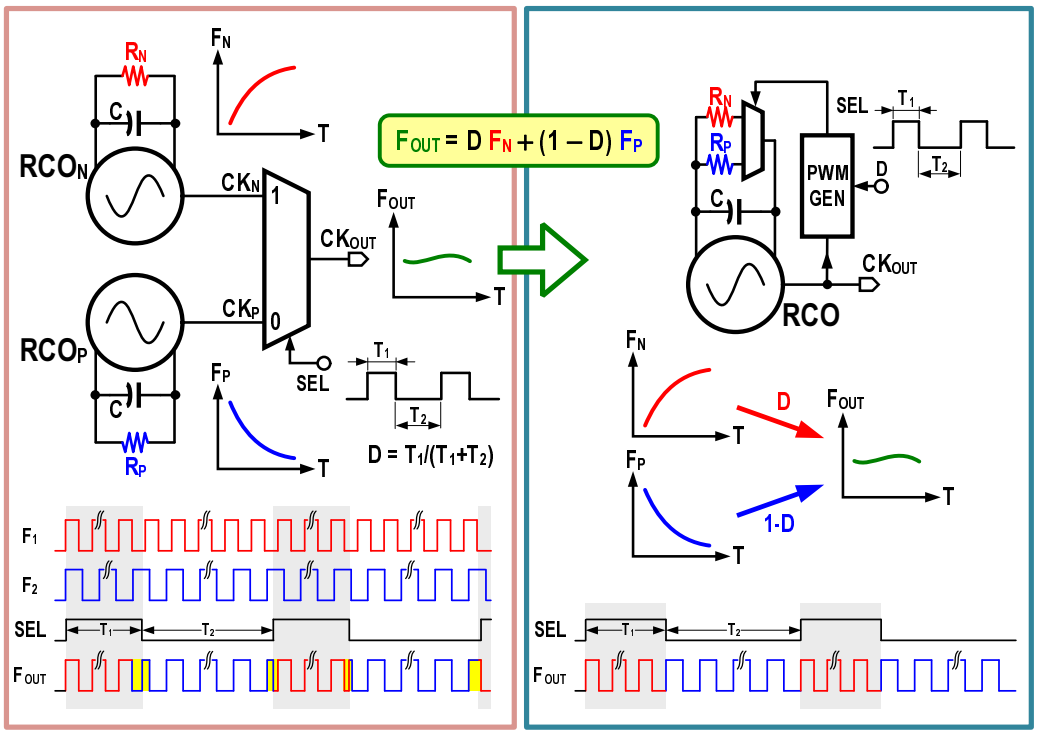

Figure 4.2: Illustration of the proposed RCO temperature compensation scheme.

a single RCO, wherein a multiplexer is used to choose between R_P and R_N as depicted in Fig. 4.2. Glitches in the output clock that may occur while switching between the resistors are avoided by synchronizing the multiplexer select signal with the output clock.

A detailed schematic of the RCO is shown in Fig. 4.3. The basic building blocks include bias circuit, comparator, chopping switches, digital PWM generator and passive components(R and C) to set the oscillator period. The bias circuit generates a current I which is then mirrored into M_1 and M_2. This current I then either flows in to capacitor C or one of the resistors R_N or R_P. During phase ϕ M_1 pumps current I into the resistor R_N or R_P depending on value of the SEL being 1 or 0 respectively and M_2 pumps current into capacitor C and vice-versa during phase $\overline{\phi}$. The ramp voltage generated across the capacitor C is then compared with the voltage across R_N or R_P for SEL bit being 1 or 0 respectively.

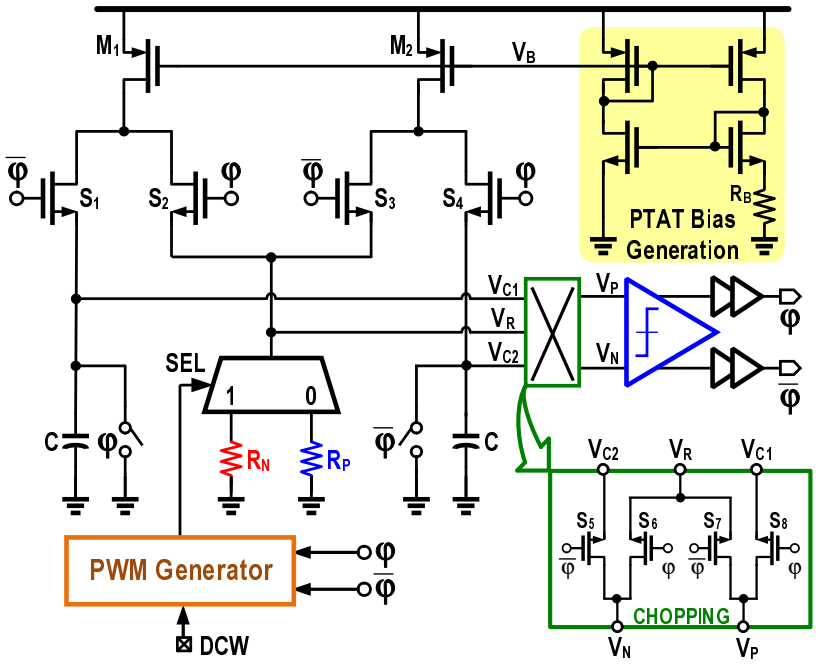

Figure 4.3: Proposed RCO architecture.

For simplicity, ignoring the impact of mismatch and offset, the period of the oscillator can be expressed as in Eq. 4.2.

$$T_{RCO} = t_{\phi} + t_{\overline{\phi}} \tag{4.2}$$

where both t_{ϕ} and $t_{\overline{\phi}}$ can be expressed as in Eq. 4.3

$$t_{\phi}(or\ t_{\overline{\phi}}) = \begin{cases} R_P(T)C + t_d(T), & \text{if SEL=0} \\ R_N(T)C + t_d(T), & \text{if SEL=1} \end{cases} \tag{4.3}$$

where $t_d(T)$ represents the comparator delay which is a function of absolute temperature T. Note that the current steering switch resistances have no impact on the oscillator period as the input to the comparator does not include the voltage drop across the switches S_{1-4}. The comparator is chopped to mitigate its offset and flicker noise by using the switch matrix [4]. The chopping switch resistances of switches S_{5-8} does not impact the period as there is no DC current flowing through them.

As can be seen from Eq. 4.2, the period of the oscillator is different for SEL bit being 0 or 1, but the temperature compensation happens over the average

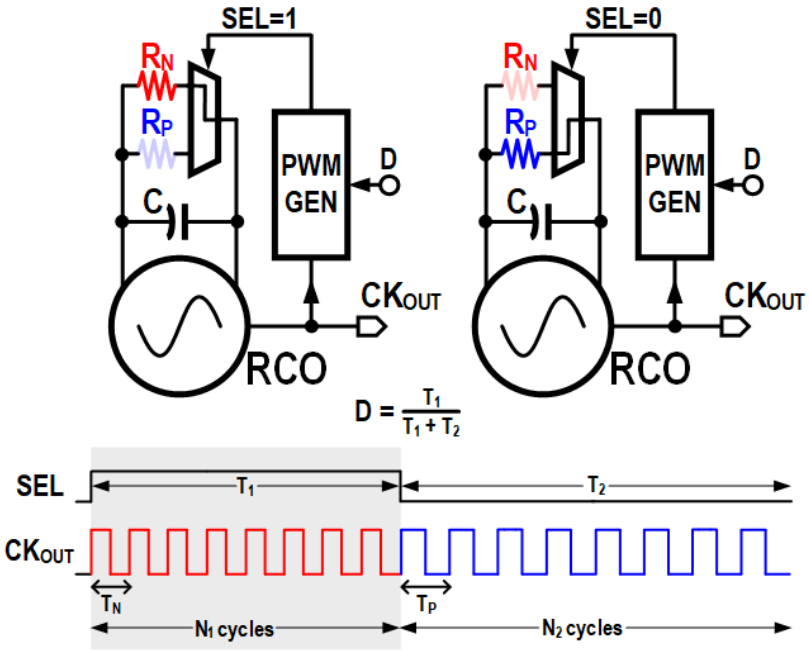

Figure 4.4: System operation of proposed architecture.

period of the oscillator. The steady-state operation is illustrated in Fig. 4.4. Assuming the period is T_P and T_N for $SEL = 0$ and $SEL = 1$ respectively and the duty cycle of the SEL signal is D, then the average period of the oscillator can be described as in Eq. 4.4. Glitches while changing the switching frequency are avoided by making the resistor transitions synchronous with the output clock and the duty cycle information is encoded digitally as a 15-bit digital codeword (DCW). A pulse-width modulator (PWM) converts the digital codeword (DCW) into a PWM output signal, SEL, used to choose between R_P and R_N.

$$T_{RCO,avg} = D * T_N + (1 - D) * T_P \tag{4.4}$$

D and subsequently DCW must be selected in such a way to cancel the first-order temperature coefficient of T_{RCO}. The choice of D and design considerations regarding it's implementations is presented in detail in section 4.3.

4.3 Calibration Procedure

The goal of the calibration procedure is to find the right DCW. The calibration is done by observing the output period as it is directly proportional to the RC time constant for the oscillator, as shown in Eq. 4.5.

$$T_{RCO} = 2 \times \begin{cases} R_P(T)C + t_d(T), & \text{if SEL=0} \\ R_N(T)C + t_d(T), & \text{if SEL=1} \end{cases} \tag{4.5}$$

where, t_d refers to the combined delay of the comparator and the digital circuitry following it and is a function of temperature T. The first step is to find the periods at 2 different temperatures T_1 and T_2 for both resistors R_P and R_N by setting $SEL = 0$ and 1 respectively. Let the measured periods be called $T_P(T_1)$, $T_P(T_2)$, $T_N(T_1)$ and $T_N(T_2)$. Then the first order slope of the period for SEL bit set to 0 and 1 is given by Eq. 4.6.

$$\begin{aligned} \alpha_P &= \frac{T_P(T_2) - T_P(T_1)}{T_2 - T_1} \\ \alpha_N &= \frac{T_N(T_2) - T_N(T_1)}{T_2 - T_1} \end{aligned} \tag{4.6}$$

Now, the required duty cycle D_{req} can be calculated from Eq. 4.7.

$$D_{req} = \frac{\alpha_P}{\alpha_P - \alpha_N} \tag{4.7}$$

It should be noted that there is tight accuracy requirement on D. The inaccuracy in D will result in an inaccuracy in the interpolation between the 2 periods T_P and T_N. The impact of inaccuracy in D can be explained using an example. Let's assume α_N and α_P to be -300 ppm/^{o} C and 150 ppm/^{o} C respectively. The D_{req} calculated from Eq. 4.7 is 1/3. Let D be encoded using an N-bit binary codeword DCW. Then the quantization error in DCW, ϵ can take a maximum value of 2^{-N}. Then DCW can be expressed as in Eq. 4.8.

$$DCW = D_{req} + \epsilon \tag{4.8}$$

Replacing D with DCW in Eq. 4.4 and expressing T_N and T_P as in Eq. 4.9, it can be shown that there will be a residual first order temperature

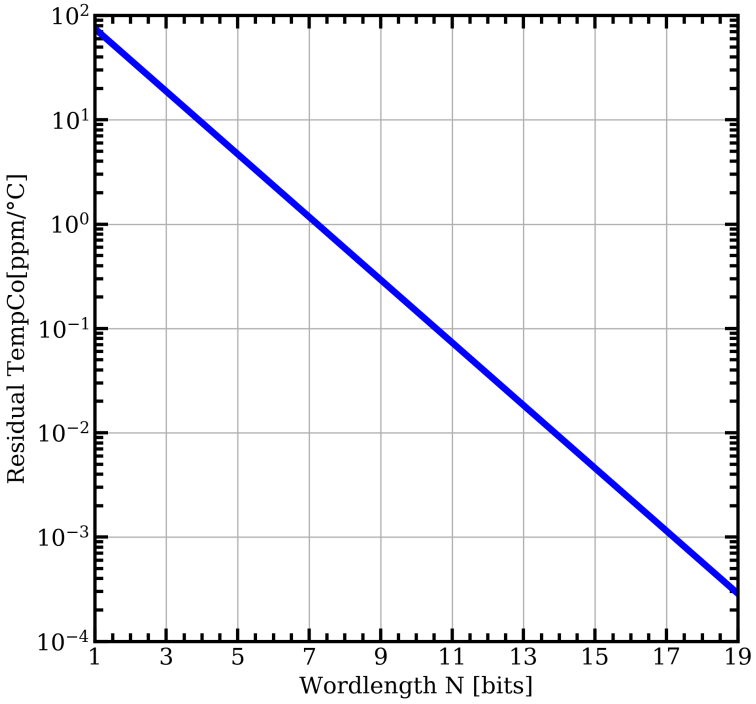

Figure 4.5: Residual first order slope error as the word-length of DCW is increased for $\alpha_N = -300$ ppm/^oC and $\alpha_P = 150$ ppm/^oC.

co-efficient of the average period which depends on ϵ as shown in Eq. 4.10.

$$\begin{aligned} T_N &= T_{N0}(1 + \alpha_N \Delta T) \\ T_P &= T_{P0}(1 + \alpha_P \Delta T) \end{aligned} \tag{4.9}$$

where T_{P0} and T_{N0} are oscillation periods for $SEL = 0$ and $SEL = 1$ respectively at room temperature.

$$\begin{aligned} T_{RCO,avg} &= DCW * T_N + (1 - DCW) * T_P \\ &= T_{RCO,avg,0} + \epsilon * (\alpha_N - \alpha_P)\Delta T \end{aligned} \tag{4.10}$$

where $T_{RCO,avg,0}$ average oscillation period at room temperature and can be expresses as $DCW * T_{N0} + (1 - DCW) * T_{P0}$. This error term in interpolation is calculated for different N and plotted in Fig. 4.5. The choice of N should be such that the residual error in slope interpolation be much lower than the higher order temperature co-efficients of the oscillator period.

Once N has been chosen to meet the requirements specified thus far, some consideration must be given as to how to implement this DCW. The implementation must maintain the resolution of DCW and also make the transitions between R_P and R_N completely synchronous with the output clock so as to not introduce any non-linearity in the interpolation of the two different periods. In order to do this, D is implemented by counting the cycles of the RCO output clock as shown in Fig. 4.4. Consider that $SEL = 1$ for N_1 cycles and $SEL = 0$ for N_2 cycles. Then the average period $T_{RCO,avg}$ over $N_1 + N_2$ cycles is given by Eq. 4.11.

$$(N_1 + N_2)T_{RCO,avg} = N_1 * T_N + N_2 * T_P \tag{4.11}$$

where, T_P and T_N are the RCO output periods with $SEL = 0$ and 1 respectively. From Eq. 4.11, the D can be calculated as:

$$D = \frac{N_1}{N_1 + N_2} \tag{4.12}$$

From Eq. 4.12 it can be seen that the inaccuracy of D can be made arbitrarily small by choosing arbitrarily large values of $N_1 + N_2$. For this work, $N_1 + N_2$ was set to be $2^{15} - 1$, and the residual error in interpolation is about 0.02 ppm/^{o} C. This is much less than the expected error in period over a temperature range of -40^o C to 85^o C. Thus, the DCW can now be calculated by the relation in Eq. 4.13.

$$DCW = N_1 = round((N_1 + N_2) * D_{req}) \tag{4.13}$$

Note that the instantaneous period will be very different from the average period, but over $N_1 + N_2$ cycles, the average period will be an accurate linear combination of the periods due to R_P and R_N, without the use of complicated switch matrices.

4.4 Circuit Implementation

4.4.1 Comparator

The schematic of the comparator is shown in Fig. 4.6. It is implemented using two gain stages composed of a resistively loaded PMOS input fully-differential amplifier followed by a differential-to-single ended (D2S) stage. The D2S is implemented using a current-mirror loaded OTA and provides rail-to-rail output signals. Thanks to the fully-balanced first stage, noise contribution from the tail current source transistor, M_{B1}, is much suppressed and the comparator supply noise immunity is significantly improved. Simulated phase noise spectral density at 1 Hz off-set was observed to be 8.73 dBc/Hz. In order to convert this number to the time-domain Allan variance, we can use Eq. 4.14 [47].

$$\langle \sigma_y^2(N,T,\tau) \rangle = \frac{N}{N-1} \int_0^{f_h} S_y(f) \frac{sin^2(\pi f \tau)}{(\pi f \tau)^2} \Big\{ 1 - \frac{sin^2(\pi r f N \tau)}{N^2 sin^2(\pi r f \tau)} \Big\} df \quad (4.14)$$

where, N is the number of data points used to calculate the variance, T is time interval between the beginnings of two consecutive measurements of average frequency, τ is the duration of averaging period of the output clock waveform and $r = T/\tau$. For the 2-point Allan variance that is generally reported as a measure of frequency stability, $N = 2$, $T = \tau$, hence $r = 1$. Replacing these values in Eq. 4.14, we get Eq. 4.15.

$$\sigma_y^2(\tau) = 2 \int_0^{f_h} S_y(f) \frac{sin^4(\pi f \tau)}{(\pi f \tau)^2} df \quad (4.15)$$

where, for both Eq. 4.14 and 4.15, $S_y(f) = (f/f_0)^2 S_\phi(f)$ and f_0 is the nominal frequency of the oscillator. The time-domain Allan variance was calculated to be 7 ppm which is 3× lower compared to the conventional case of using a D2S as comparator [4].

To avoid glitches at the comparator output, hysteresis is added by introducing a small output-dependent mismatch between the load resistors in the first stage. This is achieved using switches S_1 and S_2 that short a tiny portion of the load resistors to ground (see Fig. 4.6). When $V_P < V_N$, $\phi = 0$, hence

switch S_2 is "OFF" and switch S_1 is "ON". This creates a slight imbalance between the resistor loads of the two branches of the first stage. Similarly, when $V_P > V_N$, the imbalance is in the opposite direction, which results in some hysteresis. The amount of hysteresis is proportional to the small resistance(50 kΩ) added in series with the main load resistor(1 MΩ) and was set to be about 7 mV. Since each stage is current biased, the supply sensitivity of the delay of the comparator is very low. The comparator is biased by PTAT current source and consumes 3 μA at room temperature. The PTAT biasing reduces the comparator delay variation to within 1% of the total period.

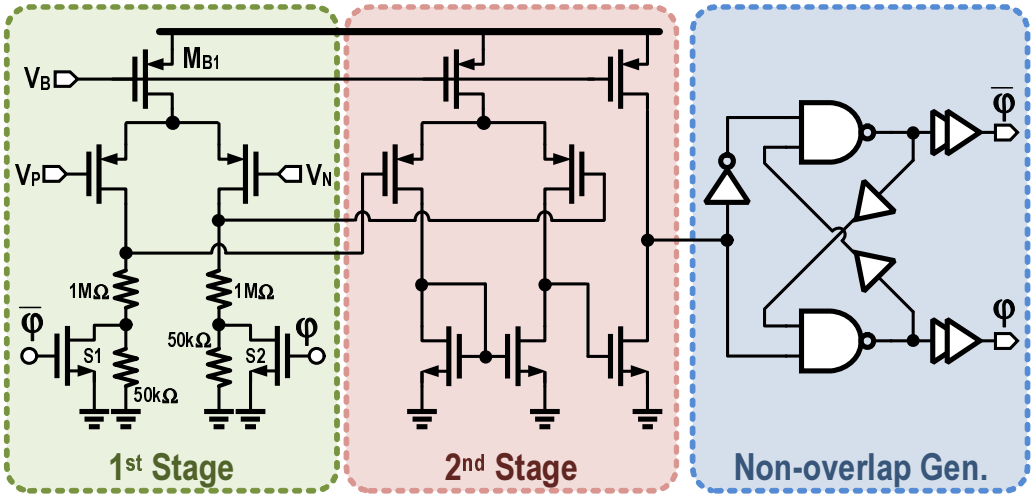

Figure 4.6: Comparator schematic.

4.4.2 Resistor and capacitor selection

Resistor selection is done based on a two primary characteristics. First, R_P and R_N should have opposing first order temperature coefficients and preferably lower higher order dependencies on temperature. Secondly, they should occupy small area. In order to reduce power consumption, the current through each resistor branch is 200 nA. The nominal value of the resistors is chosen to 1 MΩ. Therefore, the input common mode to the comparator is 200 mV. The multiplexing between the resistors is done through through switches in series with R_P/R_N. The switches are large enough to make their "on" resistance small compared to the 1 MΩ resistors. R_P is implemented as a composite resistor of silicided P+ poly resistor and un-silicided P+ poly

resistor. The silicided resistor was used to reduce the second order component of the unsilicided poly-resistor. R_N is implemented using unsilicided N+ polyresistor. Post layout simulations indicate the residual second order dependency left after first order compensation is about 2000 ppm across a temperature range of -35^o C to 85^o C.

MIM capacitors have much lower temperature dependence compared to the resistors. Capacitor C (see Fig. 4.3) is chosen to be 1 pF MIM capacitor. In this implementation, this capacitor has not been trimmed. Note that one of the drawbacks of this architecture is the average frequency of oscillation is not fixed. Due to process variation, the nominal values of the resistors and capacitors may change, which may change the nominal frequency of the oscillator at room temperature from part to part. Some of this variation may be countered by trimming the capacitor C.

4.4.3 Bias generation

PTAT bias generation using a constant-Gm biasing scheme as shown in Fig. 4.7 has been adopted for this work. Note that this current has no role in setting the RC time constant of the oscillator. The purpose of this PTAT bias current is to mitigate some of the delay increment in the comparator with increasing temperature. The biasing resistor is implemented using a composite resistor consisting of P+ and N+ poly resistors so that the resistor has zero temperature coefficient at-least to the first order.

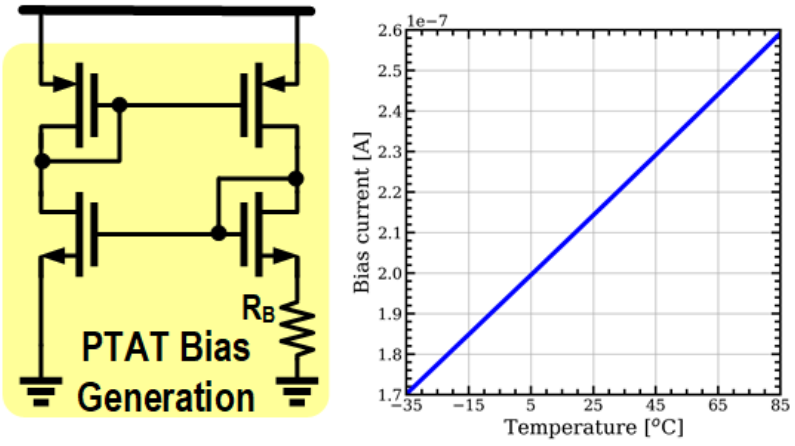

Figure 4.7: Constant-G_m biasing.

4.4.4 Counter

The SEL signal with the desired duty cycle is generated using a counter-based digital pulse-width modulator circuit shown in Fig. 4.8. It consists of a 15-bit counter and digital comparator. The counter produces a saw-tooth waveform that takes values from 0 to $2^{15} - 1$. The comparator sets SEL = 1 when the counter output is larger than the 15-bit input digital control word and SEL = 0 when it is smaller. As a result, the duty cycle of the SEL signal can be controlled with a resolution of about 0.02 ppm/^{o} C as was discussed in Section 4.3.

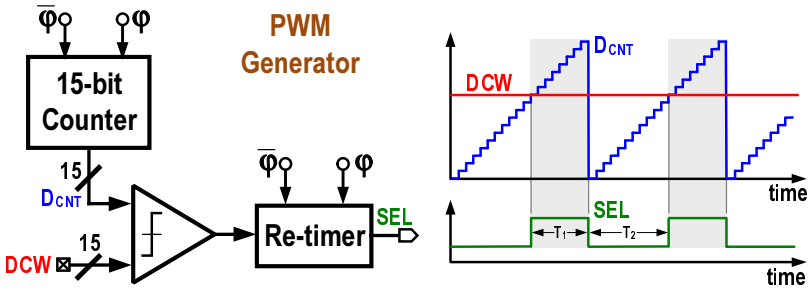

Figure 4.8: Counter schematic.

4.5 Measurement Results

A prototype of the proposed RCO was fabricated in a 65 nm CMOS process. The oscillator operates from a 1.6 V supply and consumes 7.2 μW of which 11% is consumed by the PWM generator. Eight RCO samples, each of which is packaged in a QFN package, are characterized across a temperature range of -40^o C to 85^o C. To illustrate the proposed TC cancellation scheme, F_P and F_N are measured by forcing SEL = 1 and SEL = 0, respectively, for 1 sample and plotted in Fig. 4.9.

TC_P and TC_N calculated from these plots are about +118.3 ppm/^{o} C and -475.9 ppm/^{o} C, respectively. The optimum duty cycle, D_{OPT}, needed to compensate TC_P/TC_N, was calculated off-chip using measured F_P/F_N at only two temperatures (40^o C and 85^o C) and written into an on-chip 15-bit DCW register. The measured F_{OUT} using $D_{OPT} = 0.2173$ shown at the bottom of Fig. 4.9 closely matches the calculated, $F_{OUT} = D_{OPT}F_N +$

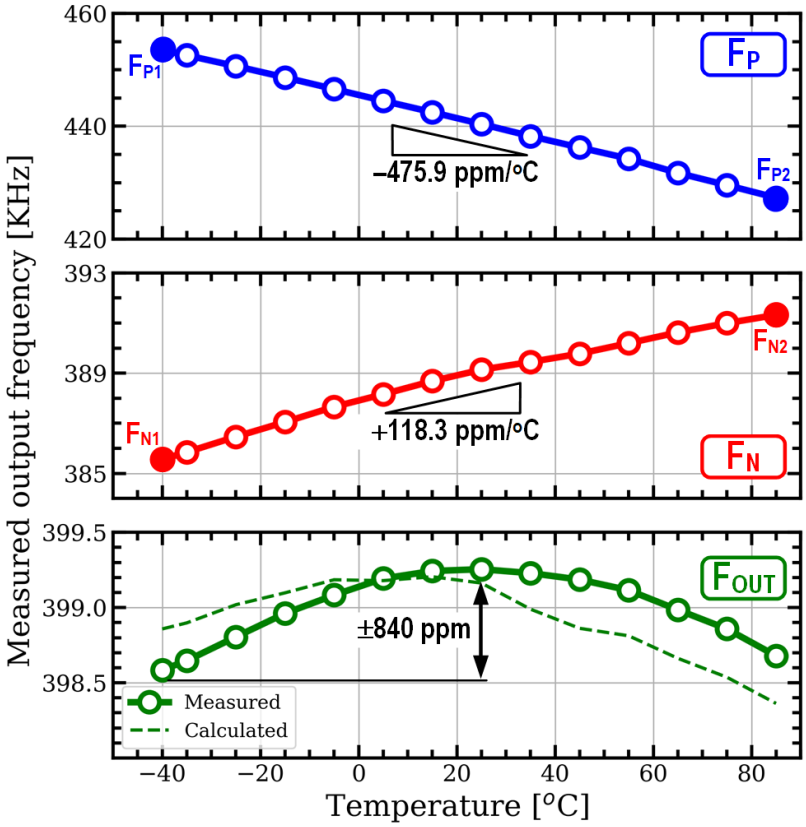

Figure 4.9: Measured F_N and F_P across temperature and measured/calculated F_{OUT} using optimal duty cycle.

$(1 - D)F_P$, which verifies that the proposed TC compensation scheme can precisely cancel the first-order TC of the RCO.

The measured frequency error plots (see Fig. 4.10) for eight samples indicate frequency inaccuracy is less than ±1000 ppm or equivalently 16 ppm/^{o} C. The measured frequency error across a supply voltage range of 1.6 V to 2 V shows that the worst-case supply sensitivity is only 2.5 ppm/mV (Fig. 4.11). The measured Allan deviation in 1-second strides is 5.7 ppm (see Fig. 4.12), which is 3x better than [4], thanks to the proposed comparator. The performance of the RCO is summarized and compared to the state-of-the-art relaxation oscillators in 4.1. The proposed RCO achieves the best reported temperature stability but with more than 7.5x better power efficiency compared to [48]. Die micrograph is shown in Fig. 4.13 and active area is 0.027 mm^2.

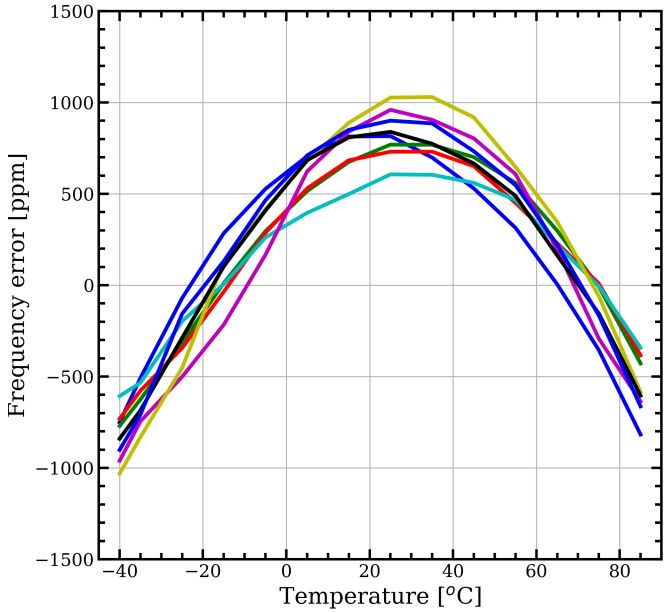

Figure 4.10: Measured frequency error versus temperature for eight samples.

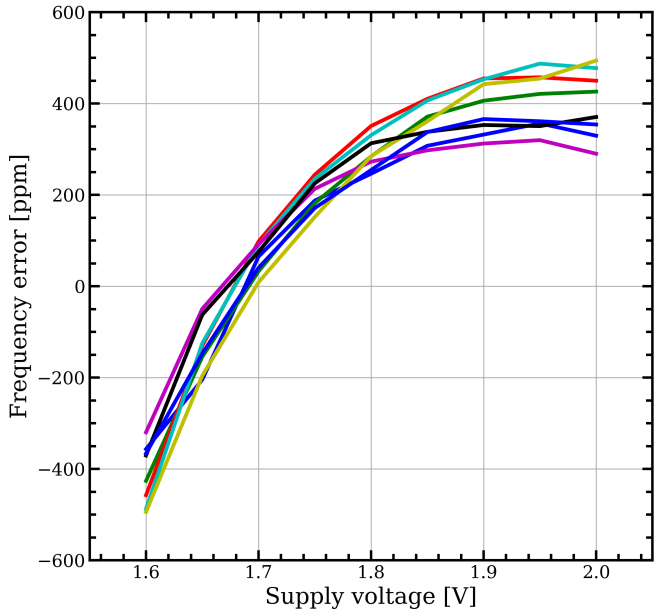

Figure 4.11: Measured frequency error versus supply for eight samples.

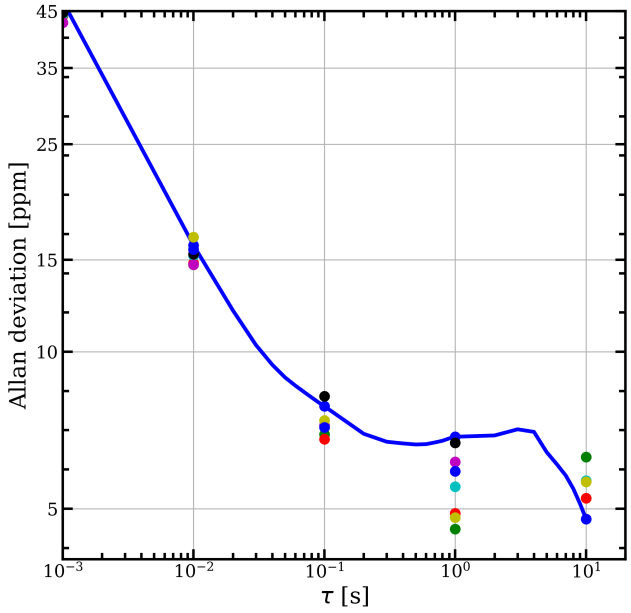

Figure 4.12: Measured Allan deviation versus duration of strides for eight samples.

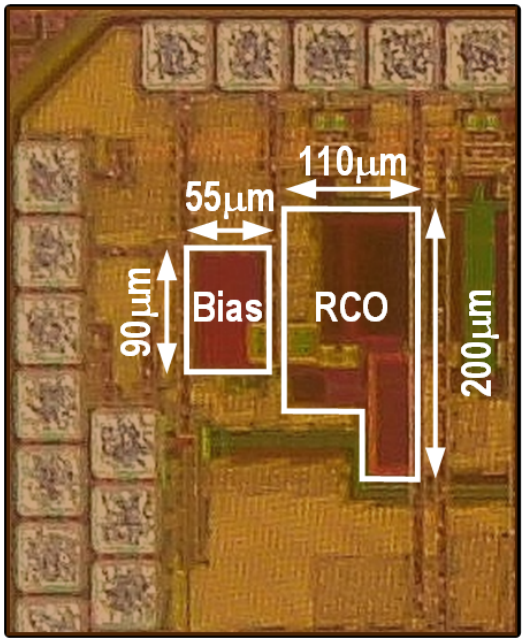

Figure 4.13: Die micrograph.

Table 4.1: Performance comparison of proposed temperature compensated oscillator with state-of-the-art designs.

	This work	[4]	[44]	[49]	[50]	[48]
Process [nm]	65	65	65	180	65	60
Frequency [kHz]	400	18.5	33	0.011	1350	32.768
Power [μW]	7.2	0.13	0.19	0.0058	0.92	4.48
Area [mm^2]	0.027	0.032	0.015	0.24	0.005	0.048
TC [ppm/^{o} C]	16	27.7	38.2	45	96	16.67
Temperature range [^{o} C]	-45 to 85	-40 to 90	-20 to 90	-10 to 90	0 to 150	-20 to 100
Supply sensitivity [ppm/mV]	2.5	50	0.9	10	9.8	1.25
Voltage range [V]	1.6 to 2	-	1.15 to 1.45	1.2 to 2.2	0.9 to 1.9	1.6 to 3.2
Number of samples	8	4	5	1	2	4
Allan deviation @ τ=1 s [ppm]	5.67	18	4	70	-	-

4.6 Conclusion

A temperature-compensated relaxation oscillator architecture that achieves excellent frequency stability with a low active area is presented. Frequency stability across a wide range of temperature is improved by precisely interpolating between resistors with opposing temperature coefficients. By obviating the need for a large trimming network of switches and resistors, it achieves excellent frequency accuracy across PVT. Fabricated in 65 nm CMOS process, the prototype 400 kHz oscillator achieves an inaccuracy of 16 ppm/^{o} C (-40^o C to 85^o C), 2.5 ppm/mV voltage sensitivity, and 5.6 ppm Allan deviation in one-second strides.

CHAPTER 5

CONCLUSION

High efficiency DC-DC power conversion is essential for high-performance battery-operated portable electronic systems. In the first part of this work, a novel architecture for a boost converter used in LED driver is presented. The architectural evolution and the implementation details are explored. By cascading a low-switching frequency time-interleaved series-parallel SC-stage with an inductive boost converter, we demonstrated that switching losses can be greatly reduced. Charge-sharing losses of the SC stage are minimized by soft-charging flying capacitors with the inductor of the boost stage. Fabricated in 180 nm BCD process, the prototype converter generates 30 V output voltage from a Li-ion battery source and can provide a load current in the range of 0 to 100 mA with an excellent peak power efficiency of 91.15% at 30 mA. Compared to state-of-the-art designs, the proposed converter achieves a 3% improvement in peak power efficiency.

But further improvement in this work is possible by incorporating current mode control to improve the existing transient response time from a few milli-seconds to a few micro-seconds. One possible way to implement current mode control is to use the conventional current sensing schemes to sense the low-side switch current of the boost stage as shown in Fig. 5.1. Both sense-FET based and filter-based current sensing can serve as a solution for sensing the inductor current.

In the second part of this work, a duty-cycle sensor was presented as a possible alternative to existing current-sensing schemes for system level power optimisation in microprocessor-based applications. The new duty-cycle sensing technique achievs 1% linearity over a duty-cycle change ranging from 3 m to 16 m, which makes it suitable for detecting small changes induced by load current in the duty-cycle of a buck converter. This technique does not require any extra resistive sense element in the power stage, nor does it require any matching between the power devices and the replica converter

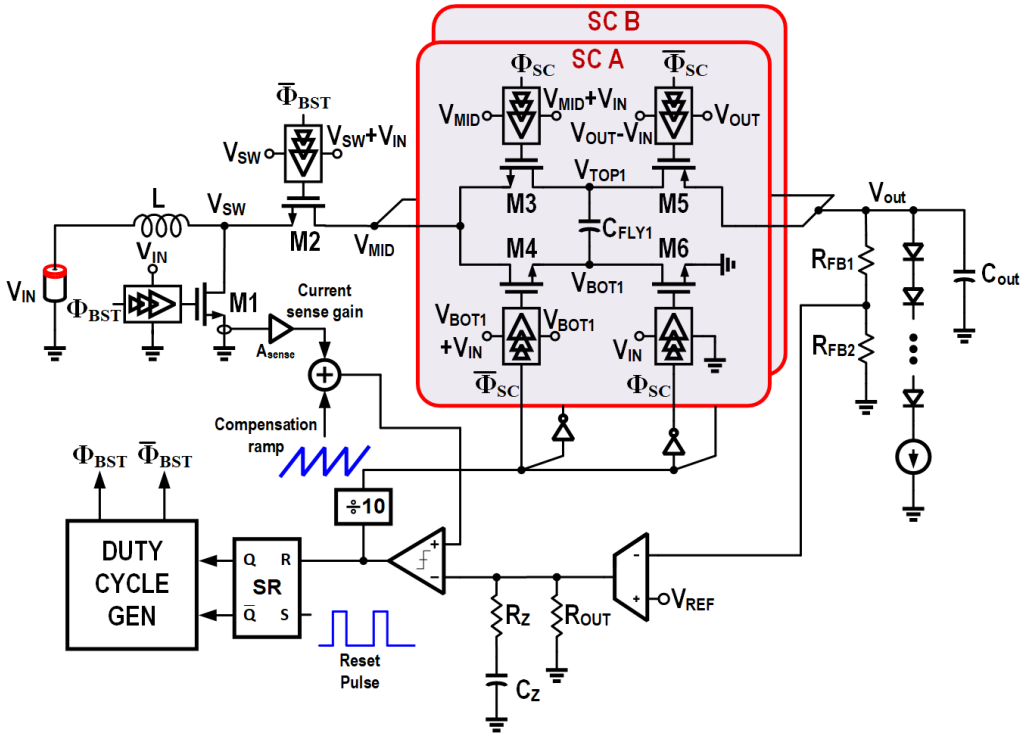

Figure 5.1: Current-mode control implementation of the proposed converter.

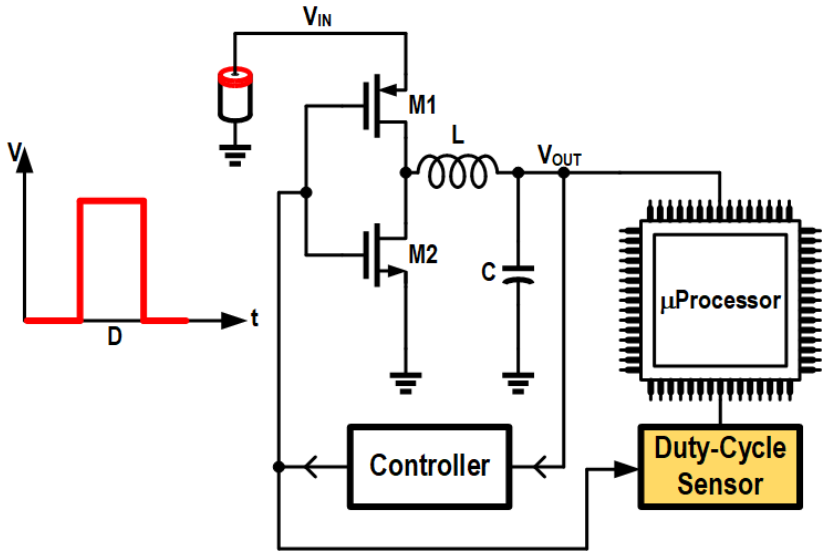

Figure 5.2: Duty-cycle sensor with buck converter as a complete current sensing solution.

devices and has negligible power penalty. As a future work, this technique needs to be successfully deployed in a high-power buck converter system, as

shown in Fig. 5.2, where the sensor needs to be immune to high levels of substrate noise from a working buck-converter.

In the third part, a temperature-compensated relaxation oscillator architecture that achieves excellent frequency stability with a low active area is presented. Frequency stability across a wide range of temperature is improved by precisely interpolating between resistors with opposing temperature coefficients. By obviating the need for a large trimming network of switches and resistors, it achieves excellent frequency accuracy across PVT. Fabricated in 65 nm CMOS process, the prototype 400 kHz oscillator achieves an inaccuracy of 16 ppm/^{o} C (-40^o C to 85^o C), 2.5 ppm/mV voltage sensitivity, and 5.6 ppm Allan deviation in one second strides. One of the drawbacks of this architecture is that the instantaneous frequency toggles between two nearby values. One possible way to have a fixed output frequency is to have a frequency-locked loop (FLL) whose reference time period is derived from the proposed high-accuracy interpolation between the resistors of opposing temperature coefficients. This way the output clock-period can be controlled as an integer sub-multiple of the reference period while preventing the interpolation effects from appearing at the output.

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