© 2021 Phuc Thanh Huynh

AN INTEGRATED GENERATOR-RECTIFIER SYSTEM FOR HIGH-POWER AC-DC CONVERSION

BY

PHUC THANH HUYNH

DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois Urbana-Champaign, 2021

Urbana, Illinois

Doctoral Committee:

Assistant Professor Arijit Banerjee, Chair
Professor Kiruba Sivasubramaniam Haran
Professor Philip T Krein
Assistant Professor Subhonmesh Bose

ABSTRACT

High power ac-dc conversion plays an increasingly important role in energy conversion systems, such as wind turbines or electric ship's grids. Conventional conversion architectures rely heavily on active rectifiers, which consist of fully-controlled power-electronics switches. These make the system bulky, lossy, and less reliable. This dissertation presents an alternative approach: integrating a multi-port permanent magnet synchronous generator (PMSG) with series-stacked power converters to create an integrated generator-rectifier system. An active rectifier processes only a fraction of the total converted power while regulating the dc bus. Diode bridges process the remaining power, allowing substantial increases in overall power density, efficiency, and reliability.

Filter capacitors are commonly connected to output of passive rectifiers to reduce the dc-bus voltage ripple. These filters are the main contributor to the overall system size, weight, cost, and failure, as well as to the low power factor at the ac ports powering the passive rectifiers. These capacitors can be eliminated by implementing appropriate phase shift between different ac ports. Alternatively, the filtering function can be integrated to the active rectifier through active control. A voltage opposite the passive-rectifier ripple component is synthesized at the active-rectifier dc-side by modulating the ac-side current. Compensation occurs due to the series connection of the rectifier dc outputs.

Deployment of the integrated generator-rectifier systems in wind-energy applications requires maximum power point tracking (MPPT) capability, which seems to be challenging due to the presence of numerous uncontrolled passive rectifiers. Due to the series connection and a constant dc-bus voltage, dc-side current of the active rectifier sets the output power of the passive rectifiers, and consequently the total generator output power. The dc-side current is dependent on the d-axis current, which can be commanded to follow a reference value. This reasoning lays foundation for MPPT using the integrated generator-rectifier system. Alternatively, the d-axis current can be used

to regulate the dc-bus voltage, opening up opportunities in dc grid-forming applications.

Elimination of capacitors at the diode rectifiers' output by appropriately phase-shifting the voltages of a multi-port generator further improves overall architecture's reliability. A generalized framework is developed to evaluate the interactions among the different generator ports, diode-bridge rectifiers, and the active rectifier used to control the power flow. This framework allows quantifying the effect of integration on the dc bus power ripple and power imbalance among different generator ports. An exemplary winding layout is proposed that ensures theoretically zero interaction between the passive ports though all the ports are mounted on a magnetic structure. Furthermore, the framework provides the guideline for generator designs to ensure successful integration with the rectifier system.

Finally, per-unit generator inductance is shown to be the handshake parameter between the generator and the rectifiers. The generator and power electronics designs are paired together to form feasible systems. Annual energy production calculation based on multiple wind profiles shows higher energy yield by the integrated system than the conventional solutions. This result proves the integrated generator-rectifier system's suitability for offshore wind energy harvesting.

To my family, for their unconditional love.

ACKNOWLEDGMENTS

I would like to thank Professor Arijit Banerjee for guiding me through the research and publication process. The research would not be possible without a supportive environment created by the University of Illinois Power and Energy Area. I would like to acknowledge the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, and the Grainger Center for Electric Machinery and Electromechanics for funding this project. Last but not least, I would like to thank graduate fellows and undergraduate students who have involved in different stages of my research.

CONTENTS

LIST OF ABBREVIATIONS

AEP	Annual Energy Production
LCOE	Levelized Cost of Electricity
PMSG	Permanent Magnet Synchronous Generator
VA	Volt Ampere
RLE	Resistor (R), inductor (L), and back emf (E)
E_0	Total generator rated per-phase line-to-neutral back emf
E	Each ac port per-phase line-to-neutral back emf
f_{sw}	Switching frequency
I_{ac}	Peak ac-side current of the active rectifier
I_{base}	Base current
I_{dc}	Dc-bus current
I_{sd}	Active-rectifier d-axis current
I_{sq}	Active-rectifier q-axis current
J	Moment of inertia
k	Number of ac ports
κ	Ratio between power outputs of an ac port power the passive and an ac port powering the active rectifier
K_i	Integral gain
K_p	Proportional gain
k_{opt}	Optimal number of ac ports
L	Total PMSG per-phase synchronous inductance

L_{ll}^{c}	Lead-lag controller transfer function
L_{pr}^{c}	Proportional-resonant controller transfer function
m	Total number of passive rectifiers
N_{series}	Number of serial group of IGBTs in a switch
$N_{parallel}$	Number of parallel IGBTs in each IGBT group
n	Total number of active rectifiers
P_a	Active-rectifier dc-side power
P_{ac}	Active-rectifier ac-side power
P_{base}	Base power
P_{dc}	Dc-bus power
$P_{loss}^{passive}$	Losses is on passive rectifier
P_{igbt}^{cond}	Conduction loss of an IGBT
P_{igbt}^{on}	Turn-on loss of an IGBT
P_{igbt}^{off}	Turn-off loss of an IGBT
P_{diode}^{cond}	Conduction loss of a free-wheel diode
P_{diode}^{rr}	Reverse-recovery loss of a free-wheel diode
P_{loss}	Total conversion losses of the power electronics converter
p_{loss}	Power electronics converter losses normalized by the base power
pu	(superscript) Per-unit
$,rated$	(subscript) Rated value
R	Total PMSG per-phase resistance
τ	Current controller time constant
V_a	Total dc-side voltage of n active rectifiers
V_{a0}	Active-rectifier average dc-side voltage
$V_{a,min}$	Minimum active-rectifier dc-side voltage
VA	Voltage-ampere rating

V_{active}	Dc-side voltage of an individual active rectifier
V_{base}	Base voltage
V_{dc}	Dc-bus voltage
V_p	Total dc-side voltage of m passive rectifiers
V_{p0}	Passive-rectifier average dc-side voltage
V_{pk}	Amplitude of k-th harmonic of the passive-rectifier voltage
$V_{passive}$	Dc-side voltage of an individual passive rectifier
V_{sd}	Active-rectifier d-axis voltage
V_{sq}	Active-rectifier q-axis voltage
ω	Generator speed normalized by the rated value (per-unit)
ω_0	Rated generator electrical frequency (line frequency)
ω_{min}	Minimum generator speed
ω_m	Mechanical speed
X_{pu}^L	Per-unit synchronous reactance
X_p	Passive-rectifier commutation reactance
Z_{base}	Base impedance

Chapter 1

INTRODUCTION

Ac-to-dc power conversion is essential in many emerging applications, including wind energy and electrified transportation. The dc interface allows prime movers to operate at variable speed, leading to maximum power point tracking in wind applications [1–4], or improved fuel efficiency in electric ships [5–7]. However, the ac-to-dc conversion at high power is a daunting task due to the limited voltage and current ratings of the available power electronics switch. This dissertation aims at solving this challenge from the conversion architecture approach. This chapter first reviews conventional high-power ac-to-dc conversion topologies and points out the inherent limitations. Research questions and philosophies to address the problem are discussed. Finally, the contributions are summarized.

1.1 Conventional approaches for megawatt-scale ac-to-dc power conversion

A typical megawatt-scale ac-to-dc conversion system includes two elements: a power electronics converter and a generator. Typically, the converter rectifies three-phase ac power into dc. The generator performs mechanical-to-electrical power conversion.

From a converter perspective, achieving power-flow control between the ac and the dc sides at megawatt power is a daunting proposition. The simplest solution is a six-pulse diode-bridge rectifier with a filter capacitor for smoothing the dc-side voltage ripple [8]. Although having simple construction, high conversion efficiency, and high reliability [9, 10], this converter cannot actively control the power flow. The control must be achieved indirectly through the generator.

Topologies based on actively controlled power electronics switches such as IGBTs solve the control problem but are challenged by limited switch rating and high conversion losses. A dc-dc

converter could be cascaded to a diode bridge to provide power flow control [10, 11]. The dc-dc converter must provide the full dc-bus voltage. Power factor correction is possible. However, it requires additional input filters made of inductors and capacitors. These filters are designed at a specific line frequency. Variable-generator-speed operation is not attainable.

Variable-speed operation and power factor control could be achieved with a three-phase pulse-width-modulation-based (PWM-based) active rectifier. Two-level is the most common topology due to simple control [12–15]. Each switch in the rectifier must be rated for the dc-side voltage and the peak ac-side current. Series/parallel-connecting multiple switches achieve higher ratings but require additional hardware and special layout to ensure equal voltage/current sharing [1]. Additional switches and hardware adversely affect the overall reliability [9]. At medium dc voltage, a two-level converter could cause excessive electromagnetic interference (EMI) because the switching node voltages alternate between zero and the dc-bus voltage at the switching frequency.

Multi-level rectifiers achieve the same functionality as the two-level topology with reduced EMI because the switching node operates at a fraction of the dc-bus voltage. Neutral-point clamped appears to be the most popular for high-power applications [16–19]. Achievements of balanced capacitor voltages and even conversion-losses distribution are major challenges. The multi-level flying capacitor is an attractive alternative due to redundant switching states for controlling capacitor voltage balancing and even loss distribution [20–22]. However, a large number of capacitors, precharging circuits, and a complex control scheme are required. The modular multi-level converter is compelling for high-power applications due to high conversion efficiency, scalability, and absence of the dc-link capacitor [23, 24]. Nevertheless, voltage balancing is required to ensure equal voltages across floating dc capacitors in the submodules [25].

For megawatt-scale power applications, in which a single converter cannot meet the power demand, generator design relieves the power converter requirement. For example, doubly-fed induction generators (DFIGs) reduce the power electronics converter rating to a fraction of the system-rated power in wind-power generation [3]. Multi-port and multi-phase permanent magnet synchronous generator (PMSG) designs have been considered to reduce the individual converter size and provide redundancy for improved system reliability [6, 26–29]. The same converter type is considered for all the generator ac ports, even though each converter has a reduced size.

1.2 Research objective

The research objective is to create an ac-to-dc conversion system at a megawatt power level that is more efficient, compact, and reliable than conventional solutions. The output of the system is dc power with an acceptable ripple component. The converter itself must be able to control power flow between the ac and dc sides. This capability enables maximum power point tracking (MPPT) in wind energy and dc-bus voltage regulation in grid-forming applications.

1.3 Philosophy

From power electronics switch selection perspective, line-frequency diodes are the best candidates to achieve high conversion efficiency, high power capability, and compactness. Figure 1.1 compares the conversion losses of three devices: a line-frequency diode, an IGBT, and an IGBT-parallel free-wheeling diode, operating at 3.6 kV–1000 A [30, 31]. The IGBT, together with the free-wheeling diode switches at 2 kHz, typical for a megawatt-scale application. A line-frequency diode has 10x lower conversion losses than an IGBT and 3.5x lower than a free-wheeling diode. The diode-based converter is more reliable than the active-switch-based counterparts due to the ruggedness of diodes [9] [32] and elimination of sensors, gate driving, as well as control circuits. Diodes are commercially available at higher VA ratings, *defined as product between the device voltage and current rating*, compared to IGBTs, as shown in Fig. 1.2, details are in Tables A.1 and A.2 in Appendix A. The surveyed IGBTs are the highest power rating of the type, while the diodes are not. Besides, the system cost could be potentially reduced: the diodes are commonly around 50 \$/MVA while the IGBTs are at least 200 \$/MVA.

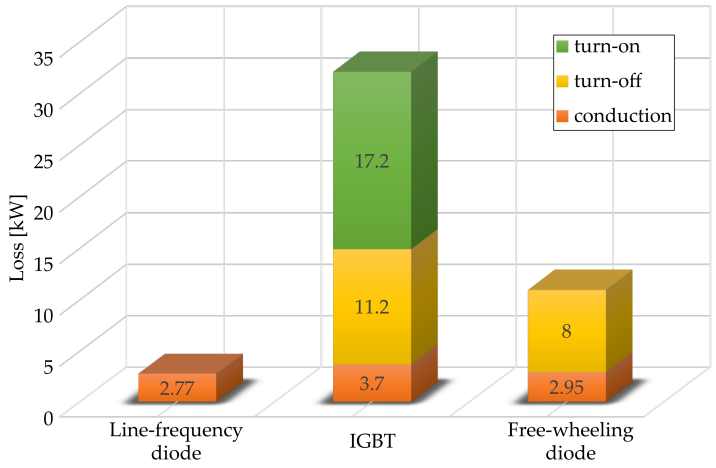


Figure 1.1: Line frequency diode has the lowest conversion losses compared to IGBT and free-wheeling diode because the loss mechanism only involves conduction.

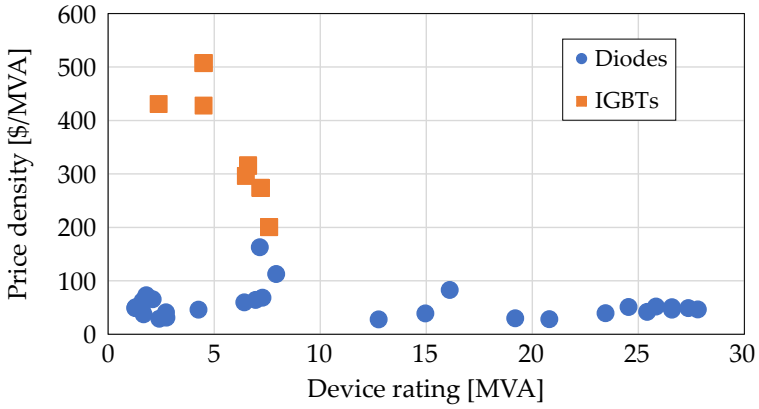


Figure 1.2: Diodes are available at higher MVA rating than IGBTs. In addition, the diodes have significantly lower price per MVA.

Although having favorable characteristics to achieve high conversion efficiency, high reliability, and compactness, diodes can not be forced to change the conduction state. Therefore, the diode bridge rectifier behaves as a voltage source when connected to a back-emf source. The output control objective must be achieved through a series-stacked controllable source. The type of controllable source is dictated by the control objective and the grid interface. For example, Fig. 1.3(a) depicts the voltage-source grid interface scenario. A series-stacked controllable current source can regulate the total power into the dc grid. On the other hand, Fig. 1.3(b) depicts a current-source dc-grid interface. The series stacked controllable voltage source can regulate the total output voltage.

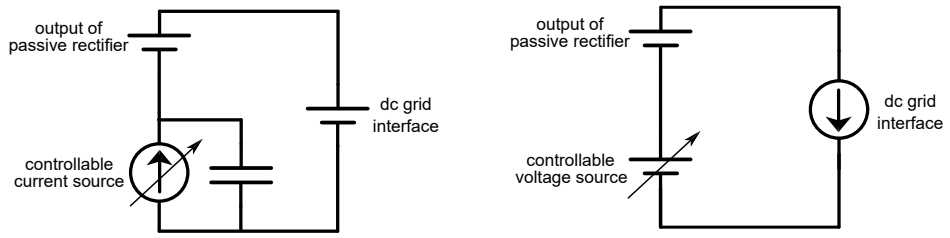


Figure 1.3: A series-stacked controllable source can control the output power of the passive rectifiers. The type of controllable source depends on the grid interface. (a) For a voltage-source grid interface, the controllable source is a variable current source. (b) For a current-source grid interface, the controllable source is a variable voltage source.

A multi-port PMSG is an appropriate generator candidate to satisfy the foregoing discussion. The generator includes two sections. One section, together with the active rectifier, forms a controllable source. The other section and diode bridges create the voltage source. The partial-power-rated active rectifier helps to meet the control objective while the passive rectifiers process most of the power. This configuration is promising to be an efficient, reliable, and compact ac-to-dc conversion architecture.

1.4 Key contributions

Key contributions of this dissertation including technical highlights and publication venues are as follows:

- The work explores the design space of an integrated generator-rectifier system and reveals potential benefits. From the design perspective, one-active-rectifier configuration minimizes the overall size [33]. The active-rectifier size and conversion losses are reduced 37% and 50% [34], respectively, in an electric ship, and by 39% and 47%, respectively, in a wind turbine [35]. Additionally, The active rectifier is shown to act like a total dc-bus voltage regulator. Under load-change and generator-speed-change conditions, the dc-bus voltage is regulated at the reference value. This contribution was published in Energy Conversion Congress & Expo 2018 [33], in Electric Ship Technology Symposium 2019 [34], and in IEEE Transactions on Power Electronics [35].

- The active-rectifier in the series-stacked architecture is shown to be able to play the role of an active filter: compensating the ripple voltage caused by the passive rectifiers. Injection of a directly-calculated d-axis current perturbation achieves the compensation when effects of the generator inductance are neglected [36]. When the effects are considered, the direct calculation approach fails because of the voltage ripple's un-defined derivatives at vertical edges caused by ac current commutation. Alternatively, a closed-loop ripple voltage compensator was developed based on lead-lag and proportional-resonant controllers. An overall controller architecture was developed to use the active rectifier as both filter element, and dc-bus voltage regulator [37,38]. This contribution was published in Applied Power Electronics Conference [36], in IEEE Transactions on Power Electronics [37], and in US patent [38].

- This work shows the integrated generator-rectifier system can regulate the total output dc-bus power, equivalent to the generator torque, under a fixed dc-bus voltage condition despite the uncontrolled diode bridges process the majority of power. Relationship between the active-rectifier d-axis current and the dc-bus power is analytically established and validate using simulation that captures the switching behavior of the power electronics [39]. Built upon [39], [40] analyzes the power ripple and the current total harmonic distortion for the whole operating speed range. The results show the generator torque ripple stays within 5% the rated torque even though most of the power is processed through passive rectifiers. The experimental results are extended to achieve MPPT at 380 W output power. This contribution was published in Energy Conversion Congress & Expo 2019 [39], and in IEEE Transactions on Power Electronics [40].

- The work in [37] and [40] assumes each generator phase is represented by a resistor, an inductor, and a back electro-motive-force source, all connected in series. Generally, this assumption does not hold in a multi-port generator because of the magnetic coupling between coils sharing the same magnetic structure. A general condition for the generator phases to be decoupled from the circuit perspective even though they share the same magnetic structure is derived in [41]. This work also discovers the trade-off between the dc-bus power ripple and the power output imbalance between an active rectifier and a passive rectifier. The condition provides guidelines for future generator development to take advantage of the

integrated rectifiers fully. This contribution was submitted to IEEE Transactions on Power Electronics [41].

- In addition to the technical feasibility and advantages, economic figures are desired to corroborate the suitability for offshore wind energy harvesting. The work in [42] shows a co-design framework to put together the rectifiers and the generators, as well as illustrates several economic merits, such as annual energy production (AEP) and levelized cost of electricity (LCOE). The results recognize that the improvements in the integrated generator-rectifier systems' overall conversion efficiency lead to higher AEP and lower LCOE than conventional solutions. This contribution was published in Energy Conversion Congress & Expo 2020 [42].

1.5 Dissertation organization

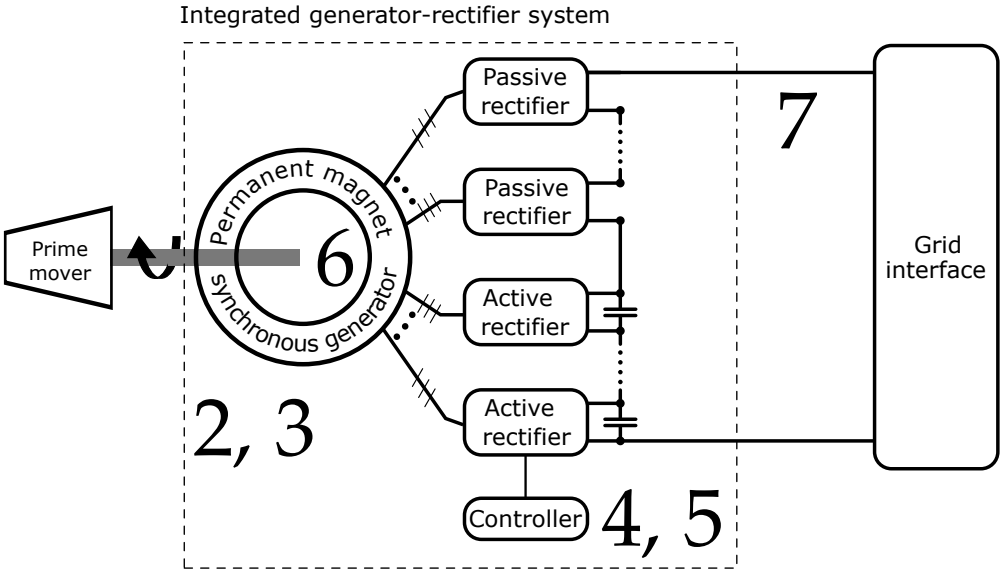


Figure 1.4: Organization of the dissertation: numbers represents the corresponding chapter to each portion of the integrated generator-rectifier system.

This dissertation discusses multiple aspects of the integrated generator-rectifier system to show the technical feasibility and the applications. Fig. 1.4 illustrates the chapter organization corresponding to the proposed system. First, the steady-state benefits and calculations of the key system

parameters are discussed in Chapter 2 and 3. From the power quality perspective, filter capacitors or appropriate phase-shift among active-rectifier ac ports could be implemented to achieve a high-quality output power. Alternatively, the active rectifier could be controlled to behave as a filter element. Details of the modeling and control strategy are discussed in Chapter 4.

Next, the key technical challenges are solved to make the integrated generator-rectifier system applicable to real-world applications. The active rectifier could be controlled as a voltage source. This control strategy leads to grid forming applications, as discussed in the latter part of Chapter 4. Besides, the active rectifier could behave as a current source as well. Chapter 5 utilizes this feature to explore the possibility of using a fractional-power-rated active rectifier to control the total dc-bus power. This capability allows regulation of wind-turbine output electrical power, making maximum power point tracking possible.

Due to the integrated nature of the architecture, only specific generator configurations could provide a successful integration. Chapter 6 derives the generator's theoretical requirements to allows the proper integration with the power-electronics architecture. This theoretical analysis paves the way for future generator development to enhance the overall system power density further. Finally, quantification of system benefits in terms of annual energy production is presented in Chapter 7 to illustrate this work's implications on the electricity end users.

Chapter 2

AN INTEGRATED GENERATOR-RECTIFIER SYSTEM

This chapter proposes the integrated generator-rectifier system based on a k-port PMSG. The configuration based on one active rectifier and the rest to be passive rectifier is shown to be optimal in terms of minimizing the active rectifier dc-side voltage. Minimization of the active-rectifier VA rating leads to a selection of the generator number of ac ports. The advantages are then illustrated through power processed by the active rectifier and reduction in conversion losses.

2.1 Proposed architecture

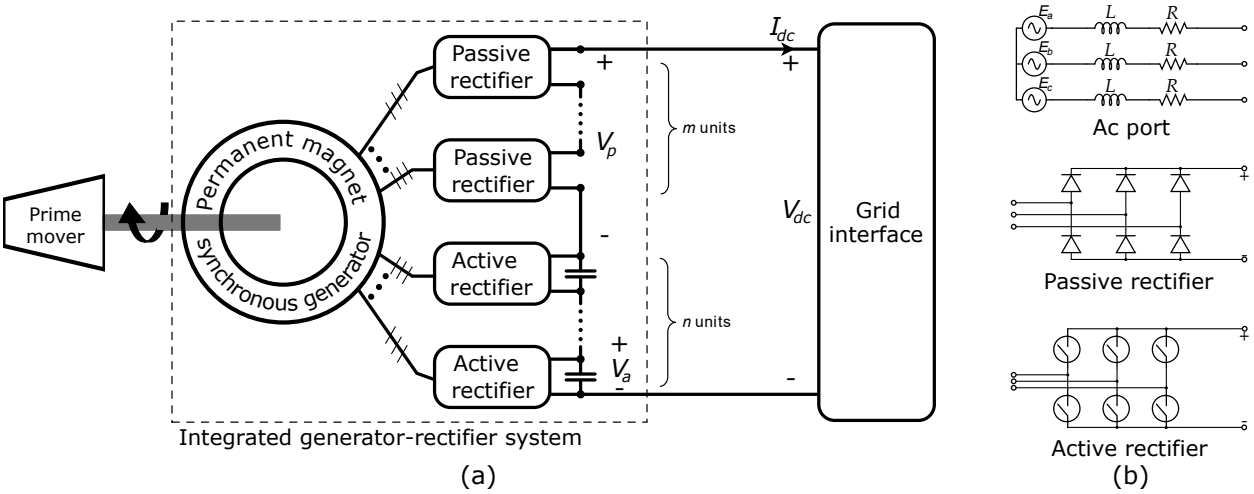


Figure 2.1: The proposed ac-to-dc conversion architecture integrated with a multi-port PMSG, driven by a prime mover operating over a limited speed range: (a) the PMSG has $m + n$ three-phase electrical ports connected to m passive and n active rectifiers, each port powers one. The dc output of these rectifiers are serially stacked and connected to a dc-bus. (b) Each of the ac ports operates as an isolated three-phase source. The passive rectifier is three-phase diode bridge. The active is a three-phase bridge rectifier with IGBTs as the switching devices.

A series-stacked ac-to-dc conversion architecture integrated with a multi-port PMSG is pro-

posed, shown in Fig. 2.1. It achieves a regulated dc bus or power-flow control while substantially reducing the need for actively-controlled power electronics switches. A prime-mover-driven PMSG has multiple three-phase ac ports. Each is connected either to an active rectifier, consisting of actively-controlled power electronics switches, or to a passive rectifier, comprising only diodes. A two-level converter is chosen to represent the active rectifier in Fig. 2.1(b). However, the active-rectifier circuit topology is not limited to only two-level. Serially stacking the dc outputs of n active with m passive rectifiers creates a relatively high voltage dc-bus compared to the individual switch rated voltage. Each rectifier provides a fraction of the voltage.

The active rectifiers regulate the dc bus voltage or performs power flow control as the prime-mover operates at variable speeds. Supporting a fraction of the dc-bus voltage, they process only a partial of the total power, leading to a substantial loss reduction. Extensive use of diodes commuting at line frequency improves the power-circuit reliability because the diode failure rate is more than 10x lower compared to power transistor [32]. In addition, employing diodes on the high-voltage side of the dc bus simplifies the hardware, eliminating numerous isolated gate drivers and voltage sensors, further improving the overall system reliability.

Multi-port and multi-phase permanent magnet synchronous generator (PMSG) designs have been considered to reduce the individual converter size and provide redundancy for improved system reliability [6, 26–29]. However, the existing multi-port generator topologies do not guarantee mutual decoupling among phases from a circuit point of view. Chapter 6 will be clarify the decoupling notion and propose appropriate generator winding layout. For the purpose of design and control discussed in Chapters 2–5, the coupling condition is assumed. Each phase of the generator is represented by a back electromotive force (emf) source in series with a resistor and an inductor (RLE model).

2.2 Design process

A PMSG with k accessible three-phase ports is considered. At the maximum speed, the PMSG delivers a rated power of P_0. The sum of line-to-neutral back electromotive force (emf) of all the ac ports is E_0. As the back emf is proportional to the operating speed, the peak line-to-neutral

value is ωE_0 where ω is the per-unit speed with the generator maximum speed as the base value. Assuming the ac ports are identical, each has a back emf value of

$$E(\omega) = \frac{\omega E_0}{k}. \tag{2.1}$$

Neglecting the generator stator-winding resistance, synchronous inductance, and the diode forward voltage drop, the average dc output voltage of each passive rectifier is

$$V_{passive} = \frac{3}{\pi}\sqrt{3}E(\omega), \tag{2.2}$$

which depends only on the generator speed. The dc-bus voltage value is selected to ensure the active-rectifier controllability at all the generator speeds. Considering a conventional single ac port with full power-rated active rectifier and assuming a space vector modulation strategy, the dc-bus voltage is at least the generator line-to-line back emf. The minimum value is selected to be the nominal dc-bus voltage:

$$V_{dc} = \sqrt{3}E_0. \tag{2.3}$$

At a lower operating speed, the dc output of the each passive rectifier governed by equation (2.2) decreases. The total decrease must be compensated by the series connected active rectifiers to maintain the dc bus voltage at $V_{dc,nom}$. Using (2.1), (2.2), and (2.3), the total dc output voltage of n active rectifiers depends on ω as

$$V_a = V_{dc} - mV_{passive} = \left(k - m\frac{3}{\pi}\omega\right)\sqrt{3}\frac{E_0}{k}. \tag{2.4}$$

Normalizing (2.4) by the base voltage, defined as

$$V_{base} = \frac{V_{dc}}{\sqrt{2}}, \tag{2.5}$$

the total dc output voltage of the active rectifiers in p.u. is

$$V_a^{pu} = \sqrt{2}\left(1 - \omega\frac{3}{\pi}\frac{m}{k}\right). \tag{2.6}$$

Equation (2.6) highlights that the total dc voltage requirements of active rectifiers depends on the generator speed, number of PMSG ac ports, and number of passive rectifiers. This generalized equation forms the basis for minimizing both the voltage rating and the VA rating of the active rectifiers.

2.2.1 Selection of number of passive rectifiers

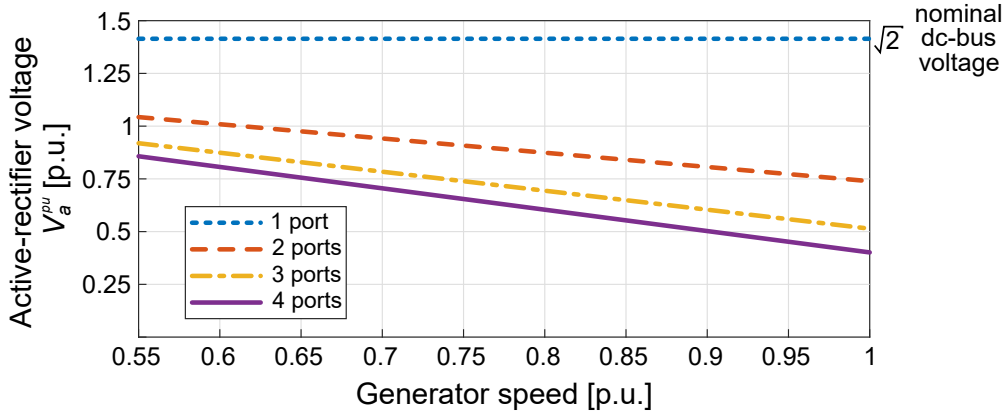


Figure 2.2: Active-rectifier dc-side voltage increases as the generator speed decreases.

The next step in the design process is to find the number of passive and active rectifiers for a k-port PMSG such that the total dc output voltage of the active rectifiers is minimized. Equation (2.6) shows V_a^{pu} decreases as m increases. As at least one active rectifier is essential to provide a dc bus voltage regulation or to control the power flow, the maximum possible value of m must be $k-1$. This design choice and (2.6) set the active rectifier output voltage requirement to a minimum value, that is

$$V_a^{pu} = \sqrt{2}\left(1 - \omega\frac{3}{\pi}\frac{k-1}{k}\right). \tag{2.7}$$

This equation suggests that the active rectifier must support a higher dc voltage at a lower generator

speed. Figure 2.2 shows this effect for different k values. For example, a four-port PMSG requires the active rectifier to support 28.3% the dc bus voltage at 1 p.u. operating speed and 60.6% at 0.55 p.u. In contrast, a single-port PMSG requires the active rectifier to support 100% the dc bus voltage at all the operating speeds.

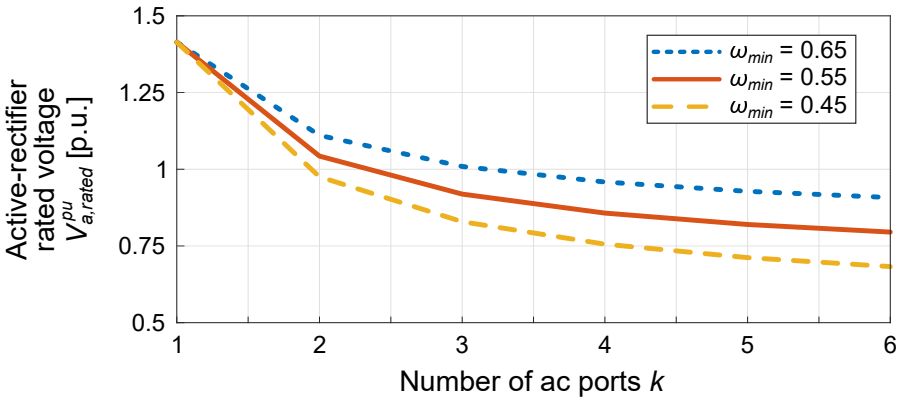


Figure 2.3: The active-rectifier rated voltage decreases as the number of ac ports increases. A lower minimum generator speed leads to a higher voltage requirement.

The maximum voltage support requirement of the active rectifier is its voltage rating. Equation (2.7) shows that the voltage rating corresponds to the minimum generator speed ω_{min} and is given by

$$V^{pu}_{a,rated} = \sqrt{2}\left(1 - \omega_{min}\frac{3}{\pi}\frac{k-1}{k}\right). \tag{2.8}$$

Figure 2.3 illustrates the dependency of the voltage rating on k for three different ω_{min} values. The voltage rating of the active rectifier decreases with an increase in number of ac ports but at a diminishing rate. The figure also demonstrates the advantage of the proposed architecture in limited-speed-range applications—the narrower the operating speed range, corresponding to a lower minimum generator speed, the greater the reduction in the voltage rating requirement. The operating speed range is application dependent. In wind-turbine applications, the minimum-to-maximum operating speed ratio is frequently chosen to be 0.7:1.3 for doubly-fed-induction-machine systems to achieve a high energy-captured-to-cost ratio [4]. In the proposed architecture, an identical speed range implies ω_{min} to be 0.55 p.u. Similarly, in gas-turbine driven applications,

such as electric ships, an ω_{min} of 0.82 p.u. increases the thermal efficiency by 3% at a light-load operation [7].

2.2.2 Selection of number of ac ports

Equation (2.8) suggests that the number of ac ports should be increased to reduce the active-rectifier voltage rating. From a system design perspective, the active rectifier VA rating, *defined as the product of the voltage rating and the current rating*, is a more important criterion. It governs the converter size, weight and cost. As shown later, the VA-rating minimization leads to the selection of the generator number of ac ports. The design step is determination of the active-rectifier current rating, an intermediate quantity to compute the VA rating.

The active rectifier current rating is set by the maximum peak-ac-line current. The peak-ac-line current is determined by the ac-side and dc-side power balance. Assuming a unity power factor operation of the active rectifier, the power-balance relationship is

$$\frac{3}{2}E(\omega)I_{ac} = V_a I_{dc}, \tag{2.9}$$

where I_{ac} and I_{dc} are the peak-ac line and dc side currents, respectively. Use (2.1), (2.4), and set m to $k-1$,

$$I_{ac} = \frac{2}{\sqrt{3}}\left(\frac{k}{\omega} - \frac{3}{\pi}(k-1)\right)I_{dc}. \tag{2.10}$$

Normalizing both sides of (2.10) by

$$I_{base} = \frac{P_{base}}{\sqrt{3}V_{base}} \tag{2.11}$$

where P_{base} is the system base power, the peak-ac-line current is expressed in p.u. as

$$I_{ac}^{pu} = \frac{2}{\sqrt{3}}\left(\frac{k}{\omega} - \frac{3}{\pi}(k-1)\right)I_{dc}^{pu}. \tag{2.12}$$

The maximum value of the peak-ac-line current across the entire operating speed range determines

the current rating and is given by

$$I_{a,rated}^{pu} = \max_{\omega \in [\omega_{min},\,1]} \frac{2}{\sqrt{3}}\left(\frac{k}{\omega} - \frac{3}{\pi}(k-1)\right) I_{dc}^{pu}. \tag{2.13}$$

Computation of this normalized current rating requires I_{dc}^{pu} to be expressed as a function of ω.

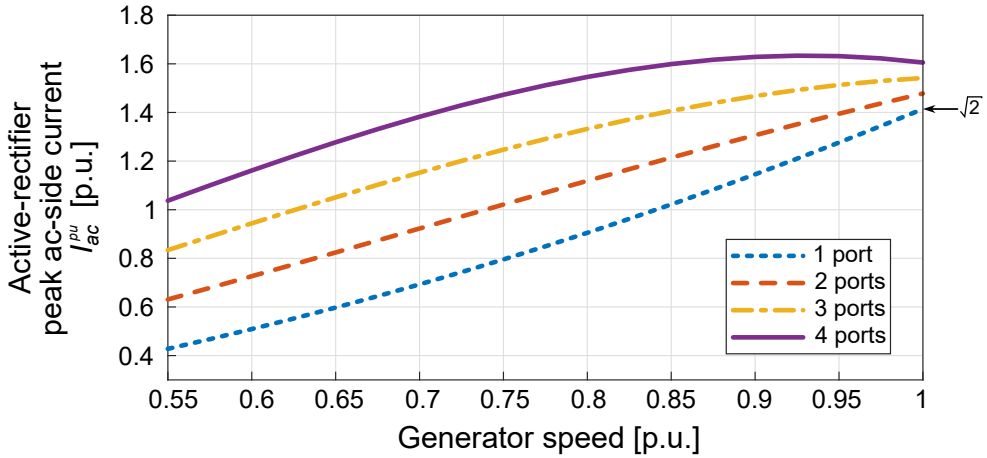


Figure 2.4: Dependency of the active-rectifier peak ac-side voltage on the generator speed and the number of ac ports.

The per-unit dc-bus current is typically a function of the per-unit generator speed. At the rated value, the current value is derived by assuming the base power at the dc bus:

$$I_{dc,rated}^{pu} I_{base} V_{dc} = P_{base}. \tag{2.14}$$

Substituting (2.3) and (2.11) into (2.14), the rated per-unit dc-bus current is

$$I_{dc,rated}^{pu} = \frac{\sqrt{3}}{\sqrt{2}}. \tag{2.15}$$

Considering a wind-turbine application, the amount of power extracted from the mechanical structure is proportional to cube of the generator speed [12, 39, 43]. Neglecting the conversion losses, the dc-bus power assumes the same value as the amount of power being extracted. Due to a constant dc-bus voltage, the dc-bus current must be proportional to the cube of the generator speed to

allow power variation to achieve MPPT. In per unit, the dc-bus current is

$$I_{dc}^{pu}(\omega) = I_{dc,rated}^{pu}\omega^3 = \frac{\sqrt{3}}{\sqrt{2}}\omega^3. \tag{2.16}$$

Figure 2.4 illustrates the ac-side current versus generator speed for different number of ac ports in a wind-energy application. The current rating does not necessarily occurs at the unity generator speed. For example, a four-port system has a current rating of 1.63 p.u. at a speed of 0.93 p.u. Compared to a conventional single-port system, the rated current is $\sqrt{2}$ at 1 p.u. speed. Using a multi-port generator may have increased the active-rectifier current requirement.

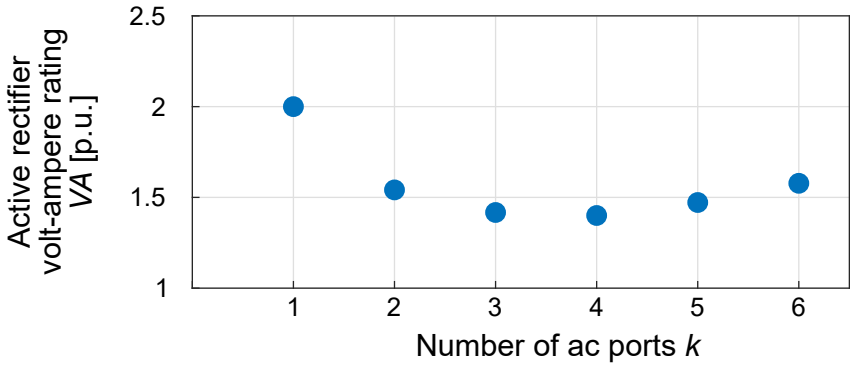


Figure 2.5: The active-rectifier VA rating has a minimum value when the number of ac ports varies.

Utilizing a multi-port PMSG reduces the active-rectifier voltage requirement, as illustrated in Fig. 2.2, but may increase the current requirement, as shown in Fig. 2.4. From the power electronics design perspective, not the individual voltage nor current rating, but the product is crucial because this quantity closely relates to the converter size, weight, and cost. Define the active-rectifier per-unit volt-ampere rating as

$$VA^{pu} = V_{a,rated}^{pu} I_{a,rated}^{pu}, \tag{2.17}$$

where voltage and current rating are given by (2.8) and (2.13), respectively. The per-unit quantity

given by (2.17) can be converted to SI unit using

$$VA = \frac{VA^{pu} P_{base}}{\sqrt{3}}. \tag{2.18}$$

The per-unit VA rating is a non-linear functions of k. Figure 2.5 illustrates the non-linearity by showing the product between voltage and current ratings from Figs. 2.3 and 2.4. Evidently, there exist an optimal number of ac ports that minimize the active-rectifier VA rating, given by

$$k_{opt} = \underset{k \in \mathbb{N}^+}{\text{argmin}} \; VA^{pu}, \tag{2.19}$$

minimizes the active rectifier VA rating. For the illustrated example, k_{opt} is 4. The corresponding VA rating is 1.4 p.u., compared to 2 p.u. of the conventional single-port system. Utilizing a multi-port PMSG reduces the active-rectifier size by 30% in wind-energy applications. This concludes the design process.

2.3 Steady-state performance

This section discusses the key performance metric of the proposed architecture. First, power processed by the active rectifier is presented. A substantial reduction in the power processed by the active rectifier is achieved compared to the conventional single-port PMSG system. This reduction leads to a lower conversion losses. From a thermal design perspective, the ac-to-dc power converter size, weight, and cost can be reduced. The improvements are illustrated using a wind-energy conversion system that is rated for 10 MW and delivers power to a 5715 V dc-bus.

2.3.1 Power processed by the active rectifier

The power processed by the active rectifier is dependent on the voltage and current at a specific operating speed. At any operating speed ω, power processed by the active rectifier is the product

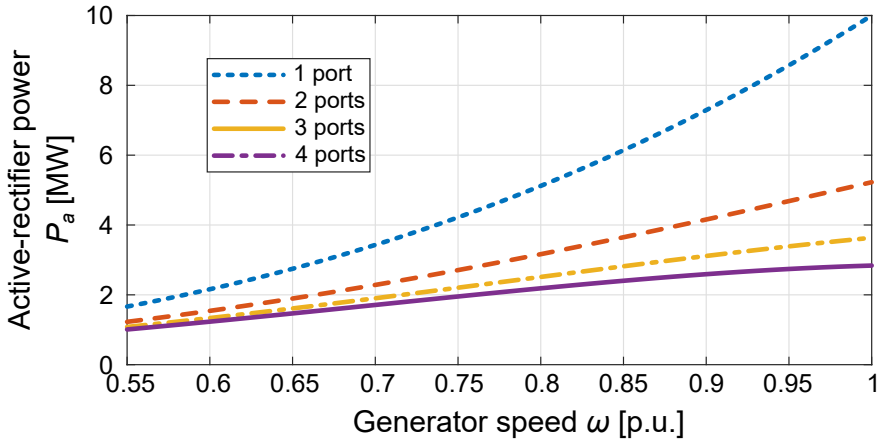


Figure 2.6: The integrated generator-rectifier system reduces the amount of power processed by the active rectifier across the whole generator speed range in wind-energy application.

of the output dc voltage and the output dc current:

$$P_a(\omega) = V_a^{pu}(\omega) V_{base} I_{dc}^{pu}(\omega) I_{base}. \tag{2.20}$$

While $V_a^{pu}(\omega)$ is determined by (2.17), I_{dc}^{pu} is application dependent. For example, for a wind turbine, I_{dc}^{pu} equals ω^3. Figure 2.6 shows the amount of power processed by the active rectifier. Utilizing a multi-port PMSG reduces the amount of power processed by the active-rectifier throughout the operating speed range. At the rated generator speed, a three-port design requires the active-rectifier to process 3.6 MW out of the 10 MW system rated power. Processing most of the power on the passive rectifier leads a significant reduction in conversion losses, as to be illustrated in Section 2.3.2.

2.3.2 Conversion efficiency

This section illustrates the improvement on conversion efficiency. Power electronics switches are selected to support the required voltage and current rating of the active rectifier, as calculated in Section 2.2. The rated values for different numbers of ac ports are summarized in Table 2.1. Assuming a two-level active rectifier topology, each switch must be rated for $V_{a,rated} = V_{a,rated}^{pu} V_{base}$ and $I_{a,rated} = I_{a,rated}^{pu} I_{base}$.

Passive rectifiers are assumed to be constructed from discrete diodes. A lower voltage margin of

Table 2.1: IGBT selection

k	$I_{a,rated}$ [A]	$V_{a,rated}$ [V]	IGBT	$N_{parallel}$	N_{series}
1	2020	5715	FZ500R65KE3 NOSA1-ND	3	2
2	2111	4214	FZ500R65KE3 NOSA1-ND	3	1
3	2202	3714	FZ500R65KE3 NOSA1-ND	3	1
4	2333	3464	FZ500R65KE3 NOSA1-ND	3	1

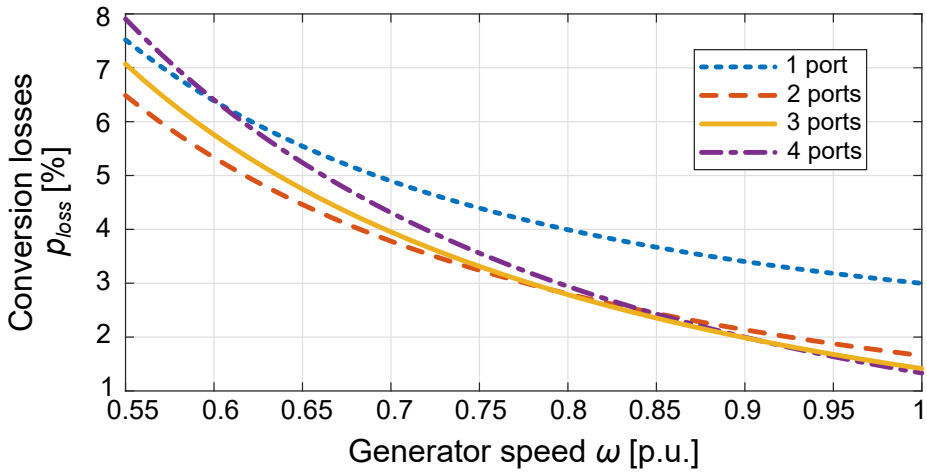


Figure 2.7: The active-rectifier VA rating has a minimum value when the number of ac ports varies.

10% is sufficient for diodes on the passive rectifiers, as they switch at ac source frequency. Vishay VS-SD2500C20K 3000-A, 2000-V rectifier diodes are chosen.

Active-rectifier switches are assumed to be constructed from IGBTs. Due to limited voltage and current rating of the IGBTs, series and parallel connecting multiple devices may be required to form a switch. Consider a single-port PMSG, the active rectifier rated voltage is 5715 V. Allowing 50% voltage margin for a safe operation, each switch in the active rectifier must support a voltage of $1.5 \times 5715 = 8572.5$ V. The highest voltage IGBT available on the market is Infineon FZ500R65KE3NOSA1-ND [31], which has a voltage rating of 6500 V and a current rating of 1000 A. Two IGBTs needs to be connected in series to support the required voltage. The active-rectifier rated current is 2020 A. Three IGBTs must be connected in parallel to meet the current requirement. Similarly, number of parallel and series IGBTs for two, three, and four ac-port PMSG are listed in Table 2.1.

Table 2.2: IGBT data for loss calculation

IGBT specs	Notation	Unit	FZ500R65KE3 NOSA1-ND [31]
Collector-emitter voltage	V_{rated}	V	6500
Peak forward current	I_{CN}	A	1000
Free-wheel diode forward voltage at low current	V_{F0}	V	1
Free-wheel diode forward voltage at peak current	V_F	V	4
Collector-emitter at low current	V_{CE0}	V	1
Collector-emitter voltage at peak current	V_{CEN}	V	5.2
IGBT rising time	t_r	μs	0.4
IGBT falling time	t_f	μs	0.5
Free-wheel diode reverse recovery charge	Q_{rr}	μC	1050
Switching frequency	F_S	kHz	2

The conversion losses include passive and active rectifier losses. For a passive rectifier, the conduction loss is the dominant component as these devices are switching at the ac source frequency. The power loss on each passive rectifier is

$$P_{loss}^{passive} = 2V_{FM}^{passive} I_{dc}^{pu} I_{base}, \tag{2.21}$$

where $V_{FM}^{passive}$ is the forward-voltage drop of the diodes used in the passive rectifiers.

For the active rectifier, the power losses include that in the IGBTs (conduction and switching) and free-wheeling diodes (conduction and reverse recovery). The losses are estimated using (18), (21), and (27) of [44] and (10) and (11) of [45], with an assumption of unity power factor. Therefore, the total loss on the series-stacked ac-dc conversion system is

$$\begin{aligned} P_{loss} =& (k-1)P_{loss}^{passive} \\ &+ 6N_{series}N_{parallel}(P_{igbt}^{cond} + P_{igbt}^{on} + P_{igbt}^{off} + P_{diode}^{cond} + P_{diode}^{rr}), \end{aligned} \tag{2.22}$$

where P_{igbt}^{cond}, P_{igbt}^{on}, and P_{igbt}^{off} represent the conduction, turn-on, and turn-off losses on the IGBT, respectively. P_{diode}^{cond} and P_{diode}^{rr} stand for conduction loss and reverse-recovery loss of the free-wheeling diode. N_{series} and $N_{parallel}$ are number or series and parallel IGBTs forming each switch,

respectively. The normalized conversion loss is given by

$$p_{loss} = \frac{P_{loss}}{P_{base}}\%. \tag{2.23}$$

Table 2.2 summarizes the device data required to compute the conversion losses. The passive diode voltage drop $V_{FM}^{passive}$ is 1.4 V [46]. Figure 2.7 shows the estimated conversion efficiency for the 5715-V, 10-MW dc bus system for wind-turbine application. The conversion losses is reduced across the whole operating speed range. Consider the minimum active-rectifier size design, $k = 3$, the conversion losses at the rated generator speed is 1.42%, a 52.7% reduction compared to the 3% of the conventional single-port system.

2.4 Experimental verification

A three-phase, 48-pole, 350 rpm, 160 watt PMSG is used to demonstrate the functionality of the proposed architecture. Each phase comprises 12 coils in series. The stator is customized to externally access all the coil terminals, as shown by Fig. 2.8(a, b). The external access allows different number-of-ac-port configurations for the PMSG. Each coil has an inductance and resistance of 2.5 mH and $0.5\ \Omega$, respectively. The back emf constant for each winding is 0.03125 V/rpm. The PMSG can be configured as one-port, two-port, three-port, and four-port through external connections. The 1-port configuration is the conventional architecture, because all the power is processed by the active rectifier. Other configurations are realizations of the proposed architecture. The setup is shown in Fig. 2.8(c). For the multi-port configuration, one ac port feeds a Texas Instrument High Voltage Motor Control and PFC Developer's Kit, named Rec-1, which operates as the active rectifier and switches at 10 kHz. The rest of the ac ports are connected to passive rectifiers constructed from MT3516A-BP three-phase diode bridges. Each diode has a forward voltage drop of 1.2 V. Dc outputs of all the rectifiers are serially connected to form the dc bus. A resistor load bank is used to draw power from the generator. A speed-controllable prime mover drives the PMSG. The dc-bus voltage is maintained at 260 V by a feedback controller implemented on the active rectifier for all operating speeds and loading conditions. The experimental results are generated using a wind load profile, which is proportional to the cube of the generator operating speed.

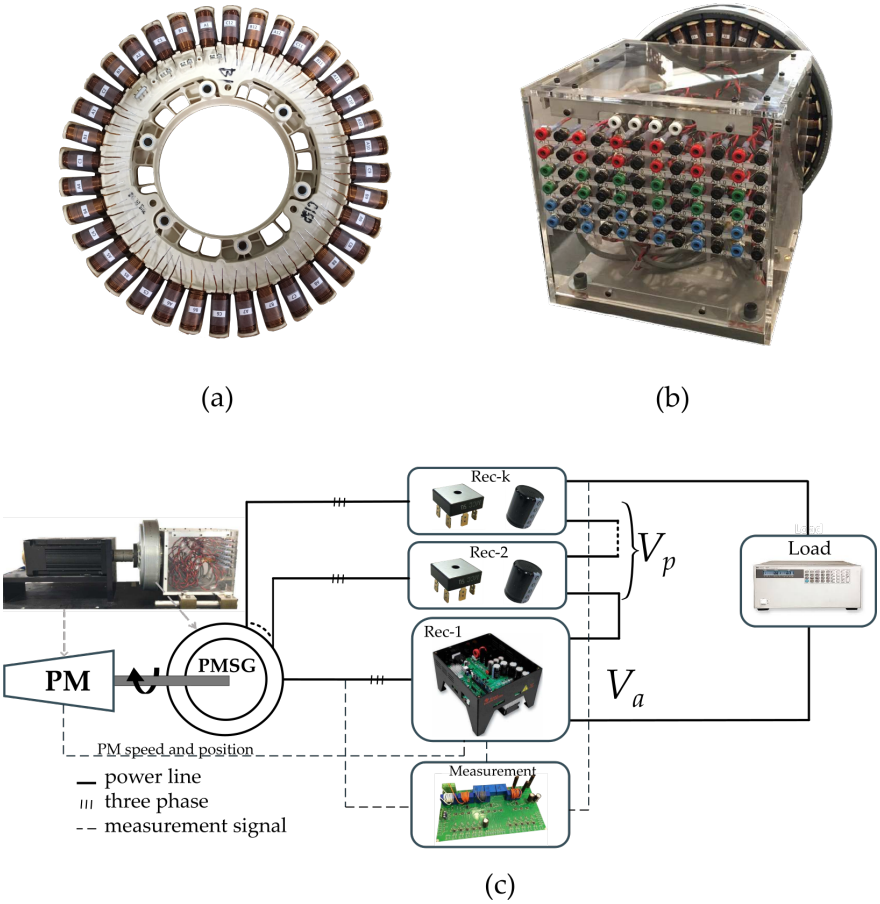


Figure 2.8: (a) Stator of a 36 slot PMSG used as the multi-port generator for the experimental setup. All the tooth coils are externally accessible. (b) The generator assembly with a front panel allows access to the winding terminals through binding posts. (c) Experiment setup: a prime mover rotates the PMSG at a controllable speed. The ac power is converted to dc by the proposed series-stacked architecture. The active rectifier senses the rotor position, ac-line, dc-bus voltage, and current to regulate the dc-bus at a constant voltage under different 6PMSG operating speed and loading conditions.

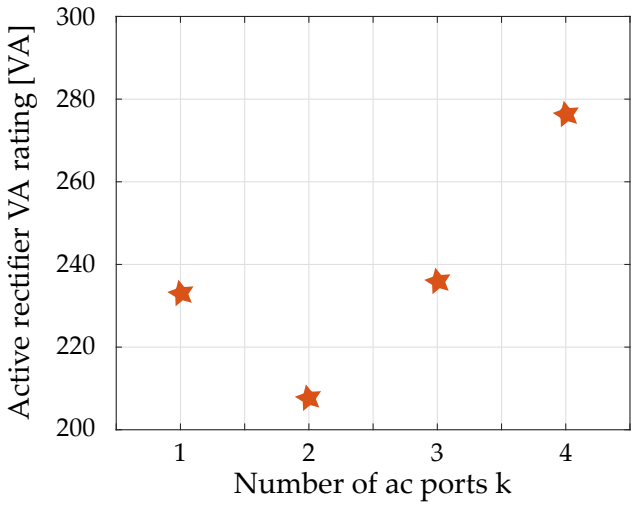


Figure 2.9: Varying number of ac-port changes the VA requirement of the active rectifier. Two-port configuration is optimal for the tested generator.

2.4.1 VA rating of the active rectifier

For each PMSG configuration, the active rectifier VA rating is calculated from the experimental setup by multiplying the maximum ac-line current and the maximum dc-side voltage of the active rectifier for all operating conditions, as shown in Fig. 2.9. For this PMSG, a two-port configuration minimizes the active rectifier VA rating. With one-port configuration, the VA rating is 233 VA while for a a two-port configuration, the VA rating reduces to 209 VA. As the number of ac ports increases, the active rectifier VA rating increases significantly.

2.4.2 Power processed by the active rectifier

Figure 2.10 shows that the power processed by the active rectifier. Using a multi-port PMSG, power processed by the active rectifier is reduced across the whole operating speed range. At the rated speed, 100 out of 166 watts are processed by the active rectifier, equivalent to 60%.

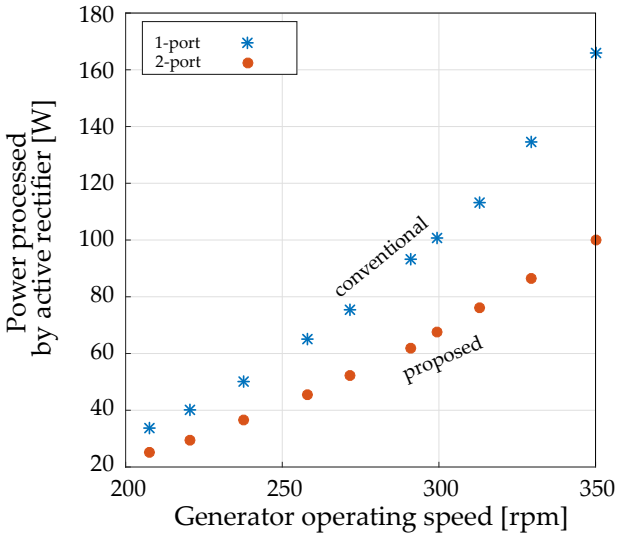


Figure 2.10: For multi-port configuration, the active rectifier processes partial power.

2.4.3 Conversion efficiency improvement

Figure 2.11 compares the conversion loss in the two configurations. The loss is measured by subtracting the measured dc-bus power from the total generator output power. The experimental results present a couple of trends that align well with the theoretical calculations in Fig. 2.7. First, the conversion system is more efficient at the rated operating condition compared to a low-speed operation. At the rated speed, majority of the power is processed by the passive rectifiers. At a lower operating speed, the active rectifier shares a dominant portion of the total power, and hence, the overall loss percentage increases. Second, the conversion loss is reduced across the whole operating speed range. The reduction ranges between 33% and 12% based on the operating speed.

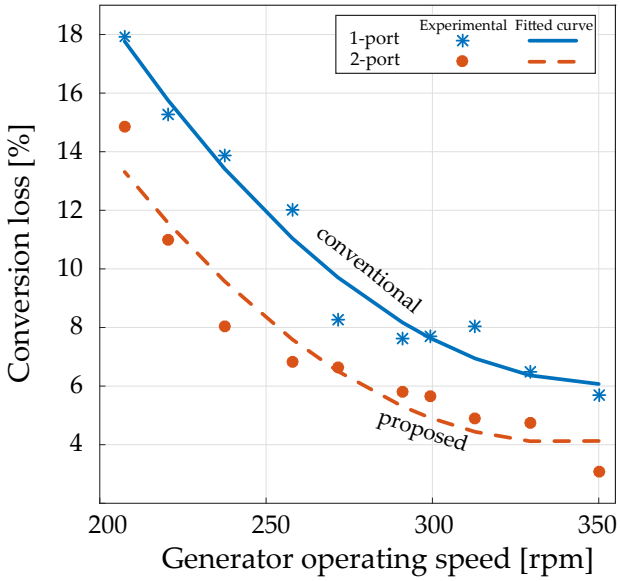


Figure 2.11: Reducing power processed by the active rectifier improves the conversion efficiency at all the operating conditions.

2.5 Conclusions

This chapter has proposed and discuss the design process of an integrated generator-rectifier system and illustrate the concept for wind-energy applications. Utilizing a multi-port PMSG leads reduces the amount of power processed by the active rectifier throughout the whole generator speed range. The active power electronics devices are inherently more lossy compared to the passive counterpart due to additional switching losses. Processing partial power on the active rectifier leads to a significant reduction in the total conversion losses.

The forgoing discussions are based on idealistic conditions, i.e., the winding resistance and the synchronous inductance of the PMSG is omitted. In practice, the resistance can be neglected but not the synchronous inductance. Practical design methodology considering these parasitic element effects is discussed in Chapter 3.

Chapter 3

DESIGN CHOICE CONSIDERING EFFECTS OF THE DIODE-BRIDGE COMMUTATION INDUCTANCE

The benefits of an integrated generator-rectifier system illustrated in Chapter 2 originate from a partially-power-rated active rectifier. Additional reduction in the active-rectifier size would further enhance the benefits. This chapter shows additional size reduction is possible by reducing the dc-bus voltage.

3.1 Dc-side voltage of the active-rectifier in system with the conventional dc-bus voltage

Consider the integrated generator-rectifier system shown in Fig. 2.1 with PMSG synchronous inductance L. The dc-bus voltage is maintained at the level for the conventional single-port configuration, i.e., $V_{dc} = \sqrt{2}V_{base}$. Out of k ac ports, one powers an active rectifier and $k-1$ power passive rectifiers. The dc-output voltage of $k-1$ passive rectifiers is

$$V_p(\omega) = \frac{3}{\pi}(k-1)\sqrt{3}E(\omega) - \frac{3}{\pi}\omega\frac{(k-1)}{k}LI_{dc}(\omega) \tag{3.1}$$

where ω is the per-unit electrical frequency, and I_{dc} is the dc-bus current. The synchronous inductance is assumed to be sufficiently small such that the passive rectifier operates in Mode I [47]. The active-rectifier dc-side voltage is the difference between the constant dc-bus voltage and the passive-rectifiers output:

$$V_a(\omega) = V_{dc} - V_p = V_{dc}^{pu}V_{base} - \frac{3}{\pi}(k-1)\sqrt{3}E(\omega) - \frac{3}{\pi}\omega\frac{k-1}{k}\omega_0 LI_{dc}(\omega). \tag{3.2}$$

where ω_0 is the rated electrical frequency. Normalizing both sides of (3.2) by V_{base}, the per-unit active-rectifier dc-side voltage is

$$V_a^{pu} = V_{pu}^{dc} - \frac{3}{\pi}\sqrt{2}\frac{(k-1)}{k} - \frac{3}{\pi}\omega\frac{k-1}{k}X_{pu}^{L}\frac{P_{dc}^{pu}(\omega)}{V_{dc}^{pu}}. \tag{3.3}$$

The following relationships are used to simplified the equation:

$$X_{pu}^{L} = \frac{\omega_0 L}{Z_{base}}, \quad Z_{base} = \frac{V_{base}^2}{P_{base}}, \quad \text{and} \quad I_{dc}(\omega) = \frac{P_{dc}^{pu}(\omega)P_{base}}{V_{dc}^{pu}V_{base}}.$$

Assuming a state-space modulation strategy, the minimum active-rectifier dc-side voltage must satisfy

$$V_{a,min} = \sqrt{3}E(\omega) \tag{3.4}$$

where $E(\omega)$ is given by equation (2.1).

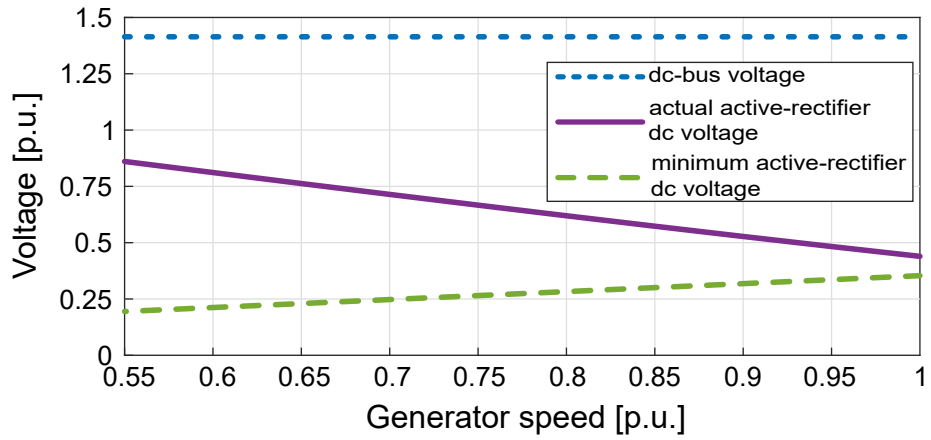


Figure 3.1: Maintaining the dc-bus voltage at the conventional value for single-port system (dotted-blue line) leads to dc-side voltage of the active-rectifier (solid-purple line) being higher than the minimum required value (dashed-green line) in a multi-port system.

Figure 3.1 illustrates the dc-bus , the active-rectifier dc-side, and the minimum voltage for a four-port configuration in wind-energy application, i.e., $P_{dc}^{pu}(\omega) = \omega^3$. At the rated generator speed, the actual active rectifier dc-side voltage is higher than the minimum requirement. It is possible to reduce the active rectifier dc-side voltage to only the minimum required value by reducing the dc-

bus voltage. Such reduction leads to lower voltage and current ratings, and consequently a smaller active-rectifier size. Details on the dc-bus voltage selection is presented in Section 3.2.

3.2 Dc-bus voltage design

The dc-bus voltage is calculated such that the active rectifier remains controllable at the rated condition. Assuming a space-vector-modulation strategy, the minimum active-rectifier dc-side voltage at the rated condition is

$$V_{a,min}^{pu} = \frac{\sqrt{2}}{k}. \tag{3.5}$$

Equating the right-hand sides of (3.5) and (3.3), as well as using $\omega = 1$ and $P_{dc}(\omega = 1) = 1$, the equation determining the minimum dc-bus voltage that ensures controllability of the active rectifier is

$$(V_{dc}^{pu})^2 - \frac{\sqrt{2}}{k}\left(\frac{3}{\pi}(k-1)+1\right)V_{dc}^{pu} + \frac{3}{\pi}\frac{k-1}{k}X_{pu}^{L} = 0. \tag{3.6}$$

The minimum dc-bus voltage is the positive root of equation (3.6).

The per-unit inductance X_L^{pu} and number of ac ports k are the two parameters determining the dc-bus voltage. Figure 3.2 illustrates the dependency of the dc-bus voltage on the number of ac ports and the per-unit reactance. As expected, the dc-bus voltage could be reduced in a multi-port PMSG compared to a single-port configuration. Reduction in the dc-bus voltage leads to lower active-rectifier voltage and current requirement, as to be illustrated in Section 3.3.

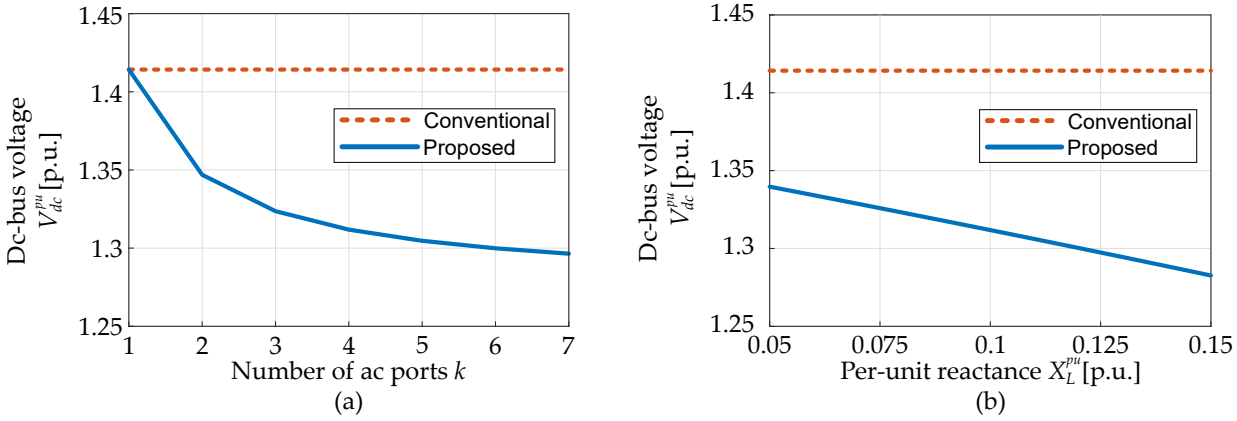


Figure 3.2: The proposed calculation leads to a lower dc-bus voltage compared to the conventional value. The figure illustrates dc-bus voltage versus (a) number of ac ports for $X_L^{pu} = 0.1$, (b) the per-unit reactance for a four-port configuration.

3.3 Effects of a lowered dc-bus voltage

Lowering the dc-bus voltage leads to a reduced active-rectifier dc-side voltage across the whole generator speed range, as shown in Fig. 3.3 for a four-port system with $X_L^{pu} = 0.1$. Conventionally, the active rectifier dc-side voltage is higher than the minimum required value. Using a dc-bus voltage calculated by equation (3.6), the active rectifier stays exactly at the minimum required value at the rated generator speed. As the speed decreases, the minimum required dc-side voltage reduces while the active-rectifier dc-side voltage increases. Consequently, the active rectifier remains controllable throughout the generator speed range.

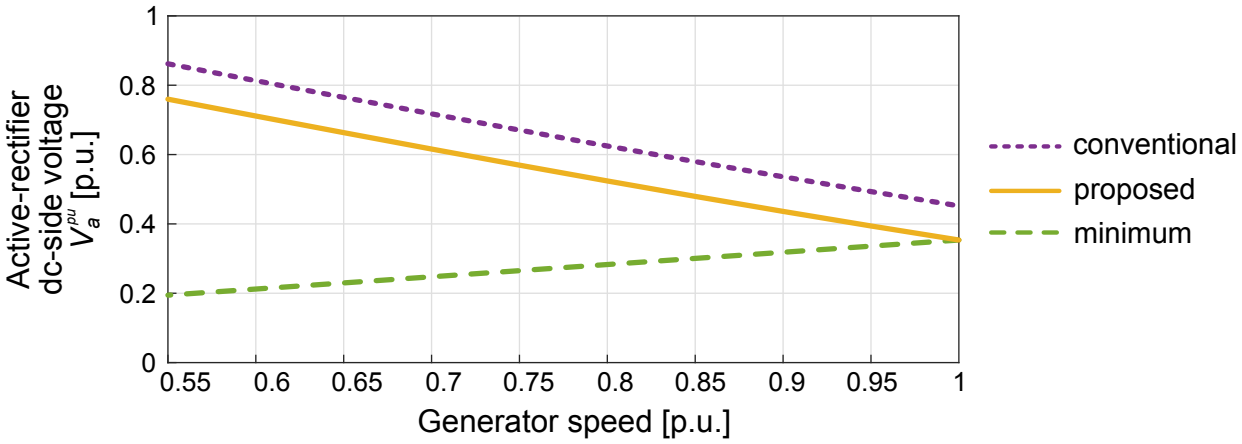


Figure 3.3: Comparison between the active-rectifier dc-side voltage with conventional dc-bus voltage (dotted-purple line) and with reduced dc-bus voltage (solid-yellow line) for a four-port system with $X_L^{pu} = 0.1$. In both cases, the active rectifier dc-side voltage is always higher than the minimum required value (dashed-green line).

Due to the series connection, a lower dc-side voltage means the active rectifier needs to process a smaller amount of power. Consequently, the peak ac-side current is reduced across the whole operating speed range. For example, Fig. 3.4 compares active-rectifier peak ac side current for three different cases. When X_L^{pu} is considered, the dc-output voltage of the passive rectifier drops due to commutation effect [47]. As the dc-bus voltage remains constant, the active rectifier must increases its dc-side voltage to make up for the loss. Consequently, the amount of power processed by the active rectifier increases. The peak ac-side current rises according to meet the power demand: the current shown by the dotted-purple line is higher than the dashed-red line. A reduction in the dc-bus voltage leads to a smaller amount of power delivered by the active rectifier. Following the same logic, the peak ac-side current is reduced, as shown by the solid-yellow curve.

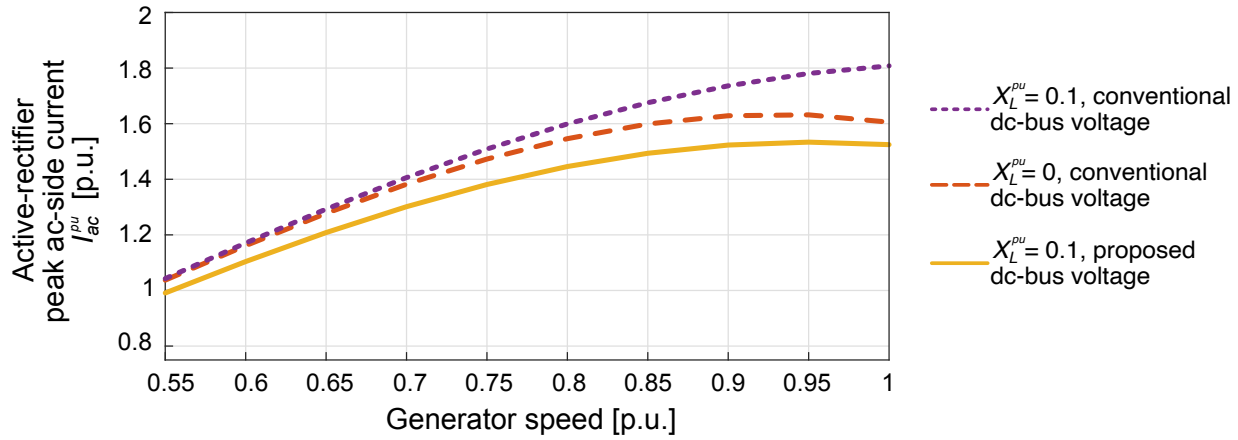


Figure 3.4: Peak ac-side current of the active rectifier versus generator speed for a four-port PMSG considering three scenarios (i) conventional dc-bus voltage with X_L^{pu} neglected (dashed-red line), (ii) conventional dc-bus voltage with $X_L^{pu} = 0.1$ (dotted-purple line), and (iii) proposed dc-bus voltage with $X_L^{pu} = 0.1$ (solid-yellow line).

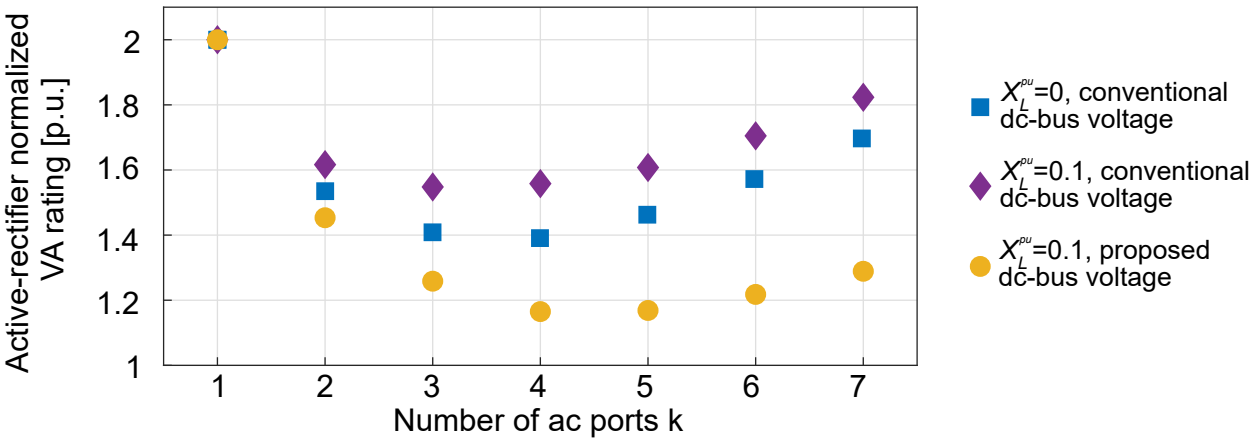


Figure 3.5: Using the proposed dc-bus voltage value leads to reduction in the active-rectifier VA rating.

Reduction in voltage and current rating leads to lower VA rating for the active rectifier, as illustrated in Fig. 3.5. When the dc-bus voltage is maintained at the conventional value and the per-unit inductance is considered, the VA rating increases, as shown by the diamond-purple line versus square-blue dots. A reduction in the dc-bus voltage using equation (3.6) leads to the active-rectifier VA rating reduction, as shown by the circle-yellow dots.

3.3.1 Optimal design considering the X_L^{pu} effects

The design goal is minimizing the active-rectifier VA rating through selection of an appropriate number of PMSG ac ports. Given a PMSG characterized by an X_L^{pu} value, the dc-bus voltage is calculated using (3.6) for each number of ac ports. The VA rating is determined as the product of by the voltage rating and the current rating. While voltage rating is set by the minimum generator speed, current rating is load-profile dependent. Section 2.2 provides a framework for the VA rating calculation. Output of the process is an optimum number of ac ports for each X_L^{pu}. For example, Fig. 3.6 illustrates the relationship between X_L^{pu} and the optimal number of ac ports for a wind-load profile [12]. The corresponding VA rating for each optimal design is shown in Fig. 3.7. A higher X_L^{pu} leads to a lower active-rectifier VA rating, however would increase power mismatch between the ac-port powering the active rectifier and the ac port powering the passive rectifier.

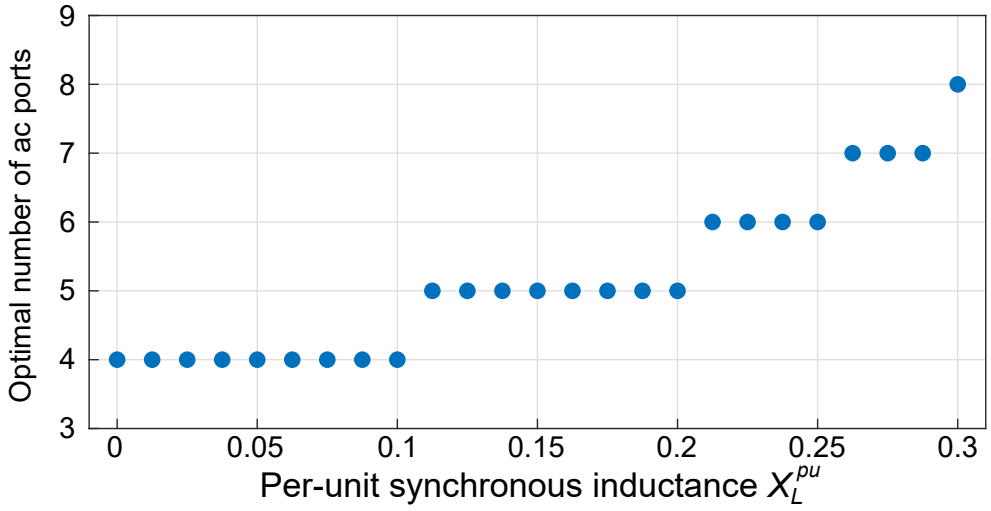


Figure 3.6: Dependency between the optimal number of ac ports and per-unit synchronous inductance considering a wind-turbine load profile.

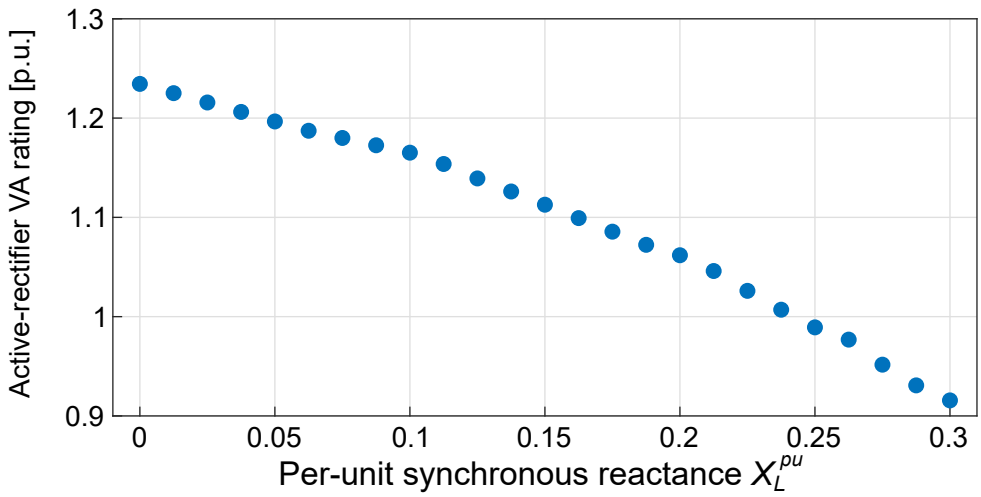


Figure 3.7: A higher per-unit synchronous inductance leads to a lower active-rectifier VA rating.

The power mismatch ac ports powering the passive rectifier and the active rectifier is understood by comparing the corresponding dc-side voltages. The current flowing through the dc-side of all the rectifiers are the same due to the serial connection. Consequently, the amount of power output is proportional to the dc voltage. Each passive rectifier provides $\frac{1}{k-1}$ the amount of voltage given by equation (3.1). The active rectifier provides the difference between the dc-bus voltage, given by equation (3.6), and the total passive-rectifier dc voltage. The power mismatch ratio, defined as the ratio between the amount of power delivered through a passive versus the active rectifier is

$$\kappa(\omega) = \frac{P_{passive}}{P_a} = \frac{V_p(\omega)}{(k-1)(V_{dc} - V_p(\omega))}. \tag{3.7}$$

The power mismatch ratio is not only a function of the number of ac ports, of the generator speed, but also of the per-unit synchronous inductance due to the dependency of V_p and V_{dc} on this parameter. The ratio is critical at the rated generator speed because the system delivers the highest amount of power at this condition. Figure 3.8 illustrates the ratio for the optimal designs given in Fig. 3.6. A higher X_L^{pu} reduces the power ratio, meaning each ac port powering the passive rectifier delivers a lower amount of power compared to the active-rectifier counterpart. At best, the ratio is 0.954, corresponding to $X_L^{pu} = 0$.

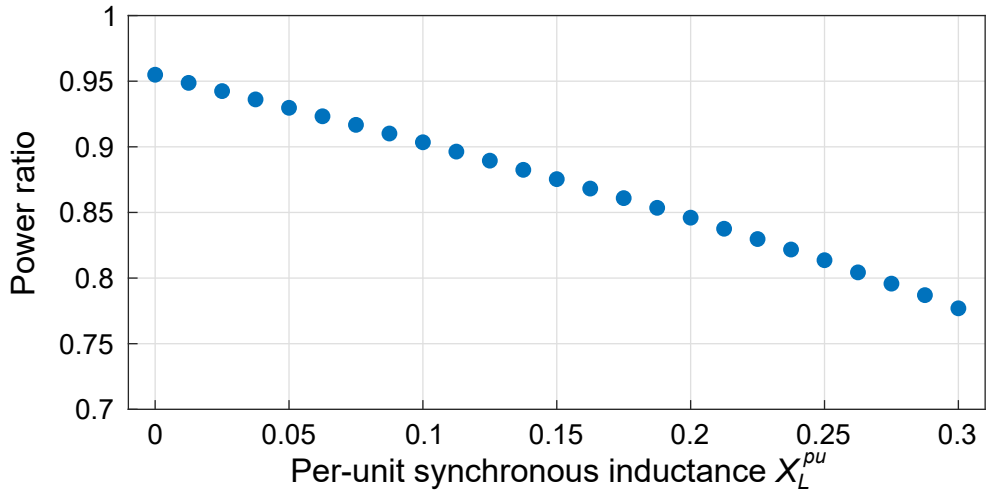


Figure 3.8: The power ratio decreases as the per-unit synchronous inductance increases, meaning a higher X_L^{pu} makes the ac port powering passive rectifiers deliver a lower amount of power compared to the ac ports powering the active-rectifier.

Figures 3.7 and 3.8 shows two opposite effects of X_L^{pu}. On one hand, a high X_L^{pu} value reduces the active-rectifier VA rating, which strongly correlates to the converter size. On the other hand, an increased in X_L^{pu} also reduce the power mismatch ratio, which potentially increases the generator size in order to deliver the rated amount of power. Selection of an optimal X_L^{pu} for an optimal system size requires knowledge on the generator design, and hence not within the scope of this dissertation. Nevertheless, an important trade off involving the per-unit synchronous inductance has been pointed out.

3.4 Conversion efficiency considering effects of a lowered dc-bus voltage

A high conversion efficiency is the goal of this dissertation. Therefore, understanding the effects of a lowered dc-bus voltage on the overall conversion efficiency is essential. Different from Chapter 2, the conversion losses presented here is calculated based on the simulated voltage and current waveforms across the power electronics switches. Simulation results are illustrated based on a 10 MW wind-energy conversion system using a PMSG with $X_L^{pu} = 0.1$.

3.4.1 Conversion loss calculation

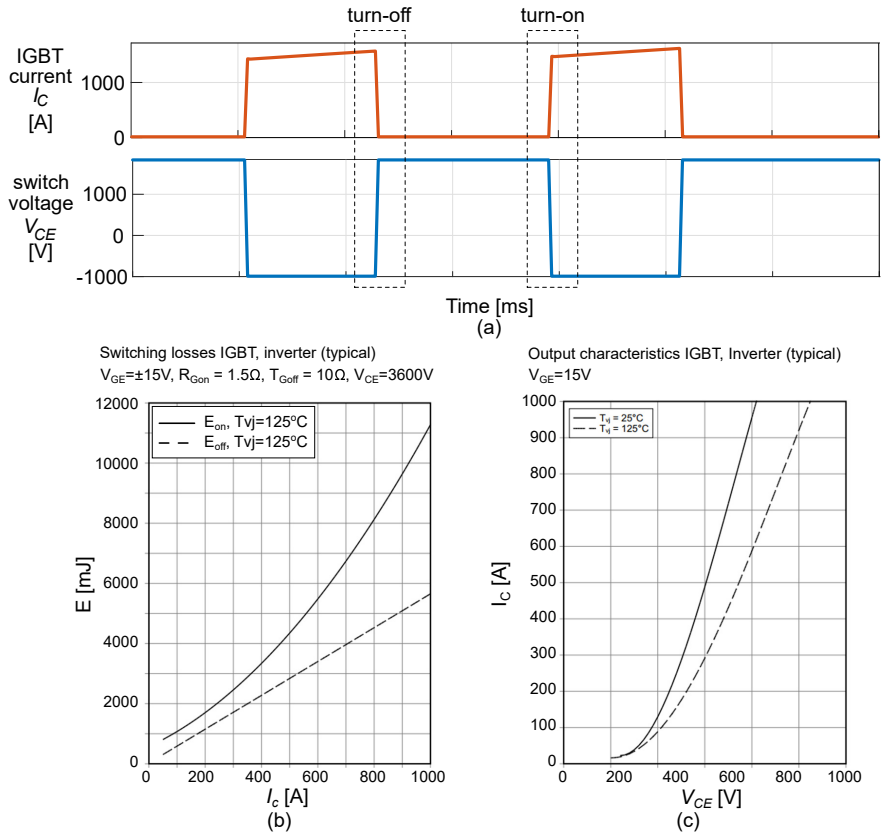


Figure 3.9: Information for loss calculation on the IGBT: (a) voltage and current waveform, (b) switching losses (turn-on and turn-off) versus conduction current graph, and (c) collector-emitter versus conduction current graph [31].

IGBT losses involve switching loss and conduction loss. Switching loss happens during the turn-on and turn-off instances because neither V_{CE} nor I_{sw} can change the value instantaneously. Zoomed in waveforms of IGBT voltage and current are shown in Fig. 3.9(a). At each turn-on and turn-off instance, the current and the switch voltage are recorded. Based on the current, the amount of energy dissipated in the turning on/off event is evaluated using the graph in Fig. 3.9(b). Data in the graph are given with $V_{CE} = 3600$ V, which might be different from the voltage at the transition instances of the IGBT. Linear scaling is used to evaluate the loss at the recorded V_{CE}. The switching loss power, denoted by $P_{igbt}^{switching}$ is calculated by the average switching-loss energy during one electrical period. The conduction loss can be calculated using the current waveform in Fig. 3.9(a) and the graph in Fig. 3.9(c). For each current level, the forward voltage V_{CE} is

evaluated. The product of the current and V_{CE} gives the instantaneous power loss due to conduction on the IGBT. The average value during one electrical period is the IGBT conduction loss, denoted as P_{igbt}^{cond}.

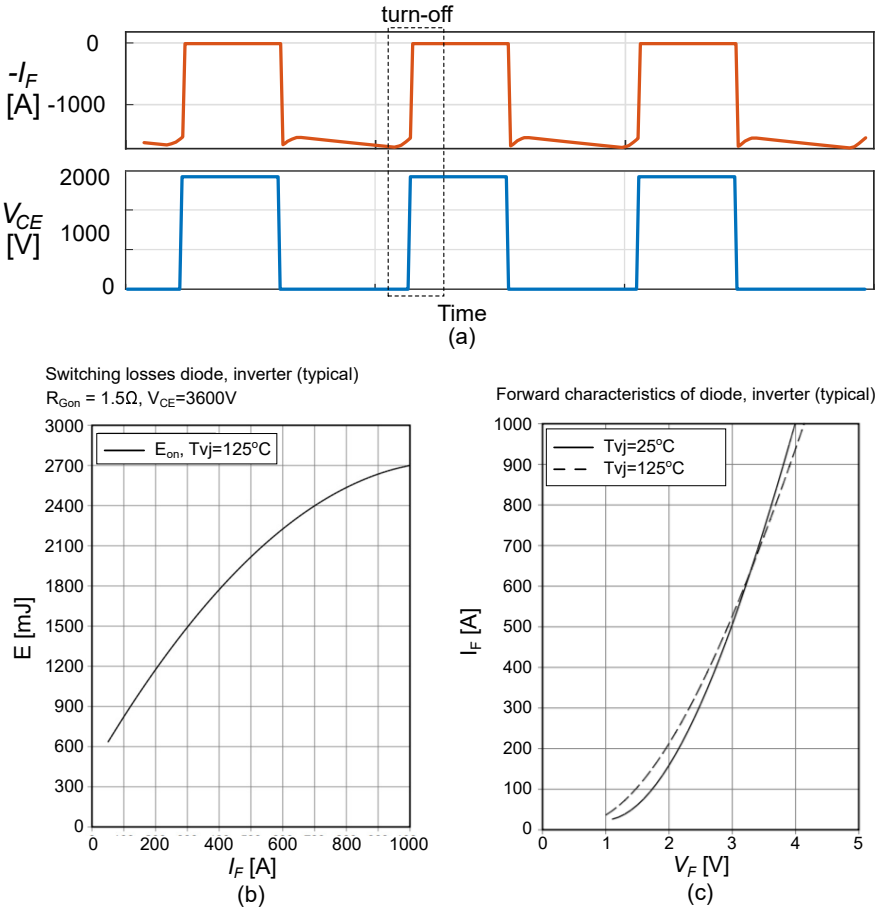


Figure 3.10: Information for loss calculation on the free-wheel diode: (a) voltage and current waveform, (b) reverse-recovery loss versus conduction current graph, and (c) forward voltage versus conduction current graph [31].

Losses on the free-wheel diode includes reverse-recovery (switching) loss and conduction loss. Reverse recovery happens during the turning-off event, identified by a transition of the current from a non-zero to zero value, as shown in Fig. 3.10(a). The current amplitude at the transition is used to estimate the energy loss using 3.10(a). The energy loss is scaled linearly with the collector-emitter voltage during the diode turn-off period to calculate the reverse recovery loss. Average loss in one electrical period is the reverse-recovery power loss, denoted by P_{diode}^{rr}. The current shown in Fig. 3.10(a) is used to calculate the conduction loss using the graph in Fig. 3.10(b). Average

energy loss in one electrical period is the conduction power loss on the free-wheel diode, denoted by P_{diode}^{cond}.

The total losses on the active rectifier are the sum of the losses on all the IGBTs

$$P_{loss}^{active} = \sum_{\text{all IGBTs}} \left(P_{igbt}^{switching} + P_{igbt}^{cond} + P_{diode}^{rr} + P_{diode}^{cond} \right). \tag{3.8}$$

Conduction is the only loss mechanism on the passive rectifiers. For each passive rectifier, two diodes always conduct to connect the ac side to the dc side. Current flowing cross each diode is the dc-side current. Assuming there are N passive rectifiers in the system, the total losses on the passive rectifiers are

$$P_{loss}^{passive} = N \times 2 \times V_F \times I_{dc} \tag{3.9}$$

The total losses on the power electronics converter are

$$P_{loss} = P_{loss}^{passive} + P_{loss}^{active} \tag{3.10}$$

3.4.2 Illustration example

A Simulink model , as shown in Fig. 3.11, is created to evaluate the conversion losses on the active rectifier. The active rectifier is a two-level converter driven by space-vector-modulation PWM. Two current controllers are created to regulate the d-axis and q-axis current of the ac port. Details on the current controller will be presented in Chapter 4 and Chapter 5. While the q-axis current is kept at zero for a unity power-factor operation, the d-axis current is calculated such that 10 MW of rated power is delivered to the dc bus.

The first step in calculation is determination of the physical voltage values. The voltage value is determined by the voltage rating of switches used in the active rectifier and the converter topology. The active rectifier provides the highest amount of dc-side voltage at the minimum generator speed. The physical voltage handled by the active rectifier at this point corresponds to the per-unit value

given by equation (3.3). Knowing a pair of physical value and per-unit value allows calculation of base voltage V_{base}. Having V_{base} and P_{base}, conversion of all quantities from per-unit to physical unit is possible. For example, consider a four-port PMSG with X_L^{pu} of 0.1, operating in the speed range from 0.55 to 1, and delivering 10 MW of power to the dc-bus at the rated power. The active rectifier is two-level and utilizes 6.5 kV IGBTs. Equation (3.6) results in a dc-bus voltage of

$$V_{dc} = 1.3118 \tag{3.11}$$

Using equation (3.3), the active-rectifier dc-side voltage at the minimum generator speed is

$$V_a^{pu}(\omega = 0.55) = 0.7597, \tag{3.12}$$

which is the active-rectifier rated voltage. Assuming the maximum voltage on each switch is half of the rated value, a two-level converter can provide a dc-bus voltage at maximum of half the switch rated voltage. Using 6.5 kV switches allows a rated voltage of 3.25 kV. The based voltage of the system is

$$V_{base} = \frac{V_{a,rated}}{V_{a,rated}^{pu}} = 4.28 \text{ kV}. \tag{3.13}$$

At a generator speed ω, the active-rectifier dc-side voltage $V_a(\omega)$ is determined by the product between V_{base} and V_a^{pu}, as given by (3.3). For a wind-turbine application, the dependency between the dc-bus power and the generator speed is

$$P_{dc}^{pu}(\omega) = \omega^3. \tag{3.14}$$

The back emf of the active-rectifier ac port is

$$E(\omega) = \omega \frac{V_{base}\sqrt{2}}{\sqrt{3}}. \tag{3.15}$$

Power balance between the ac and the dc side of the active rectifier allows determination of the

d-axis current

$$\frac{3}{2}I_{sd}E(\omega) = V_a(\omega)\frac{P_{base}P_{dc}^{pu}(\omega)}{V_{dc}^{pu}V_{base}}. \tag{3.16}$$

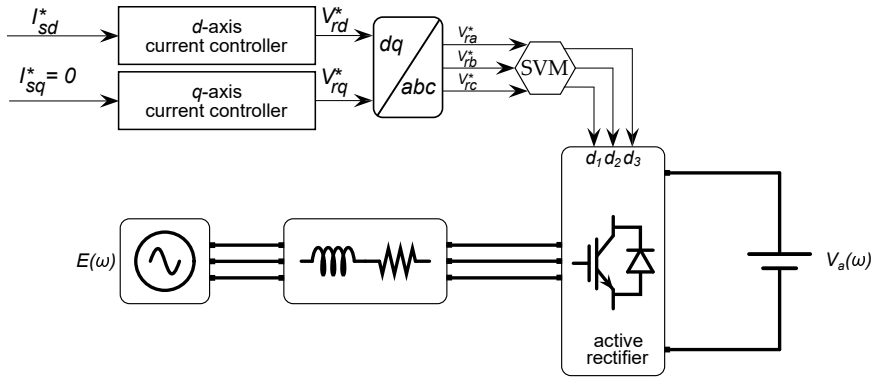


Figure 3.11: Lowering the dc-bus voltage reduces the overall conversion losses.

Conversion losses are compared in Fig. 3.12 between two four-port PMSG systems with $X_L^{pu} = 0.1$ delivering 10 MW power to the dc-bus. One system has the conventional dc-bus voltage and the other utilizes the proposed value calculate by equation (3.6). At the rated generator speed, the conversion losses has reduced from 1.3% to 0.89%. A similar trend is observed across the whole generator speed range. Reduction in the conversion losses is due to a lowered active-rectifier dc-side voltage, which help lowering the switching losses.

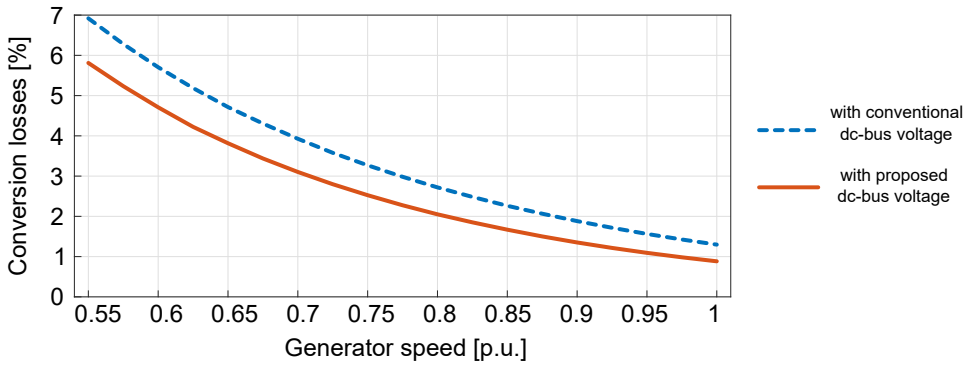


Figure 3.12: Lowering the dc-bus voltage reduces the overall conversion losses.

3.5 Conclusions

This chapter has discussed a design choice for the dc-bus voltage of an integrated generator-rectifier system. Conventionally, the dc-bus is maintained as the peak line-to-line total generator back emf to keep the active rectifier controllable at all the generator speed. Such a dc-bus voltage leads to increased active rectifier VA rating when the synchronous reactance is considered in a multi-port PMSG case. A method to calculate the dc-bus voltage is proposed by recognizing that the dc-bus voltage can be reduced without losing controllability of the active rectifier. The reduced dc-bus voltage results in a significant reduction of the active rectifier voltage, current, and consequently the VA rating.

To this point, the integrated generator-rectifier has been discussed in an average sense, i.e., all the voltage and current equations consider the average value. Due to the diode bridge operation, a voltage ripple always exists at the passive-rectifier dc output. This component is required to be small for high-quality dc power. Chapter 4 discusses techniques used for voltage ripple minimization.

Chapter 4

DC-BUS RIPPLE CORRECTION AND VOLTAGE REGULATION USING THE ACTIVE RECTIFIER

Creating a low-voltage-ripple dc bus and achieving a high power factor at the passive rectifiers are desirable for delivering high-quality power while minimizing the generator size. The low voltage-ripple requirement is accomplished conventionally with bulky filter capacitors connected to passive rectifiers, as shown in Fig. 4.1. However, these filters compromise the ac-side power factor. Without compromising the dc-bus voltage quality, the filter capacitor could be eliminated by introducing appropriate phase shifts between different ac ports connected to the passive rectifiers [39]. However, this approach requires either a specially-designed generator winding layout [6, 29] or by using multiple machines [48].

In contrast, this chapter focuses on using the series-connected active rectifier to compensate for the ripple created by the passive rectifiers. A control scheme is proposed that allows both the ripple compensation and the overall dc-bus voltage regulation. The voltage ripple caused by the passive rectifier is partially canceled by using the active-rectifier to inject harmonics into the d-axis current. The original concept of ripple voltage compensation is discussed in [49]. This chapter extends the controller design by including effects of the generator synchronous inductance on the passive-rectifier dc-side voltage. A closed-loop controller is developed for active compensation. An experimental setup that emulates a multiport PMSG is created to illustrate the proposed method as well as the dc-bus voltage regulation.

The rest of this chapter discusses the control strategy. Section 4.1 provides details on the concept of active voltage-ripple compensation and develops a linear dynamic model used for controller design. Section 4.2 discusses a control architecture to achieve active ripple compensation and shows a controller example. An overall dc-bus voltage control architecture is discussed in Section 4.3. Simulation and experimental results to corroborate the approach are presented in Section 4.4.

Nomenclature

x time-domain variable

X average value/ dc component of x

$\tilde{x}$ small signal/ perturbation/ ac component of x

x^*/ X^* reference value of x/ X

$X(s)$ Laplace domain representation of x

4.1 Active voltage-ripple compensation using the active rectifier

This section first discusses the concept of active ripple voltage compensation. Fourier analysis of the ripple sequence shows the maximum reduction in the ripple factor is achieved by eliminating the first harmonic. Then, a linearized model for the integrated generator-rectifier system is developed. This model allows controller design based on the loop-shaping technique.

4.1.1 Concept of active ripple voltage compensation

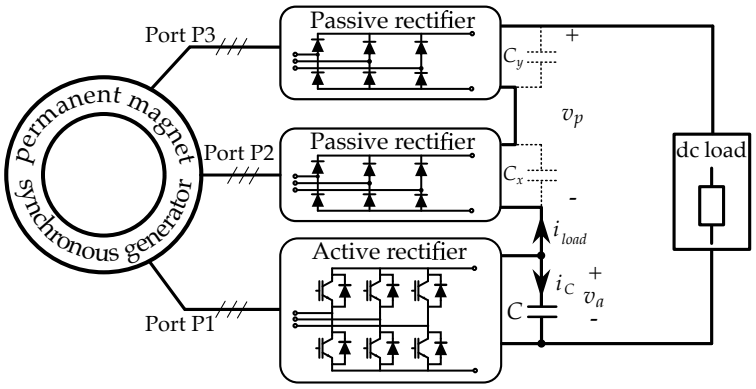


Figure 4.1: Integrated generator-rectifier system with one active-rectifier series connects with multiple passive rectifiers to create a regulated dc bus. The passive-rectifier dc voltage is filtered by capacitors. The active rectifier regulates the total dc-bus.

Active compensation allows removal of passive-rectifier filter capacitors C_x and C_y, marked by dotted lines in Fig. 4.1. The output voltage of the passive rectifier follows a profile depicted in Fig. 4.2(a) with E being the peak line-to-neutral back-emf of the ac port. This profile has a ripple component at six times the electrical fundamental frequency caused by the three-phase diode bridge operation. Mathematically,

$$v_p(t) = V_p + \sum_{k=1}^{\infty} V_{pk} \cos(6k\omega t + \phi_k) \tag{4.1}$$

where V_p is the average component, ω is the fundamental electrical frequency, V_{pk} and ϕ_k are the amplitude and the phase, respectively, of the sinusoidal ripple component at $6k\omega$.

The active rectifier generates a voltage ripple opposite the passive rectifier to create a low-voltage-ripple dc bus, as shown in Fig. 4.2(b). Mathematically,

$$v_a(t) = V_a - \sum_{k=1}^{N} V_{pk} \cos(6k\omega t + \phi_k) \tag{4.2}$$

where V_a is the average component and N is the highest harmonic order that can be synthesized by the active rectifier. Active compensation partially eliminates the voltage ripple and reduces the dc-bus voltage ripple factor.

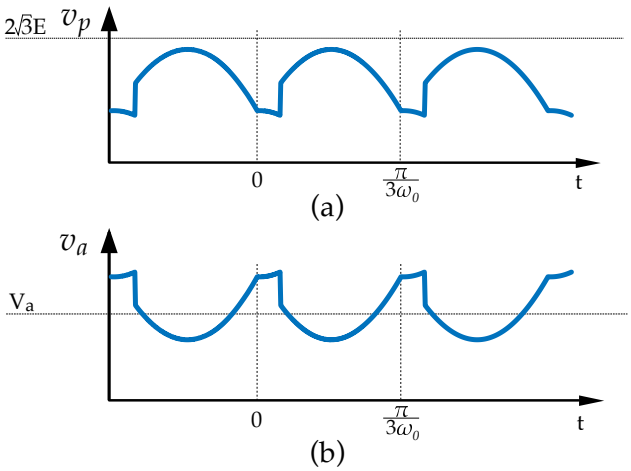


Figure 4.2: (a) Dc-output voltage of the passive rectifiers in the integrated generator-rectifier system. (b) Dc-side voltage of the active rectifier for ripple compensation.

Fig. 4.3 illustrates the effects of the active voltage-ripple compensation using a PMSG with

0.05 p.u. synchronous reactance and 0.007 p.u. phase resistance. The ripple factor is 2.8% without active compensation. This value drops to 1.2% when the ripple at six times the fundamental frequency is incorporated, corresponding to $N = 1$. Incorporating higher harmonics further reduces the ripple factor, but at a diminishing rate.

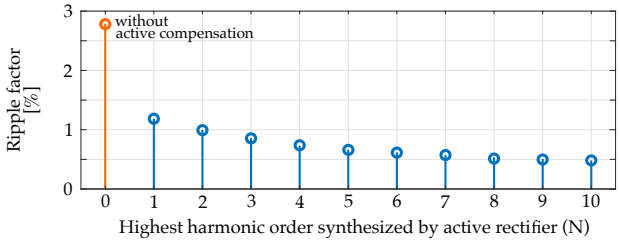


Figure 4.3: Ripple factor on the dc-bus voltage reduces as the highest harmonic order in the active rectifier dc-side voltage increases. The highest amount of reduction is achieved when the first harmonic is incorporated.

4.1.2 Active-rectifier ac-current dynamic model and control

The voltage ripple on the active-rectifier dc-side voltage is generated by precisely controlling the power drawn from the corresponding ac port, achieved through regulating the ac-side current. A dynamical model describing the interaction between the generator and the active rectifier is necessary to realize the control approach. This interaction is well approximated by a transfer function with one zero in the right-half plane and two poles in the left-half plane. The zero arises from the synchronous inductance while the poles are due to the filter capacitor and the current controller dynamics.

The ac port powering the active rectifier is modeled in the dq reference frame with the d-axis aligned to the generator peak phase-A back emf. The three-phase back emf d- and q- axis components are $e_{sd} = e$ and $e_{sq} = 0$, respectively, where e is the generator back emf (peak line-neutral). Two dynamic equations governing the active rectifier ac-side currents in the dq reference frame are

$$L\frac{di_{sd}}{dt} = -Ri_{sd} + \omega L i_{sq} + e - v_{rd}, \text{ and} \tag{4.3}$$

$$L\frac{di_{sq}}{dt} = -Ri_{sq} - \omega L i_{sd} - v_{rq}, \tag{4.4}$$

where v_{rd} and v_{rq} are the d-axis and q-axis voltages, respectively, created by the active rectifier.

The terms i_{sd} and i_{sq} are the d-axis and q-axis currents, respectively. L and R are the per-phase PMSG synchronous inductance and resistance, respectively.

A proportional-integral (PI) controller with feed-forward terms based on (4.3) to regulate the d-axis current is

$$v_{rd}^* = K_p(i_{sd}^* - i_{sd}) + \int K_i(i_{sd}^* - i_{sd})dt + e + \omega L i_{sq} \tag{4.5}$$

where i_{sd}^* is the reference current, v_{rd}^* is the active-rectifier d-axis voltage, and K_p and K_i are the proportional and integral gains, respectively. The d-axis current follows a first-order dynamics when the pole-zero cancellation tuning method is used [50]. In particular,

$$K_p = -\frac{L}{\tau} \text{ and} \tag{4.6}$$

$$K_i = -\frac{R}{\tau}, \tag{4.7}$$

where τ is a design choice. The d-axis current dynamics is

$$\tau\frac{di_{sd}}{dt} = -i_{sd} + i_{sd}^*. \tag{4.8}$$

This control strategy creates a left-half plane pole at frequency $\frac{1}{\tau}$. A similar control rule is applied for the q-axis current:

$$v_{rq}^* = K_p(i_{sq}^* - i_{sq}) + \int K_i(i_{sq}^* - i_{sq})dt - \omega L i_{sd}. \tag{4.9}$$

The q-axis current is typically maintained at zero for unity power-factor operation to minimize the current rating of the active rectifier.

4.1.3 Dynamic model of the active rectifier voltage

The active-rectifier dc-side voltage and the d-axis current are coupled by a power balance relationship between the ac and the dc sides at a given dc-bus current. The ac-side instantaneous power

is

$$p_{ac} = \frac{3}{2} e i_{sd} - \frac{3}{2} i_{sd}^2 R - \frac{3}{2} i_{sd} L \frac{di_{sd}}{dt}. \tag{4.10}$$

The q-axis current component i_{sq} does not contribute to the instantaneous power as it is kept at zero. The first and the second terms in the right-hand side of (4.10) show power drawn from the back-emf source and power loss on the phase resistance, respectively. The last term represents the synchronous inductance power, which is, conventionally, neglected. Inclusion of the last term is necessary in active compensation because the ripple voltage has a higher frequency than the back emf. The dc-side instantaneous power is

$$p_{dc} = v_a \left(C \frac{dv_a}{dt} + i_{load} \right), \tag{4.11}$$

where i_{load} is the current supplied to the dc bus, and C is the filter capacitor at the active rectifier, as shown in Fig. 4.1. The term $C \frac{dv_a}{dt}$ represents the current flowing into the filter capacitor. Equating (4.10) and (4.11) leads to

$$C v_a \frac{dv_a}{dt} = -v_a i_{load} + \frac{3}{2} e i_{sd} - \frac{3}{2} i_{sd}^2 R - \frac{3}{2} i_{sd} L \frac{di_{sd}}{dt}. \tag{4.12}$$

Equation (4.12) shows a non-linear relationship between the active-rectifier d-axis current and its dc-side voltage.

Analysis and controller design are carried out using a linearized system around an equilibrium point, assuming the voltage ripple is small relative to the average value. For any input I_{sd}, the system is at equilibrium when the state v_a takes the value

$$V_a = \frac{1}{I_{load}} \left(\frac{3}{2} E I_{sd} - \frac{3}{2} I_{sd}^2 R \right) \tag{4.13}$$

where E is the d-axis ac-port back emf at the the rated condition and I_{load} is the nominal value of the dc-bus current. At this equilibrium point, the input and the state satisfy the relationship:

$$-V_a I_{load} + \frac{3}{2} E I_{sd} - \frac{3}{2} I_{sd}^2 R = 0. \tag{4.14}$$

Considering perturbations $\tilde{i}_{sd}$ and $\tilde{v}_a$ around the equilibrium point implies $i_{sd} = I_{sd} + \tilde{i}_{sd}$ and $v_a = V_a + \tilde{v}_a$. Substituting these representations in equation (4.12) and using equation (4.14), the voltage ripple dynamic is

$$(C\tilde{v}_a + CV_a)\frac{d\tilde{v}_a}{dt} = -\tilde{v}_a I_{load} + \frac{3}{2}\tilde{i}_{sd}E - \frac{3}{2}\tilde{i}_{sd}^2 R - 3I_{sd}\tilde{i}_{sd}R - \frac{3}{2}(I_{sd} + \tilde{i}_{sd})L\frac{d\tilde{i}_{sd}}{dt} \tag{4.15}$$

The ripple voltage dynamic is non-linear due to the product between the state and its derivative, i.e., $\tilde{v}_a\frac{d\tilde{v}_a}{dt}$ and $\tilde{i}_{sd}\frac{d\tilde{i}_{sd}}{dt}$, and the quadratic term $\tilde{i}_{sd}^2$. Assuming $\tilde{v}_a \ll V_a$, $\tilde{i}_{sd}R \ll E$, and $\tilde{i}_{sd} \ll I_{sd}$, the non-linear equation (4.15) is approximated by a linear equation:

$$CV_a\frac{d\tilde{v}_a}{dt} = -\tilde{v}_a I_{load} + \left(\frac{3}{2}E - 3I_{sd}R\right)\tilde{i}_{sd} - \frac{3}{2}I_{sd}L\frac{d\tilde{i}_{sd}}{dt}. \tag{4.16}$$

The d-axis current dynamic follows a linear ordinary differential equation, as shown by (4.8). Thus, perturbation $\tilde{i}_{sd}$ and the large signal i_{sd} have the same governing equation, as given by (4.8):

$$\tau\frac{d\tilde{i}_{sd}}{dt} = -\tilde{i}_{sd} + \tilde{i}_{sd}^*. \tag{4.17}$$

Equations (4.16) and (4.17) constitute the dynamic model for the active-rectifier ripple voltage. The input is the reference d-axis current perturbation. The transfer function from input to output is expressed as

$$G(s) = \frac{V_a(s)}{I_{sd}^*(s)} = -\frac{3I_{sd}L}{2I_{load}}\frac{\left(s - \frac{E-2I_{sd}R}{I_{sd}L}\right)}{\left(\tau s + 1\right)\left(\frac{CV_a}{I_{load}}s + 1\right)}. \tag{4.18}$$

where $V_a(s)$ is the Laplace transform of the active-rectifier dc output voltage perturbation $\tilde{v}_a(t)$, and $I_{sd}^*(s)$ is the Laplace transform of the perturbation $\tilde{i}_{sd}^*(t)$ in the d-axis current reference value. This system has two poles in the left-half plane and one zero in the right-half plane. The first pole is at frequency $\frac{1}{\tau}$. Typically, τ is chosen to be between five and ten times the power electronics switching period. The second pole has frequency $\frac{I_{load}}{CV_a}$. Typical design choices place the second pole to the left of the first pole to ensure a low ripple voltage at the switching frequency. The right-half plane zero location depends on the generator parameters and the operating condition.

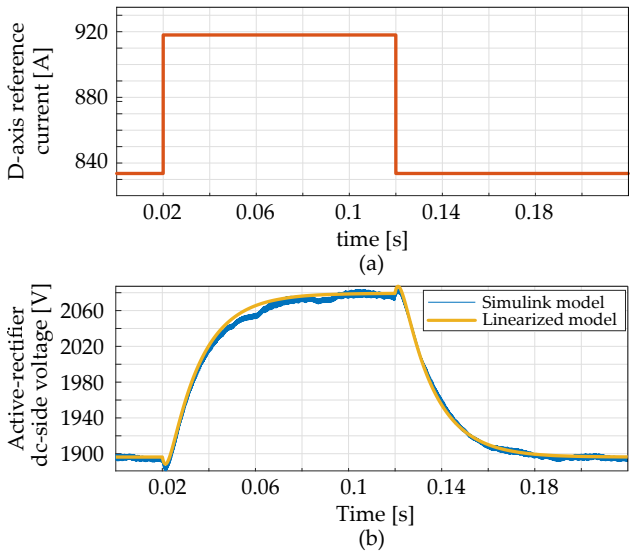


Figure 4.4: Verification of the linearized model. (a) Current command used for verification. (b) Subject to the current command, the linearized (4.18) and simulation model generate active rectifier voltage responses that match.

4.1.4 Linearized model verification

A MATLAB-Simulink model is created, following the diagram in Fig. 4.1, to verify the linearized dynamic of the active rectifier. The active rectifier is IGBT-based and switches at 2.5kHz, emulating a power converter at megawatt-power level [51]. Parameters for the ac ports are listed in Table 4.1. The selected inductance value corresponds to 0.05 p.u. reactance, typical for slotless PMSG [52]. Assuming each ac port has a line-to-neutral back emf of 952 V and the generator-rated power is 3 MW, the per-phase synchronous inductance is 2.2 mH. The per-phase equivalent resistance is 36.7 mΩ, assuming the per-unit resistance is 0.007. At the rated power condition, the d-axis current of the active-rectifier port is 843.6 A. The dc-bus voltage is maintained at 4.9 kV, the total peak line-to-line back emf of all the ac ports. The dc-bus current to deliver the rated power is 615 A. The filter capacitor is chosen such that the frequency of the second pole is seven times lower than the first pole, i.e., $C = 4.4$ mF. The linearized model has two poles at 500 rad/s and 71.4 rad/s, respectively, and a zero at 526 rad/s. Fig. 4.4 compares the active-rectifier dc-bus voltage waveforms when the d-axis current varies by 10% from the nominal value. The well-matched waveforms confirm the validity of the two-pole, one-zero model in (4.18). The second pole dominates the step response, as it has a much lower frequency compared to the first pole. The right-half

Table 4.1: Parameters used for verification

Parameter	Notation	Value	Unit
Power	P	3	MW
Rotor speed	ω_m	15	rpm
Number of poles	N_{pole}	40	
Electrical frequency	ω	5	Hz
Switching frequency	f_{sw}	2.5	kHz
Peak back emf (line-to-neutral)	E	952	V
Per-phase synchronous inductance	L	2.2	mH
Per-phase resistance	R	37	mΩ
Dc-bus voltage	V_{dc}	4.9	kV
Dc-bus current	I_{load}	615	A
Filter capacitance	C	4.4	mF
Active-rectifier nominal d-axis current	I_{sd}	844	A
Current-controller time constant	τ	2	ms

plane zero causes the initial response opposite to the command direction. This verification allows a controller design to actively compensate the voltage ripple by using linear system tools.

4.2 Voltage-ripple compensator architecture

This section discusses the control architecture used to perform active voltage-ripple compensation, as shown in Fig. 4.5. The ripple compensator comprises a lead-lag (LL) controller [53] and a proportional-resonant (PR) controller [54]. The LL controller is used to adjust the open-loop phase margin. The PR controller allows the voltage ripple to be tracked with zero-phase delay. Input to the ripple compensator is achieved by filtering the passive rectifier dc-output voltage. Only the ripple component at the target compensation frequency is allowed to pass through the reference voltage filter.

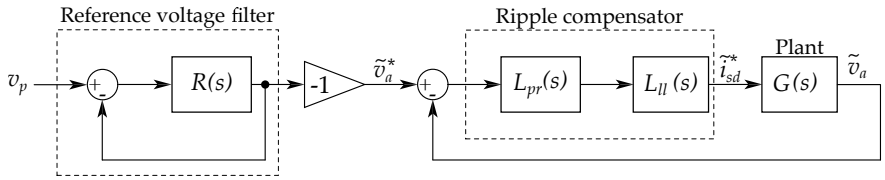


Figure 4.5: The proposed control architecture to modulate the active rectifier dc-side voltage for compensating the passive-rectifier voltage ripple.

4.2.1 Controller design

The controllers are designed to modify the plant dynamics such that the open-loop transfer function has a positive phase margin to ensure stability and high gain at the ripple-voltage frequency to achieve compensation. The modification is achieved by using an LL controller $L_{ll}(s)$ with the transfer function

$$L_{ll}^{c}(s) = \frac{K_{ll}}{\beta_{ll}} \frac{s + \frac{1}{T_{ll}}}{s + \frac{1}{\beta_{ll} T_{ll}}} \tag{4.19}$$

where K_{ll}, β_{ll}, and T_{ll} are the design parameters [53]. The next step is providing high gain at the ripple voltage frequency. This is accomplished by a PR L_{pr}^{c} in series with the LL controller:

$$L_{pr}^{c}(s) = K_{p}^{pr} + \frac{2K_{i}^{pr} w_{c}^{pr} s}{s^2 + 2w_{c}^{pr} s + (\omega^{pr})^2}, \tag{4.20}$$

where K_{p}^{pr}, K_{i}^{pr}, w_{c}^{pr}, and w^{pr} are the design parameters [54]. The frequency w_{c}^{pr} is set to the voltage-ripple frequency. Closing the control loop by feeding the error $\tilde{v}_a^* - \tilde{v}_a$ to input of the ripple compensator leads to a reference tracking with unity gain and zero phase delay.

The reference signal $\tilde{v}_a^*$ is set to negative of the passive-rectifier voltage ripple. The voltage ripple is achieved by filtering the passive-rectifier voltage v_p using the reference voltage filter block in Fig. 4.5 with

$$R(s) = \frac{2K_{i}^{pr} w_{c}^{pr} s}{s^2 + 2w_{c}^{pr} s + (\omega^{pr})^2}. \tag{4.21}$$

4.2.2 Design guidelines

The first step to design the voltage ripple compensator is the selection of the filter capacitance for a chosen switching frequency and a rated operating condition. The switching frequency sets the first pole of the transfer function from the d-axis current perturbation to the ripple voltage, as given by (4.18). The filter capacitance is chosen such that frequency of the second pole is five to ten times lower than the first pole under the rated operating condition.

The next step is to select the gains K_{ll}, β_{ll} and T_{ll} for the LL controller to achieve a desired phase margin greater than 30 degree for the loop gain $L_{ll}^{c}(s)G(s)$ [53]. The cross-over frequency of $L_{ll}^{c}(s)G(s)$ enforces the upper bound of the ripple frequency that can be compensated.

The last step is to select the gains K_{p}^{pr}, K_{i}^{pr}, ω_{c}^{pr}, and ω^{pr} for the PR controller such that the resonant peak is at the targeted ripple frequency [54].

4.2.3 Stability analysis of the linearized model for different operating conditions

The active voltage-ripple compensator designed following the guidelines in Section 4.2.2 is guaranteed to be stable at the rated load condition due to a positive phase margin. Stability needs to be analyzed at partial load condition and partial speed conditions. This analysis is done by evaluating the poles of the closed-loop transfer function from $\tilde{v}_a^*$ to $\tilde{v}_a$ in Fig. 4.1:

$$\begin{aligned} &F(s;\omega^{pu}, I_{load}, I_{sd}, V_a) \\ &= \frac{L_{ll}^{c}(s)L_{pr}^{c}(s;\omega^{pu})G(s;I_{load}, I_{sd}, V_a, \omega^{pu})}{1 + L_{ll}^{c}(s)L_{pr}^{c}(s;\omega^{pu})G(s;I_{load}, I_{sd}, V_a, \omega^{pu})}, \end{aligned} \tag{4.22}$$

where ω^{pu} is the per-unit generator speed. Parameters explicitly changed with the operating condition are added after each semicolon. For the PR controller, the resonant frequency is adapted to the generator speed by substituting ω_{c}^{pr} by $\omega^{pu}\omega_{c}^{pr}$. The plant transfer function is modified by replacing E with $\omega^{pu}E$. Assuming I_{load} is generator-speed dependent, V_a is calculated by

$$V_a = V_{dc} - n\frac{3}{\pi}\omega^{pu}E - n\frac{3}{\pi}\omega^{pu}\omega L I_{load}(\omega^{pu}) \tag{4.23}$$

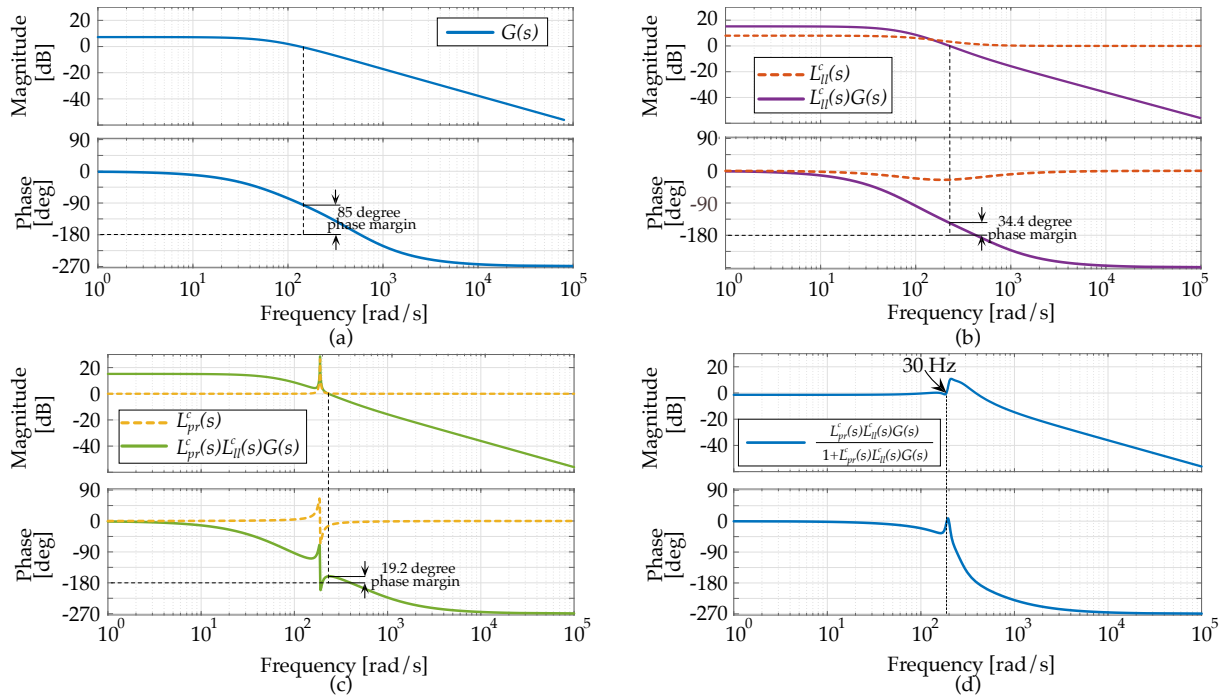


Figure 4.6: (a) Bode plot of the linearized plant. (b) An LL compensator (dashed-orange curves) modifies the cross-over frequency, leading to increased gain at low frequencies and a satisfactory phase margin (solid-purple curves). (c) PR controller (dashed-yellow curves) adds a resonant peak to the open-loop system (solid-green curves) without de-stabilizing the system. (d) The overall closed-loop system is stable and exhibits close-to-unity gain and close-to-zero phase at the ripple voltage frequency of 30 Hz.

where ω is the rated electrical frequency and n is the number of passive rectifiers. Neglecting the resistive losses, the d-axis current is calculated using the power balance equation

$$I_{sd} = \frac{2}{3}\frac{1}{\omega^{pu}E}V_a I_{load}. \tag{4.24}$$

A design example is given in Section 4.2.4. The switching frequency is assumed to be a typical value for a megawatt-scale system. The ripple frequency, line frequency and filter capacitor are calculated accordingly. Stability is analyzed under variable load and speed conditions assuming a wind-turbine operation.

Table 4.2: Controller parameters for the simulation system

	Parameter	Value	Unit
LL controller	K_{ll}	2.5	V/V
	β_{ll}	2.5	-
	T_{ll}	0.0033	s
PR controller	K_p^{pr}	1	A/V
	K_i^{pr}	20	A/V
	ω_c^{pr}	0.5	rad/s
	ω^{pr}	60π	rad/s

4.2.4 Design example

Fig. 4.6(a) shows the Bode plot of the plant with parameters from Table 4.1, as given by (4.18). The two poles are at 71.4 rad/s and 500 rad/s, respectively. The right-half plane zero is at 526 rad/s. The plant has a phase margin of 85 degrees and a zero-frequency gain of 0.35 dB. The first pole is recognized through a knee point and the transition of the phase angle from zero to -90 degrees at sub 100 rad/s frequencies. Involvement of one more pole and another zero is observed in the frequency range above 1000 rad/s: the Bode-plot magnitude decreases at a -20-dB/decade rate while the phase angle approaches -270 degrees.

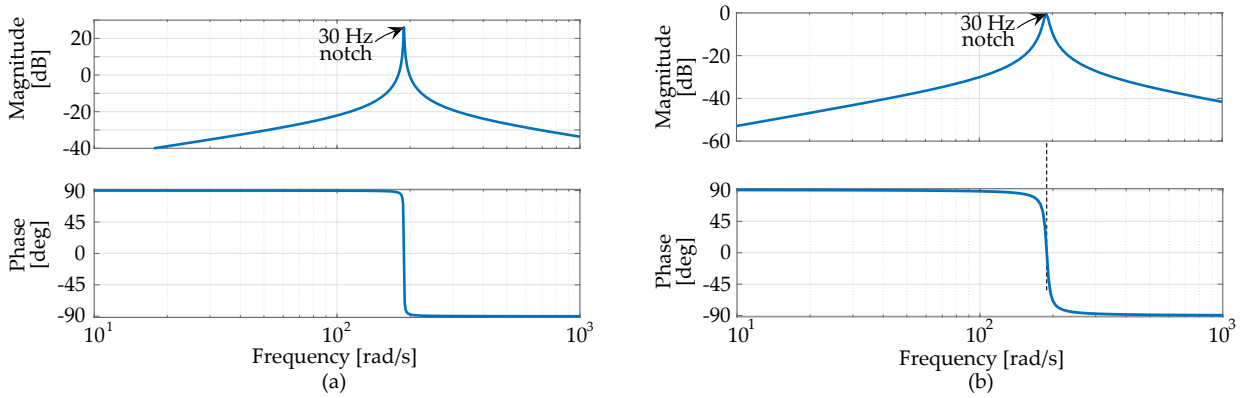


Figure 4.7: (a) Bode plot of the resonant filter $R(s)$ with a very high-gain peak at 30 Hz. (b) Wrapping a feedback loop around the resonant element results in the ripple extractor with the Bode plot showing a notch of unity gain and zero phase at the desired frequency of 30 Hz.

The open-loop gain should be high at low frequencies for a fast reference tracking. The LL controller is used to increase the gain while keeping the phase margin in the range of 30 degree. The controller gains are designed following [53] and summarized in Table 4.2. The Bode plot of

the LL controller is shown by the dotted-orange line and the total loop gain by the purple line in Fig. 4.6(b). The cross-over frequency moves to the right at 233 rad/s and the zero-frequency gain is 15.2 dB. The phase margin of 34.4 degrees ensures closed-loop stability. The maximum ripple frequency should be lower than the cross-over frequency of 233 rad/s, or 37 Hz. The target ripple frequency is chosen to be 30 Hz, corresponding to a fundamental frequency of 5 Hz. The selection is based on the electrical frequency of direct-drive wind turbines [55].

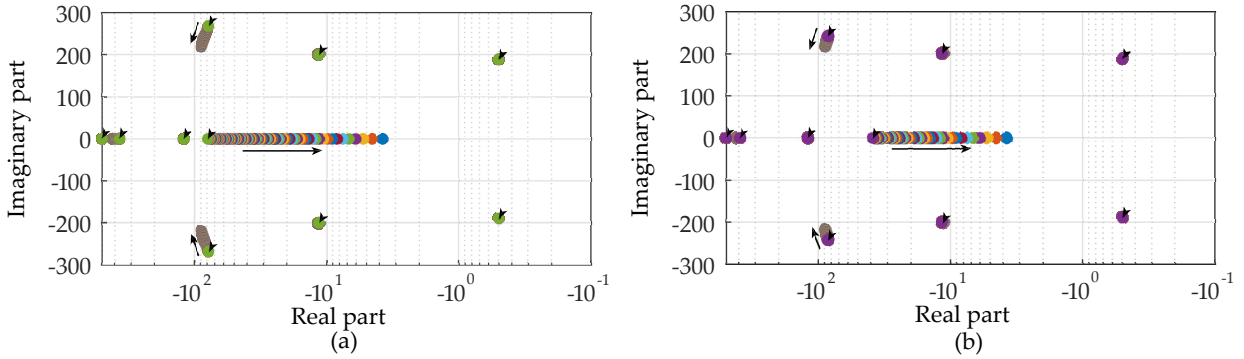


Figure 4.8: (a) The closed-loop transfer-function poles remain in the left-half plane under varying load conditions. The V-shape markers indicate the roots at rated load. The arrows show the root moving directions when the load reduces. (b) Similar observation for the variable speed conditions. The arrows show the root moving directions when the speed reduces.

A PR controller with parameters shown in Table 4.2 is used to modify the open-loop gain at 30 Hz. The Bode plot of L_{pr}^{c} is shown by the dashed-yellow curve in Fig. 4.6(c). The total open-loop gain, shown by the solid-green line, has a peak of approximately 30 dB at 30 Hz and a phase margin of 19.2 degree. The closed-loop system is stable and has close-to-unity gain with close-to-zero phase at 30 Hz, as shown in Fig. 4.6(d).

The reference ripple voltage is generated by filtering the dc-output V_p of the passive rectifier using the resonant part of the controller in (4.20). Fig. 4.7(a) shows the Bode plot of the resonant element $R(s)$ using parameters from Table 4.2. This plot has a high-amplitude notch at 30 Hz. Adding a feedback loop around the resonant element results in the reference voltage filter, which has unity gain and zero phase delay at 30 Hz and low gain at other frequencies, as shown in Fig. 4.7(b). This characteristic ensures voltage ripple only at 30 Hz from the input passed to the ripple compensator.

Fig. 4.8 shows stability of the example system by evaluating the poles of the closed-loop system

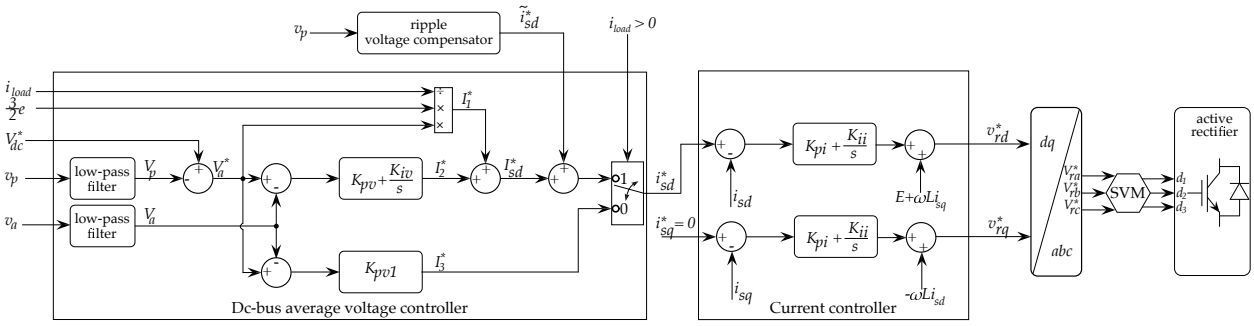


Figure 4.9: Overall control architecture for dc-bus voltage regulation and active voltage-ripple compensation.

given by (4.22) for variable-load and variable-speed conditions. First, the dc-load current is varied from 5% to 100% of the rated amount while the generator speed is kept at the rated value. Locus of the poles is shown in Fig. 4.8(a). For all the loading conditions, the roots remains in the left-half plane, implying controller stability. Second, the generator speed is varied between 0.55 pu and 1 pu. The load current is selected to be proportional to the cube of the per-unit generator speed to emulate operation of a wind turbine [12, 39, 43]. Similar to results of the first test, all the poles remain in the left-half plane, as show in Fig. 4.8(b).

4.3 Overall dc-bus voltage controller architecture

In addition to ripple compensation, the dc-bus voltage must be regulated in practical applications. An overall control architecture to achieve both goals is shown in Fig. 4.9. The voltage ripple compensator, shown in Fig. 4.5, is a part of this overall control architecture. The rest of the architecture is used to regulate the average dc-bus voltage.

4.3.1 Average dc-bus voltage controller

The dc-bus average voltage controller takes the passive-rectifier and active-rectifier dc-side voltages, the load current, the ac-port peak back emf, and the reference dc-bus voltage as inputs. It generates the d-axis current command to meet the amount of power required by the dc load while maintaining the dc-bus voltage at the reference value V_{dc}^*. The active-rectifier average dc-side voltage V_a^* is set to equal the voltage difference between the reference dc-bus V_{dc}^* and the average

dc-side V_p:

$$V_a^* = V_{dc}^* - V_p. \tag{4.25}$$

Low-pass filters are applied to the instantaneous v_a and v_p measurements to extract the average components. The output I_{sd}^* of the dc-bus average voltage controller includes a feed-forward term and an output of a PI controller. The feed-forward term I_1^* helps achieve a fast dynamic response. It is calculated based on an ideal power-balance relationship of the active rectifier, neglecting conversion losses and effects of the phase resistance:

$$I_1^* = \frac{V_a^* I_{load}}{\frac{3}{2}E}. \tag{4.26}$$

In practice, conversion losses always exist. Simply using the feed-forward term does not set the average voltage on the active-rectifier dc-side to V_a^*. A PI controller generates a correction term I_2^* based on the voltage mismatch. The integral term ensures a zero steady-state error. The overall control law for the average d-axis current component is

$$I_{sd}^* = I_1^* + K_{pv}(V_a^* - V_a) + \int K_{iv}(V_a^* - V_a)dt \tag{4.27}$$

where K_{pv} and K_{iv} are the proportional and integral gains. The gains are tuned by a pole-placement technique [35].

Under a zero dc-load condition, the integral term leads to oscillatory behavior of the dc-bus voltage. A proportional (P) controller is used for regulation. Output of the average voltage controller is

$$I_3^* = K_{pv1}(V_a^* - V_a) \tag{4.28}$$

where K_{pv1} is the proportional gain, which is selected to be a fraction of K_{pv}.

A signal multiplexer is added at the controller output to select the PI controller with feedforward term, or the P controller. If I_{load} is greater than zero, output of the PI controller is designated as the d-axis current command. Otherwise, output of the P controller is selected. The ripple voltage

compensator is deactivated to avoid power circulation in the active-rectifier ac port for a zero-load condition.

4.3.2 Additional design considerations

Dc-bus voltage and the active-rectifier filter-capacitor size are critical. A sufficiently high dc-bus voltage is required to keep the active rectifier controllable. However, a high dc-bus voltage necessitates an over-sized active rectifier and compromises the conversion efficiency. Filter capacitor size is crucial. Too low of value causes excessive dc voltage ripple at the switching frequency. Too high a value reduces the plant cross-over frequency, which in turn limits the maximum voltage ripple that can be compensated.

Selection of the active-rectifier dc-side voltage

The active rectifier dc-side voltage must satisfy

$$v_{a,min} > \sqrt{3}E \tag{4.29}$$

due to space-vector modulation. The minimum value is expressed in terms of the average value V_{a0} of the active rectifier and the maximum voltage ripple $\tilde{v}_{p,max}$ of the passive rectifier:

$$v_{a,min} = V_a - \tilde{v}_{p,max} \tag{4.30}$$

The minimum value occurs when the ripple voltage of the passive rectifier stays at the maximum. Assuming there are n passive rectifiers, the maximum ripple voltage on the corresponding dc output is

$$\begin{aligned} \tilde{v}_{p,max} &= v_{p,max} - V_p \\ &= n\sqrt{3}\left(1 - \frac{3}{\pi}\right)E \end{aligned} \tag{4.31}$$

where $v_{p,max}$ is the maximum voltage on the dc-side of the passive rectifier. Substituting (4.31) into (4.30) and using the inequality (4.29), the requirement on the active-rectifier average component is

$$V_a > \sqrt{3}E + n\sqrt{3}\left(1 - \frac{3}{\pi}\right)E. \tag{4.32}$$

Considering the system in Fig. 4.1 with parameters given in Table 4.1, the minimum active-rectifier average dc-side voltage is $V_{a,min} = 1799$ V. This value is higher than the conventional requirement that the dc-side voltage must be at least 1650 V, the peak line-to-line back emf. The excess voltage is required to perform active voltage ripple compensation.

Selection of the dc-bus voltage

The dc-bus voltage is selected such that at all loading conditions the active-rectifier ac-side voltage never falls below the value determined in Section 4.3.2. Due to operation of the dc-bus average-voltage controller, the active-rectifier dc-side voltage average component V_a automatically decreases if V_p increases and vice versa, to keep the dc-bus voltage constant. The maximum value of V_p sets the minimum value of V_a. Assuming there are n passive rectifiers in the system, the maximum dc output voltage is

$$V_{p,max} = n\frac{3}{\pi}E\sqrt{3}. \tag{4.33}$$

The minimum dc-bus voltage is

$$V^*_{dc,min} = V_{p,max} + V_{a,min}. \tag{4.34}$$

Considering the example system, the maximum dc-side voltage of two passive rectifiers is $V_{p,max} = 3151$ V. The minimum dc-bus voltage becomes $V^*_{dc,min} = 4950$ V.

Filter-capacitor sizing

The capacitor sizing is dictated by two requirements: (i) location of the second pole, and (ii) ripple voltage at the switching frequency. Typically, the second pole should be far from the first pole. In this paper, the second pole is located at one-seventh the frequency of first pole. In addition, the capacitor should be sufficiently large to ensure a low ripple voltage at the switching frequency [49, 56].

4.4 Results

This section verifies the proposed method through simulation and experiment. The ripple factor is effectively reduced in a simulation three-port system with a 4.95-kV dc bus and 3-MW power. The simulation results first illustrate the active voltage ripple compensation at the rated loading condition. Then, the performance at partial load and partial generator speed is demonstrated. Experimental implementation further corroborates the active compensation strategy.

4.4.1 Simulation

A Simulink model following Fig. 4.1 is set up. Each ac port has the synchronous inductance and equivalent resistance values shown in Table 4.1. The active rectifier is a two-level converter switching at 2.5 kHz, representative for MW-scale power converters [1].

Fig. 4.10 illustrates waveforms in pre- and post-compensation, and Table 4.3 summarizes the key performance metrics. Before 0.2 s, a constant d-axis current results in sinusoidal phase currents and a fixed active-rectifier dc-side voltage. The ripple voltage caused by the passive rectifier appears at the dc bus, causing a 2.8% ripple factor. At 0.2 s, active compensation modulates the active-rectifier d-axis current and deforms the phase currents. The active rectifier dc-side voltage counteracts the voltage ripple on the passive rectifier. The ripple factor is 1.21%, a 67.5% reduction, and matches well with the values shown in Fig. 4.3. The output power of the ac port feeding the active rectifier is modulated to generate the voltage ripple, as shown in by Fig. 4.10(c). Consequently, the power output of the whole generator has higher ripple, as shown by the yellow

waveform. A high power ripple is due to functional substitution of the passive-rectifier filters C_x and C_y by the active rectifier. In wind-power applications, the generator ripple power does not cause an excessive rotor-speed oscillation due to a high rotor moment of inertia, as shown in Fig. 4.1(d). The inertia value used for illustration is $J = 12.6 \times 10^6$ kg.m^2 [57].

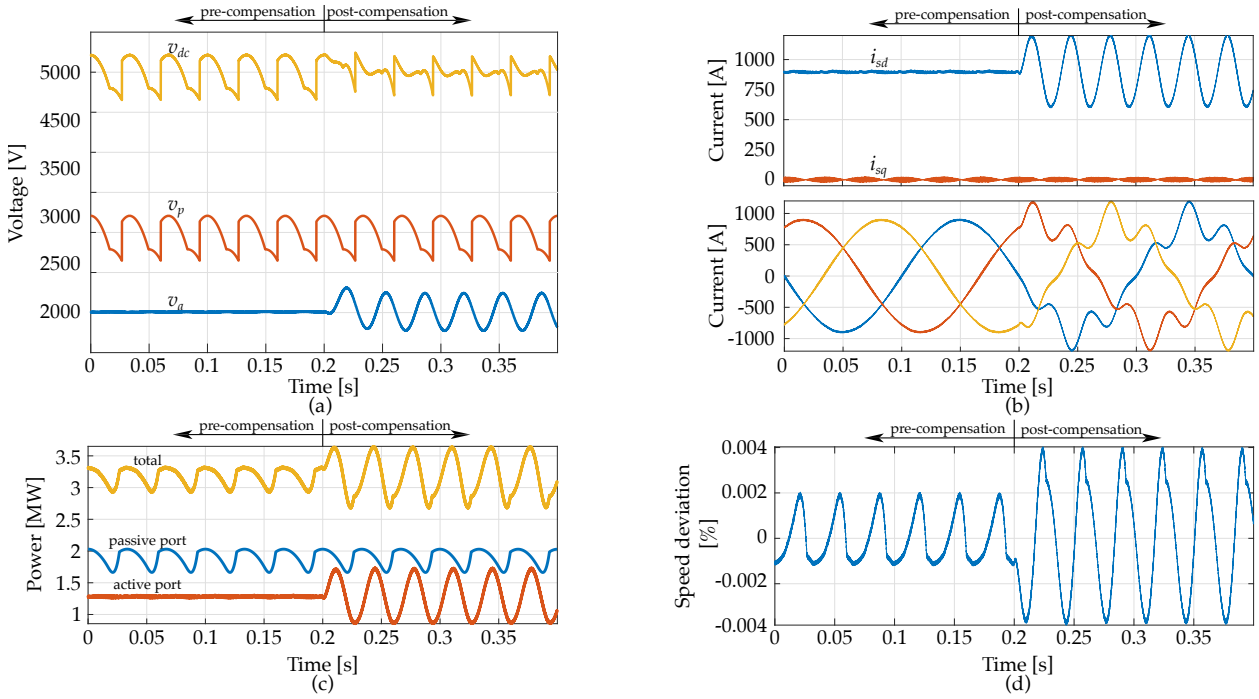


Figure 4.10: Simulation waveforms. (a) The dc-side voltage of the active rectifier (blue line) is modulated to counteract the passive rectifier voltage (orange line), leading to a reduced voltage-ripple dc bus (yellow line). (b) The d-axis and q-axis currents are maintained as constant values prior to compensation (top plot), leading to sinusoidal phase currents (bottom plot). At $t = 0.2$ second, the harmonic current is injected to the d-axis component, leading to deformation in the phase currents. (c) Power output of the ac ports feeding the passive rectifiers (blue), the active rectifier (red), and of the whole generator (yellow). (d) The power ripple causes speed oscillation, but at a very small percentage of the rated speed.

Table 4.3: Comparison between pre- and post-compensation

		Dc-bus voltage ripple factor	Active-rectifier ac-port power factor
Simulation	pre	2.8%	1
	post	1.2%	0.95
Experiment	pre	2.19%	0.99
	post	1.22%	0.95

Implementation of active voltage ripple compensation leads to a higher active-rectifier volt-ampere (VA) rating, *defined as the product of peak dc-side voltage and peak ac-side current*. This increase is illustrated using simulation results in Fig. 4.10. The pre-compensation period corresponds to a system without active compensation. The active-rectifier dc-side voltage and the peak ac-side current are 1958 V and 854 A, respectively, leading to a VA rating of 1.67 MVA. Implementation of the active voltage ripple compensation increases the ratings to 2174 V and 1161 A, respectively. The resultant VA rating is 2.52 MVA. Higher voltage- and current-rating active power electronics switches must be used compared to a system without active compensation. However, the bulky filter capacitors at passive rectifiers can be eliminated, leading to a significant reduction in system weight, as well as promising improvements in overall reliability.

Fig. 4.11 illustrates the operation of the proposed proposed control architecture, including start-up, shut-down, restart, and dc-load variation. Initially, the load current is zero, all the controllers are disabled. At time $t = 0.25$, the load current increases from zero to the rated value of 606 A. Both the dc-bus voltage controller and the active voltage ripple compensator are activated, leading to the dc-bus voltage being maintained at 4.95 kV. At 1 s, the load current changes to zero. The dc-bus voltage has an overshoot and then settles to the reference value due to the contribution of I_3^*. At 2.25 s, the load current increases again to the rated value. The ripple voltage compensator and the PI controller are activated, leading to a stable 4.95 kV dc-bus voltage. From time 3.5 s, the load current is stepped down to zero in five steps; each has an amplitude of 20% of the rated load current. Finally, the dc-bus current steps up to 40% of the rated value from zero. During the transition, the dc-bus voltage experiences transient behavior at the stepping instances and then stabilizes.

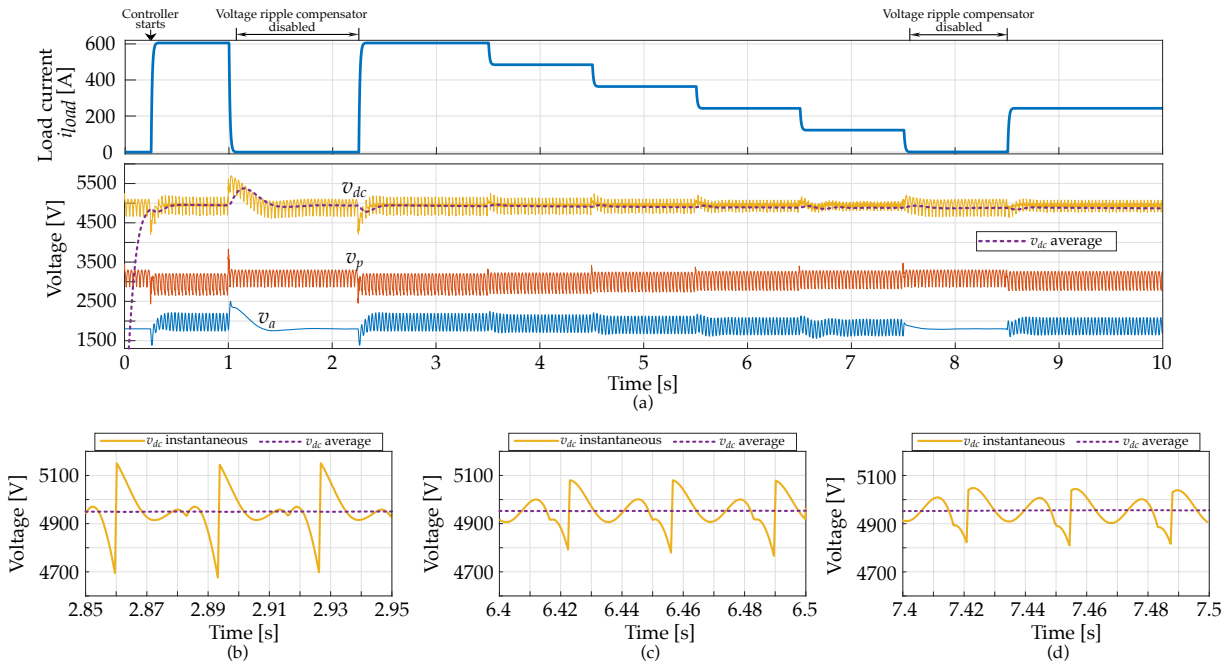


Figure 4.11: (a) The average dc-bus voltage controller regulates the dc-bus voltage when the load current is non zero. During the positive-load-current intervals, the ripple voltage caused by passive the passive rectifiers are actively compensated, leading to a low voltage-ripple dc-bus. (b, c, d) Zoomed-in voltage waveforms at different time intervals.

The active ripple voltage compensation and dc-bus voltage regulation are achieved at variable generator speeds. Assuming a linear relationship between back emf and generator speed, each ac port has a back emf of $E\omega^{pu}$ where ω^{pu} is the normalized generator speed. Fig. 4.12 illustrates the variable-speed operation while the dc-bus power is maintained at 3 MW. At time 1.75 s, the generator speed decreases to 0.8 p.u. The dc-side voltage of the passive rectifier V_p decreases accordingly. The voltage controller increases the active rectifier dc-side voltage to make up for the drop, maintaining the dc-bus voltage at the commanded value of 4.95 kV. At 1.75 s, the speed increases back to the rated value. Due to the increase in the passive rectifiers output, the active rectifier decreases the dc-side voltage. During the process, active voltage ripple compensation succeeds, as shown in Fig. 4.12(b).

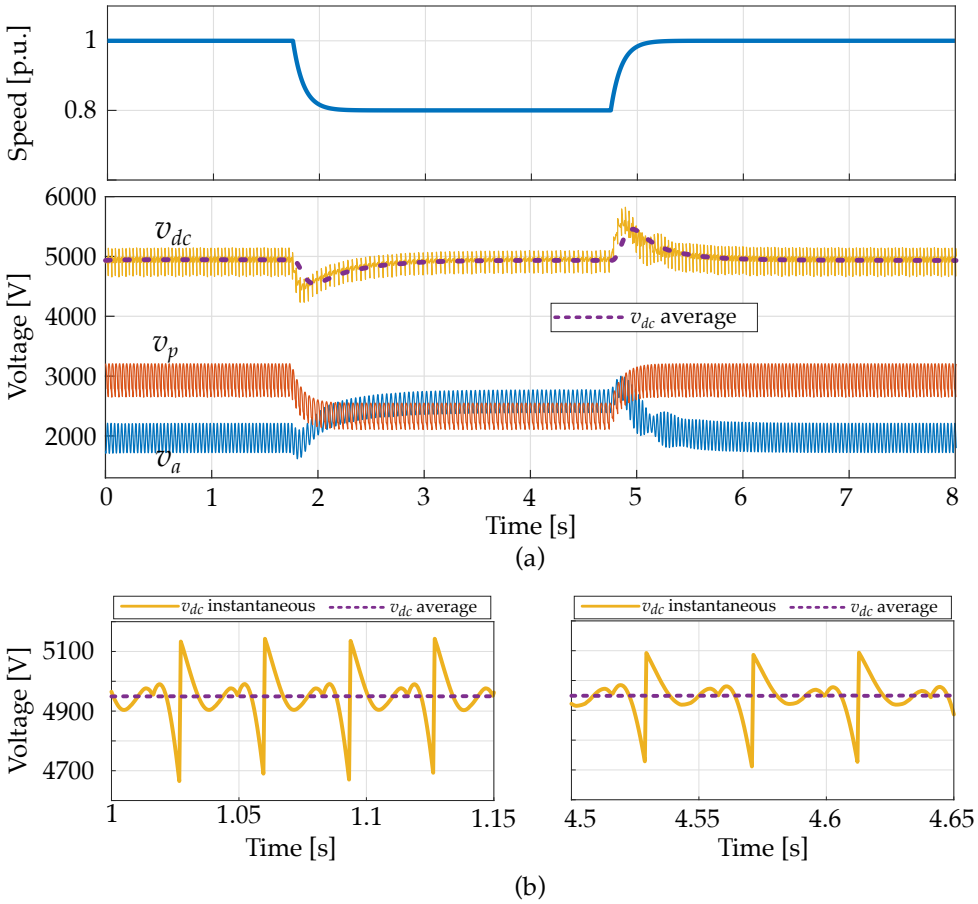


Figure 4.12: (a) When the generator speed varies, the active rectifier reacts to the voltage variation on the passive-rectifier output to maintain the dc-bus voltage constant. (b) During the transition and steady-state conditions, the voltage ripple is compensated. Refer to Fig. 4.10(a) for waveform of an uncompensated condition.

Table 4.4: Parameters of the experimental setup

Parameter	Notation	Value	Unit
Power	P	17.7	W
Rotor speed	ω_m	45	rpm
Number of poles	N_{pole}	48	
Electrical frequency	ω	18	Hz
Switching frequency	f_{sw}	10	kHz
Peak back emf (line-to-neutral)	E	18	V
Per-phase synchronous inductance	L	25	mH
Per-phase resistance	R	6	Ω
Dc-bus voltage	V_{dc}	93.5	kV
Dc-bus current	I_{load}	0.19	A
Filter capacitance	C	19	μF
Active-rectifier nominal d-axis current	I_{sd}	0.3	A
Current-controller time constant	τ	0.5	ms

4.4.2 Experimental Results

A laboratory set up is built, as shown in Fig. 4.13(I), to further validate the proposed strategy. The generator consists of three assemblies, named Port-1, Port-2, and Port-3. Port-1 powers an active rectifier while the other two feed passive rectifiers. Each port has 48 poles, a synchronous inductance of 25 mH, an equivalent series resistance of $6\ \Omega$, and a voltage constant of 0.4 V/rpm. Each generator assembly is rated for 1300 rpm, 700 watts, 5.5 A, and 310 V. The rectifier outputs are connected in series and deliver power to a resistive load.

The active rectifier switches at 10 kHz. The current controller is designed to have a time constant of 0.5 ms, corresponding to the first pole at 2000 rad/s. The target compensation frequency should not exceed half the first-pole frequency. The ripple frequency is chosen to be 680 rad/s, corresponding to a rotational speed of 45 rpm. The active rectifier ac-side peak current is selected to be 0.3 A to keep the per-unit inductance at 0.05 p.u., following the simulation condition. Note that the operating condition is not the rated one. However, it is required to ensure a low per-unit

synchronous inductance to follow the simulation condition. The second pole is selected to be at 271 rad/s, one-seventh of the first-pole frequency, leading to a capacitor value of 19 μF. Parameters of the experimental setup are summarized in Table 4.4.

The voltage ripple compensator has parameters $\beta_{ll} = 3$, $K_{ll} = 0.025$ V/V, $T_{ll} = 5 \times 10^{-4}$ s, $K_p^{pr} = 1$ A/V, $K_i^{pr} = 20$ A/V, $\omega_c^{pr} = 0.5$ rad/s, and $\omega^{pr} = 680$ rad/s. Tustin transformation with sampling time of 100μs is applied to convert the controllers in continuous time to discrete time for implementation on the Texas Instrument C2000 F28035 microcontroller. The integration time step is the same as the sampling time.

Experimental results and a performance metric are shown in Fig. 4.13(II) and Table 4.3, respectively. The active compensation is activated at 0.1 second. Before the activation, voltage ripple of the passive rectifier is reflected on the dc-bus voltage, as shown in Fig. 4.13(IIa). The ripple factor is 2.19%. After the activation, the dc-bus voltage ripple is reduced, leading to a ripple factor of 1.22%. Active compensation is achieved through current modulation, as shown in Fig. 4.13(IIb). Harmonic analysis in Fig. 4.13(IIc) shows a significant amplitude reduction of the 108 Hz component, the target compensation frequency. Simulation waveforms using the model discussed in Section 4.4.1 with parameters from the experimental setup is shown in Fig. 4.13(III). Close match between corresponding waveforms in Fig. 4.13(II) and Fig. 4.13(III) further corroborates validity of the proposed active-ripple compensation framework.

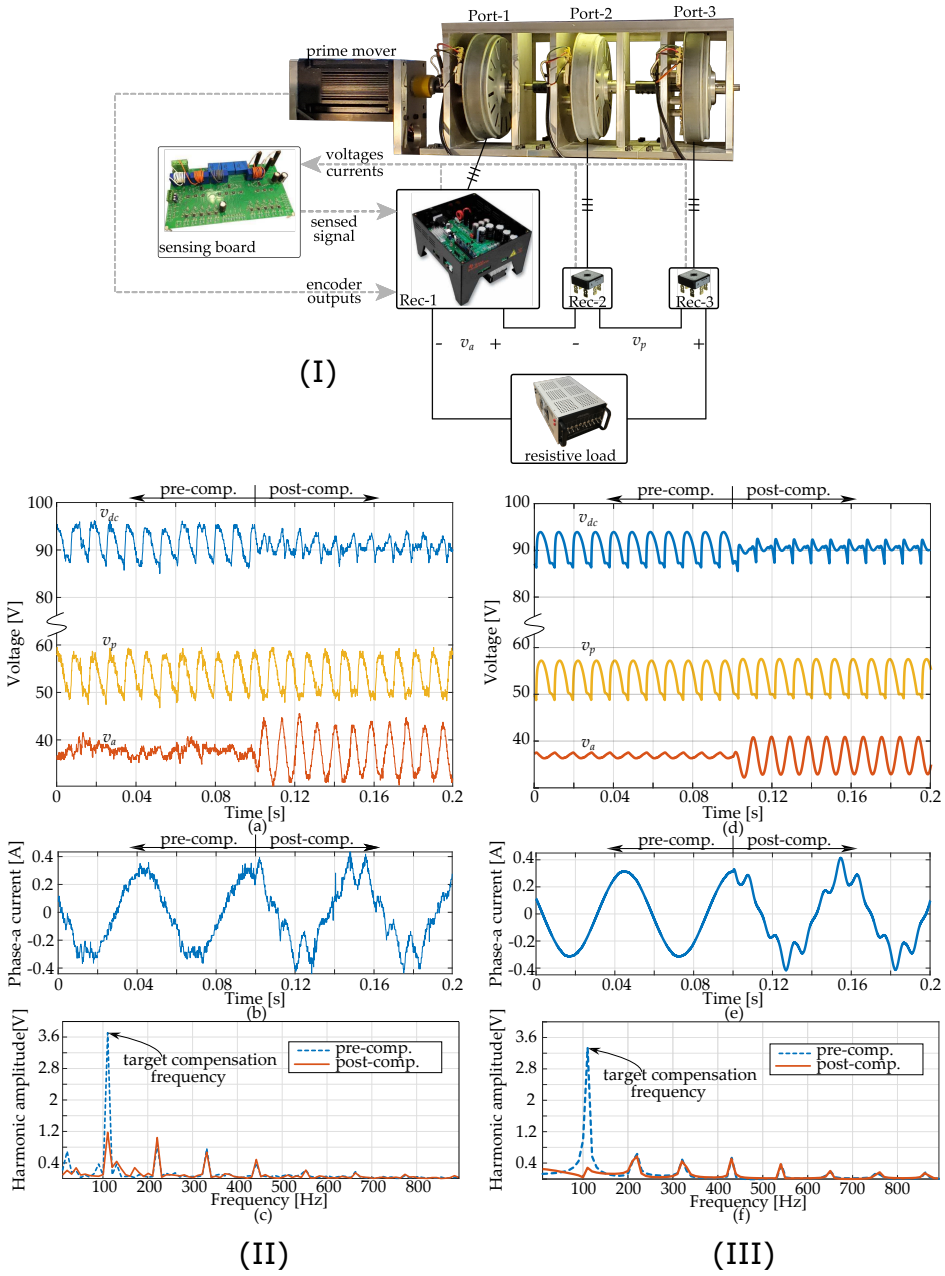


Figure 4.13: Experimental setup and results. (I) Experimental setup based on a three-port generator. Outputs of the rectifiers are serially connected to power a resistive load. The passive rectifiers Rec-2 and Rec-3 do not have filter capacitors. The active rectifier Rec-1 performs dc-bus voltage regulation and active voltage ripple compensation. (II) Experimental results on active voltage-ripple compensation. (a) The active rectifier modulates its dc-side voltage (red curve) to compensate for the voltage ripple of the passive rectifier (yellow curve) leading to a low-ripple dc bus voltage (blue curve). (b) Active compensation is attained by adding harmonics to the ac side current of the active rectifier. (c) Active compensation reduces the harmonic amplitude at 108 Hz by 67%, from 3.7 V to 1.2 V. (III) Simulation results corresponding to experimental waveforms in (II) using parameters from the experimental setup, as listed in Table 4.4.

Fig. 4.14 shows performance of the active-ripple voltage compensation at various dc-bus current conditions. At 45 rpm, each ac port has a back emf of 18 V (peak line-to-neutral). Using (4.32) with $n = 2$ for two passive rectifiers, the minimum active-rectifier dc-side voltage is 34 V. The no-load dc-side voltage of two passive rectifiers is 59.5 V. Consequently, the dc-bus voltage is the sum of the two, or 93.5 V. Step changes of 25% the rated dc-bus current value are applied. The average controller effectively maintains constant dc-bus voltage, as shown in Fig. 4.14(a). The active-voltage ripple compensation is activated throughout the whole period. Zoomed in waveforms for the passive-rectifier and dc-bus voltage ripple are shown in Fig. 4.14(b, c, d). The two voltage ripples are identical if active ripple compensation is not implemented. The graphs show that the dc-bus voltage ripple is lower than that of the passive rectifier. This reduction implies effectiveness of the compensation strategy at varying loading conditions.

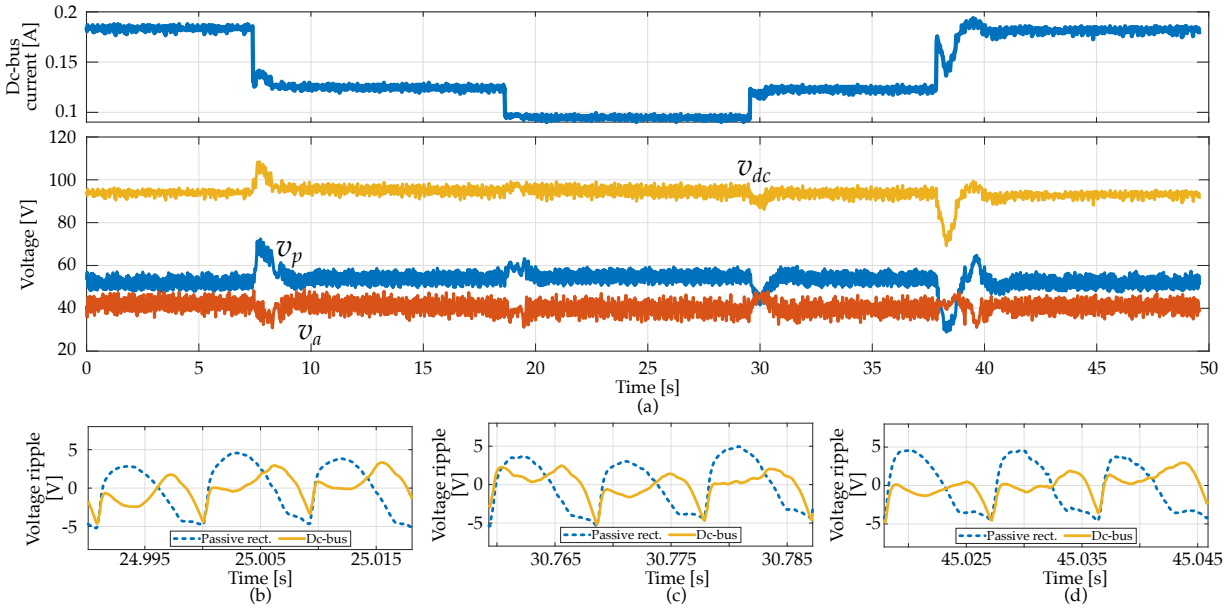


Figure 4.14: Experimental results under load-varying conditions. (a) Under different dc-bus current conditions, the dc-bus voltage is maintained at 93.5 V. (b,c,d) The dc-bus voltage ripple is lower than that of the passive-rectifier at time periods corresponding to different loading conditions.

4.5 Conclusions

This paper has presented a control methodology to use an active rectifier both as a filter element and a dc-bus voltage regulator. To perform the function of a filter element, the active rectifier modulates its dc-side voltage by injecting harmonics into the d-axis current. The voltage variation is opposite the passive-rectifier dc-side voltage, leading to an active compensation. The second function is fulfilled by adjusting the average value of the d-axis current using a PI controller with average dc voltages as the feedback signals. The proposed scheme is fundamentally different from the conventional filter-capacitor approach for voltage-ripple reduction. Energy stored in the mechanical structure is utilized to reduce the voltage ripple. Consequently, the filter capacitors can be removed. Elimination of these bulky elements leads to multiple benefits, including improvement in overall reliability and power density, as well as reduction in system cost.

Chapter 5

WIND-TURBINE MAXIMUM POWER-POINT TRACKING

Consider an integrated generator-rectifier system adapted for wind-energy applications as shown in Fig. 5.1. the prime mover is a wind turbine operating at variable speed. The wind turbine shares a common shaft with the multi-port PMSG. The ac power is converted to dc by the integrated generator-rectifier system. The dc output is connected to a stiff dc interface. The integrated generator-rectifier system performs power point tracking to extract the maximum power from the wind turbine.

Power flow control in the integrated generator-rectifier system, shown in Fig. 5.1 is challenging due to the presence of numerous passive rectifiers. The control is vital to achieve a maximum power point tracking (MPPT), which is imperative in the wind energy applications [12, 43, 58, 59]. The MPPT is accomplished through control of the series-connected active rectifier. The control framework based on a relationship between the active rectifier d-axis current and the dc-bus power is established.

This chapter is organized as follows: Section 5.1 discusses a method to reduce the dc-bus voltage ripple by shifting the generator back emfs. Section 5.2 discusses the power flow-control framework for the integrated generator-rectifier system and applies the methodology for MPPT. Simulation and experimental results are presented in Section 5.3 and 5.4, respectively, to corroborate the findings.

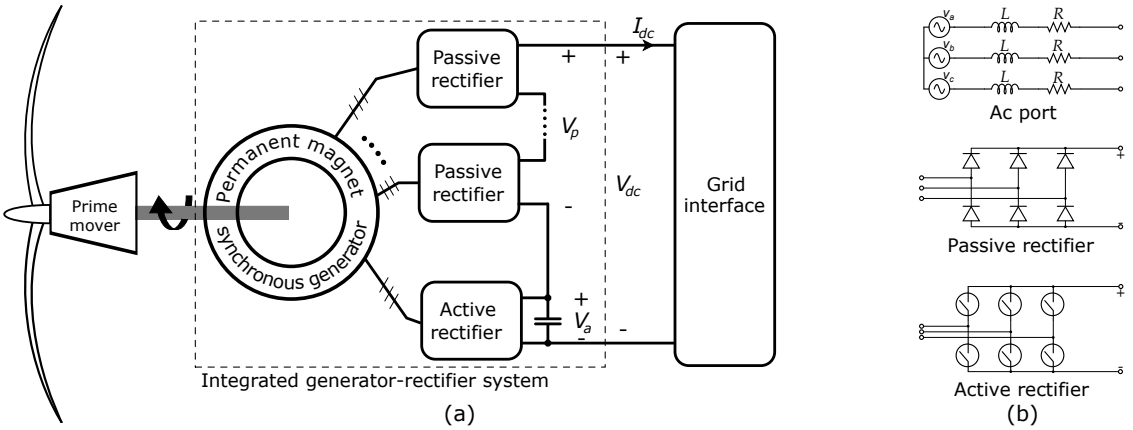


Figure 5.1: (a) Wind turbine power-point tracking architecture. (b) Circuit model for ac ports, passive, and active rectifier.

5.1 Voltage ripple reduction through phase-shifting the ac ports

Considering a PMSG with k three-phase ac ports, $(k-1)$ ports power passive rectifiers with no output filter capacitors. The dc output voltage ripple of each passive rectifier has a peak every $\frac{\pi}{3}$ radians, as shown in Fig. 5.2(a). Serial connection of the dc outputs with an appropriate phase shift leads to a minimal voltage ripple percentage, *defined as the ratio between the peak-to-peak ripple and the average value*. For example, the ripple percentage of two passive rectifiers with $\frac{\pi}{6}$ phase shifting is 3%, compared to 14% without phase shifting, as shown in Fig. 5.2(b). In general, a phase shift of $\frac{\pi}{3(k-1)}$ radian minimizes the voltage ripple for a system with $(k-1)$ passive rectifiers. Increasing the number of ac ports reduces the voltage ripple percentage but at a diminishing rate, as shown in Fig. 5.2(c). This technique is similar to the use of multi-pulse diode rectifiers and phase-shifting transformers in high power drives to reduce the line current harmonic distortion [60].

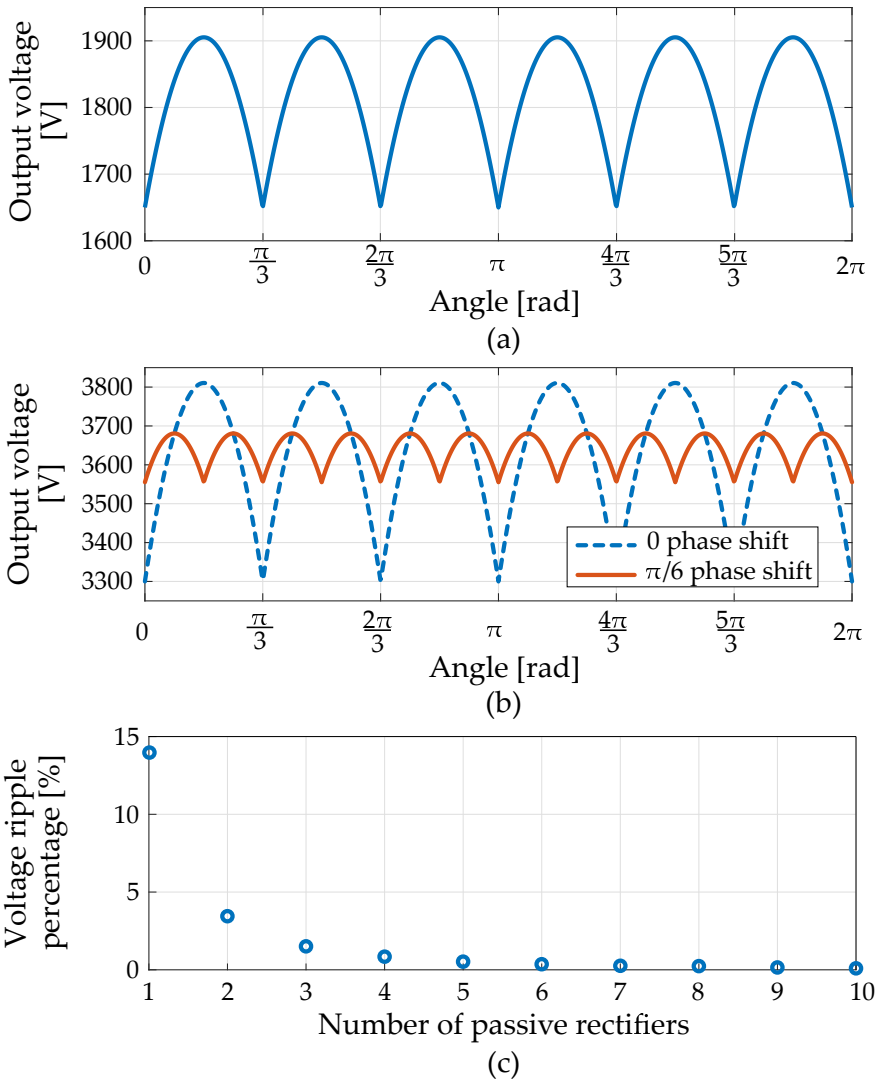


Figure 5.2: Example output voltage waveforms from the integrated system in Fig. 2.1 with each ac port generating 1.1 kV peak line-to-neutral voltage. (a) Dc output voltage of one passive rectifier. (b) Dc output voltage of two passive rectifiers connected in series with/without phase shifting between the corresponding ac ports. (c) Ratio between the voltage V_p peak-to-peak ripple and the average value reduces as the number of passive rectifiers increases.

5.2 Power-flow Control for the Integrated Generator-Rectifier System

This section develops the power-flow control framework for the proposed integrated generator-rectifier system. The system dc output is assumed to connect to a stiff dc interface. This assumption is valid for both ac and dc collection grids [1]. For the ac case, the interface is an intermediate dc

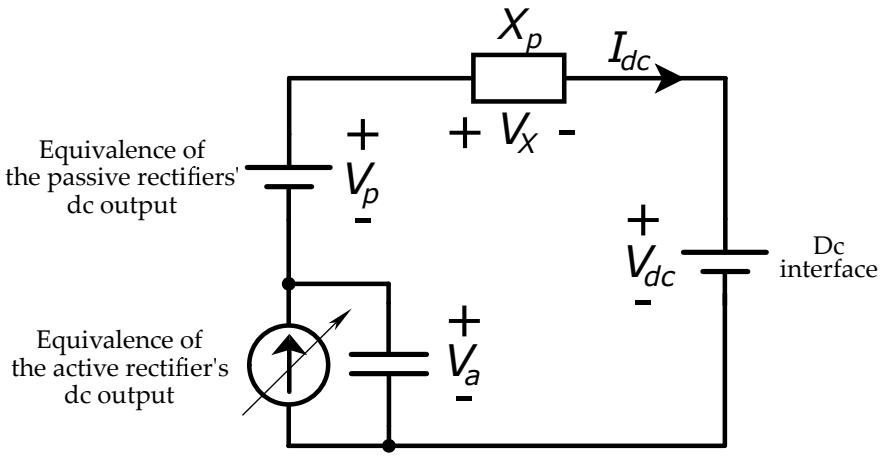


Figure 5.3: Simplified equivalent circuit of the integrated generator-rectifier system. The dc output of the passive rectifiers is modeled by a voltage source. The output of the active rectifier is modeled by a controllable current source. The serial voltage and current sources are connected to a constant dc voltage representing the dc interface.

bus that is maintained by a grid-side converter. For the dc case, the dc voltage is maintained by a converter at the dc-grid substation [2, 61].

A simplified equivalent circuit of the integrated system is shown in Fig. 5.3. The total output of the passive rectifiers is modeled as a generator-speed-dependent voltage source, denoted by V_p, in series with a commutation reactance, denoted by X_p. By ensuring a phase shift among different ac ports, the voltage ripple of the total passive rectifier output can be neglected, as detailed in Section 5.1. The active rectifier dc-side voltage, denoted by V_a, is determined by the difference between the constant grid interface voltage, V_{dc}, and the passive rectifier output voltage. The controllable amount of power drawn by the active rectifier determines its dc-side current. The active rectifier is modeled by a controllable current source. Due to the series connection, the current flowing out from the active rectifier determines the amount of power flowing into the dc bus, as detailed in Section 5.2.1. Cascaded proportional-integral (PI) controllers are proposed for practical implementation. The power-flow control framework is applied to perform MPPT in Section 5.2.2.

5.2.1 Power-flow control using the active rectifier

Assuming a negligible voltage ripple and a constant dc-bus current I_{dc}, the total dc output voltage of $(k-1)$ passive rectifiers at the generator speed ω is

$$V_{passive} = \underbrace{\frac{3}{\pi}(k-1)\sqrt{3}E(\omega)}_{V_p} - \underbrace{(k-1)\left(\frac{3}{\pi}\omega L + 2R\right)I_{dc}}_{V_X}. \tag{5.1}$$

where L and R are the synchronous inductance and per-phase equivalent series resistance of each ac port, respectively [47]. The back emf $E(\omega)$ is speed dependent:

$$E(\omega) = \frac{\omega}{2\pi f_0}E_0 \tag{5.2}$$

where f_0 and E_0 are the rated electrical frequency and the rated line-to-neutral peak back emf, respectively, of each ac port. The term V_X captures effects of the synchronous inductance, the phase resistance, and the dc-bus current on the dc-side voltage of the passive rectifier. The synchronous inductance is assumed to be sufficiently low such that the duration of phase current commutation is less than one-sixth of the electrical period, corresponding to Mode I operation of a conventional six-pulse diode bridge rectifier.

The next step is to derive a relationship between the active rectifier ac-side current and the dc bus power. Neglecting the conversion losses in the active rectifier, the power balance between the ac and the dc sides leads to

$$\frac{3}{2}E(\omega)I_{sd} - \frac{3}{2}I_{sd}^2R = V_aI_{dc} \tag{5.3}$$

where V_a is the active rectifier dc-side voltage and I_{sd} is the d-axis component of the active rectifier ac-side current. The d-axis is aligned with the peak phase-A back emf. Using Fig. 5.3,

$$V_a = V_{dc} - V_p - X_pI_{dc}. \tag{5.4}$$

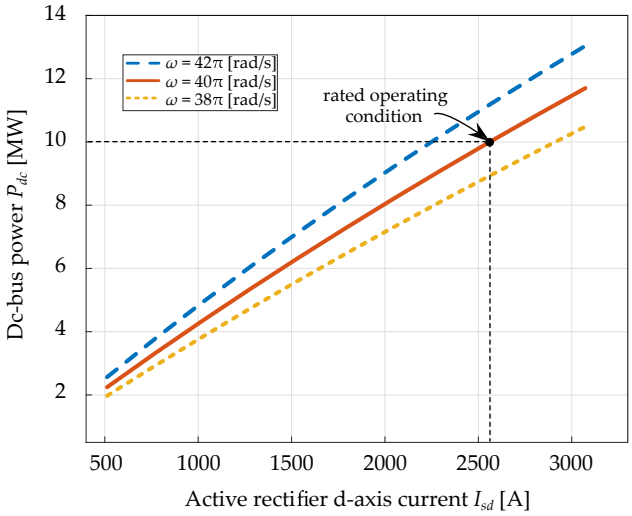


Figure 5.4: At each generator speed, the power drawn from the integrated generator-rectifier system depends on the active rectifier $d-$axis current.

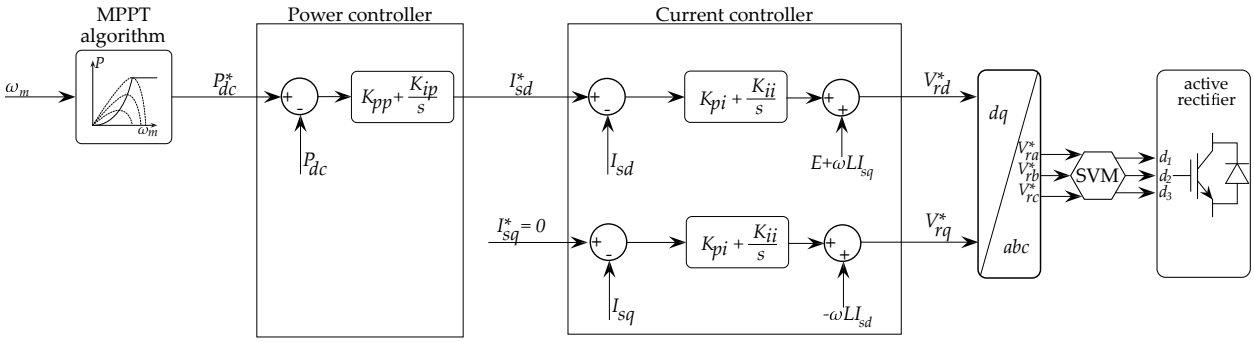


Figure 5.5: Cascaded architecture applied to the active rectifier to accomplish power-flow control for the whole integrated generator-rectifier system.

The dc-bus current is represented by

$$I_{dc} = \frac{P_{dc}}{V_{dc}} \tag{5.5}$$

where P_{dc} is the dc-bus power. Substituting (5.5) and (5.4) in (5.3), the dc-bus power relates to the active rectifier d-axis current by

$$\frac{3}{2}E(\omega)I_{sd} - \frac{3}{2}I_{sd}^2R = P_{dc}^2\left((k-1)\frac{1}{V_{dc}^2}\left(\frac{3}{\pi}\omega L + 2R\right)\right) + P_{dc}\left(1 - \frac{3}{\pi}(k-1)\frac{\sqrt{3}\mathcal{E}(\omega)}{V_{dc}}\right). \tag{5.6}$$

Equation (5.6) signifies that the active rectifier d-axis current can control the power flowing into the dc-bus, or, equivalently, the power drawn from the turbine.

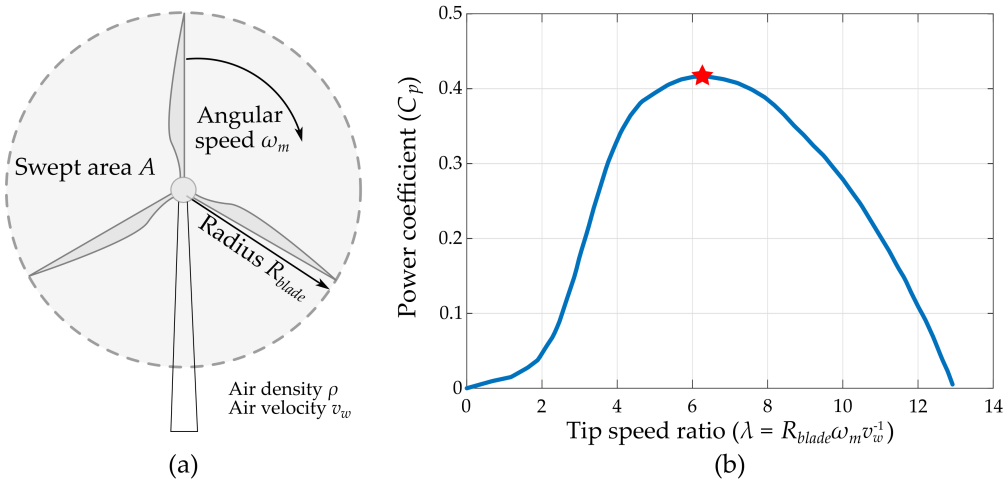


Figure 5.6: (a) Illustration of a three-bladed wind turbine. (b) A typical wind turbine power coefficient versus tip speed ratio curve [62].

Figure 5.4 illustrates the relationship between I_{sd} and P_{dc} using a 10 MW wind turbine system based on a three-port PMSG having a rated back emf of 1.1 kV at 20 Hz electrical frequency. The relationship is also demonstrated at two other electrical frequencies to show the possibility of using power control for regulation of the generator speed. Each ac port has the equivalent series resistance of 12 mΩ and the synchronous inductance L of 0.47 mH. These values correspond to 0.02 p.u. resistance and 0.1 p.u. synchronous reactance, respectively, at the rated operating condition.

Power-flow control can be achieved using a cascaded architecture, as illustrated in Fig. 5.5. The inner loop comprises current controllers to regulate the d-axis and q-axis currents of the active rectifier, as discussed in Chapter 4. The d-axis and q-axis current control the power flow and power factor, respectively. Setting the q-axis current to zero leads to a unity power-factor operation of the active rectifier. The outer-loop power controller calculates the d-axis current command to deliver the reference amount of power P_{dc}^{*} to the dc bus. The power command is the output of an MPPT algorithm that takes generator rotational speed as an input.

5.2.2 MPPT using Integrated Generator-Rectifier System

The proposed power-control architecture is applied to track the wind turbine maximum power point. MPPT is achieved if at each generator speed, the electrical power drawn follows the max-

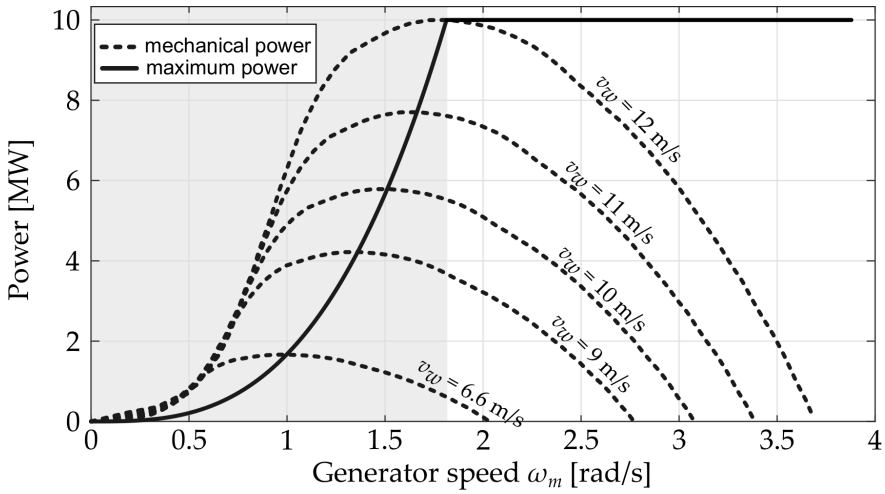


Figure 5.7: Mechanical power curves and maximum power curve of a 10 MW wind turbine.

imum power curve [43]. Consider a wind turbine in Fig. 5.6 with $R_{blade} = 90$ m, operating at a rated wind speed of 12 m/s and an air density ρ of 1.15 kg/m^3. Figure 5.7 plots the mechanical power curves of the wind turbine at various wind speeds using dashed lines. The maximum power curve is formed by connecting peak values of all the mechanical power curves. Consider the operation at a wind speed of 12 m/s. The vertical line crossing the intersection between the maximum power curve and the mechanical power curve splits the graph into two regions. In the gray region, the input mechanical power to the generator is higher than the output electrical power. The generator rotational speed increases. Then, the generator enters the white region, in which the mechanical power is lower than the electrical power. The generator slows down. Eventually, the speed settles at the border of the two regions, at which point the maximum power of 10 MW is generated.

5.3 Simulation Results

This section verifies the relationship between the active-rectifier d-axis current and the dc-bus power predicted by equation (5.6) using a Simulink model based on a three-port PMSG. Then a mechanical turbine model is incorporated and the integrated generator-rectifier system is controlled to perform MPPT. The results shows the current-power relationship is accurately predicted and the MPPT is achievable.

5.3.1 Power-flow control

Figure 5.8(a) shows the simulation diagram for the theoretical relationship verification. A three-port PMSG is modeled by three voltage sources with frequency and amplitude dependent on an external reference-speed signal. Parameters of each port follow the values given in Section 5.2.1. Port-1 and Port-2 are connected to three-phase diode rectifiers. The phase-A voltages (and also -B and -C) of these two ports are shifted $\frac{\pi}{6}$ electrical radian from each other to minimize the voltage ripple on the passive rectifiers' dc output. Port-3 powers an IGBT-based active rectifier that switches at 2 kHz. The rectifier outputs are serially connected to form the dc bus. The dc-bus voltage is maintained at 5.7 kV to represent the grid interface.

Figure 5.8(b) illustrates that the active-rectifier d-axis current is the control input for the dc-bus power. The upper plot shows the current waveforms corresponding to different active-rectifier d-axis current reference values, when the q-axis current is commanded to stay at zero. The dc-bus current follows the d-axis current. The dc-bus power varies proportionally to the dc-bus current, as shown by the bottom plot of Fig. 5.8(b).

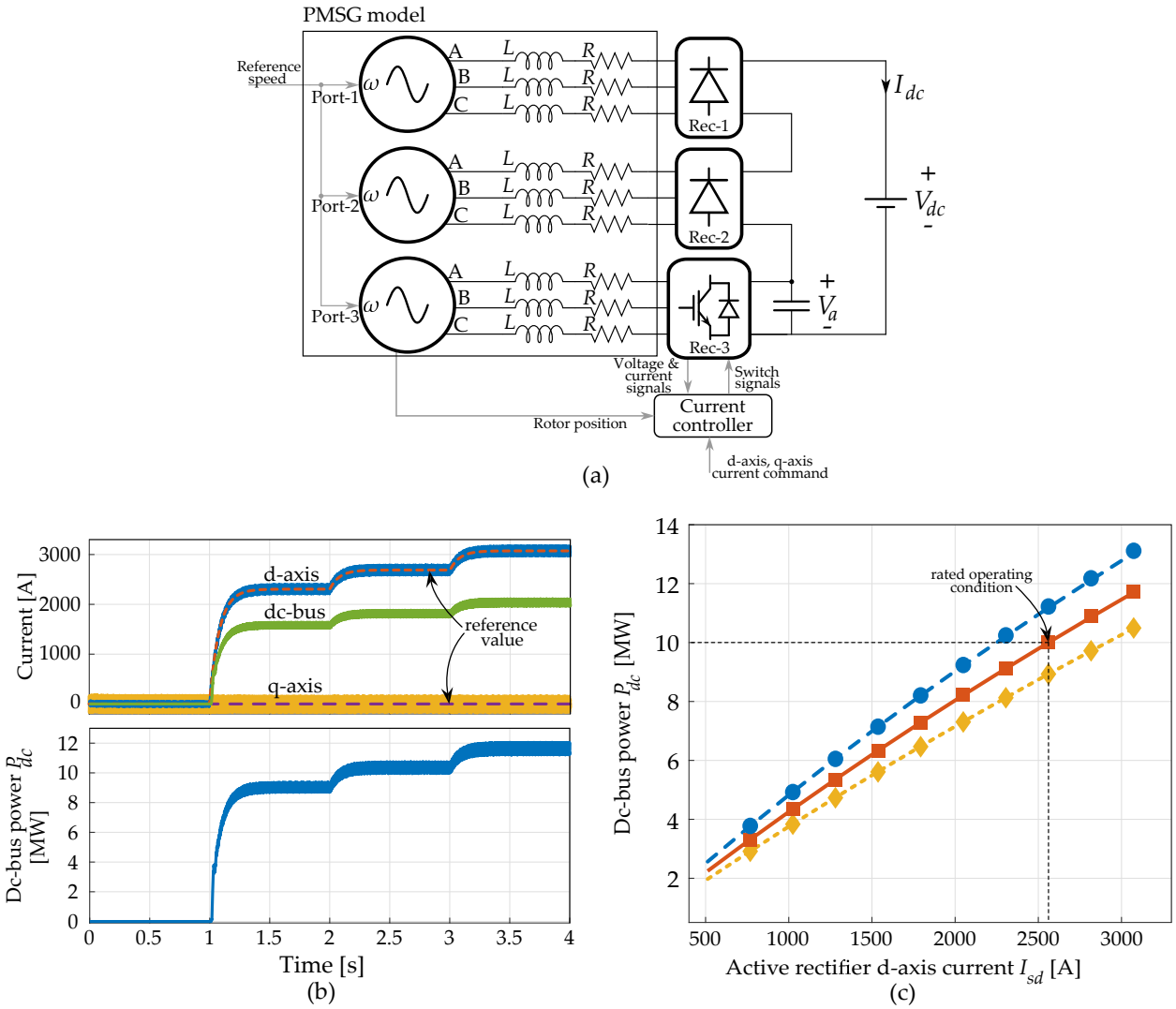


Figure 5.8: (a) Simulation diagram based on a three-port PMSG. (b) (Top plot) The active rectifier d-axis and q-axis current track the reference command, presented by the dotted lines. By changing the d-axis current, the dc-bus current varies accordingly, leading to a change in the dc-bus power (bottom plot). (c) The relation between dc-bus power and active-rectifier d-axis current acquired from the simulation model (recorded by the markers) matches the theoretical analysis (plotted by the lines using equation (5.6)).

Verification of the theoretical analysis, equation (5.6), is shown in Fig. 5.8(c). Different dc-bus power values are recorded at generator speeds $\omega = 38\pi,\ 40\pi$, and 42π rad/s, while the d-axis current takes values ranging from 500 A to 3100 A. The recorded dc-bus power is plotted versus the d-axis current using the diamond, square, and circle markers. For each ω, equation (5.6) is used to predict the dc-bus power and shown by dotted, solid and dashed curves.

5.3.2 MPPT illustration

The simulation model presented in Fig. 5.8(a) is used to illustrate the application of the proposed integrated generator-rectifier system to achieve MPPT. The reference speed to the generator is the output of a wind turbine with dynamics

$$J\omega_m \frac{d\omega_m}{dt} = P_{turbine} - P_{dc} \tag{5.7}$$

where J is the wind turbine moment of inertia, chosen to be 28.7×10^6 kg.m^2. To reduce the total running time of the simulation, this value is selected to be 50 times lower than a representative value for a 10 MW turbine [55]. For each wind speed, the turbine power $P_{turbine}$ follows the mechanical power curve in Fig. 5.7. Taking the turbine rotational speed as the feedback signal, the MPPT algorithm in Fig. 4.5 sets the power controller reference value to follow the maximum-power curve in Fig. 5.7.

Figure 5.9 shows that the proposed integrated generator-rectifier architecture tracks the wind turbine maximum power point. At time zero, the turbine rotates at 55% of the rated speed and the wind speed is 12 m/s. The turbine mechanical power is 10 MW while the dc-bus is commanded to draw 2 MW. The 8 MW difference speeds up the wind turbine. As the turbine speed increases following the solid-blue line in Fig. 5.9(a), the MPPT algorithm increases the power command sent to the power controller, shown by the dotted-orange line in Fig. 5.9(b). Eventually, the electrical power equals the mechanical power, making the wind turbine settle to the optimal speed, at which point the maximum power of 10 MW is extracted. The corresponding d-axis and q-axis currents are shown in Fig. 5.9(c).

The operation under varying wind speed conditions is also illustrated in Fig. 5.9. At instances $t = 5.5$ second and $t = 10.5$ second, the wind speed changes to 10 m/s and 11 m/s, respectively. In response to the wind speed variation, the MPPT controller varies its power command, shown by the dotted-orange lines in Fig. 5.9(b). The dc-bus power successfully tracks the reference power, allowing the turbine to rotate at the optimal speed for maximum power extraction.

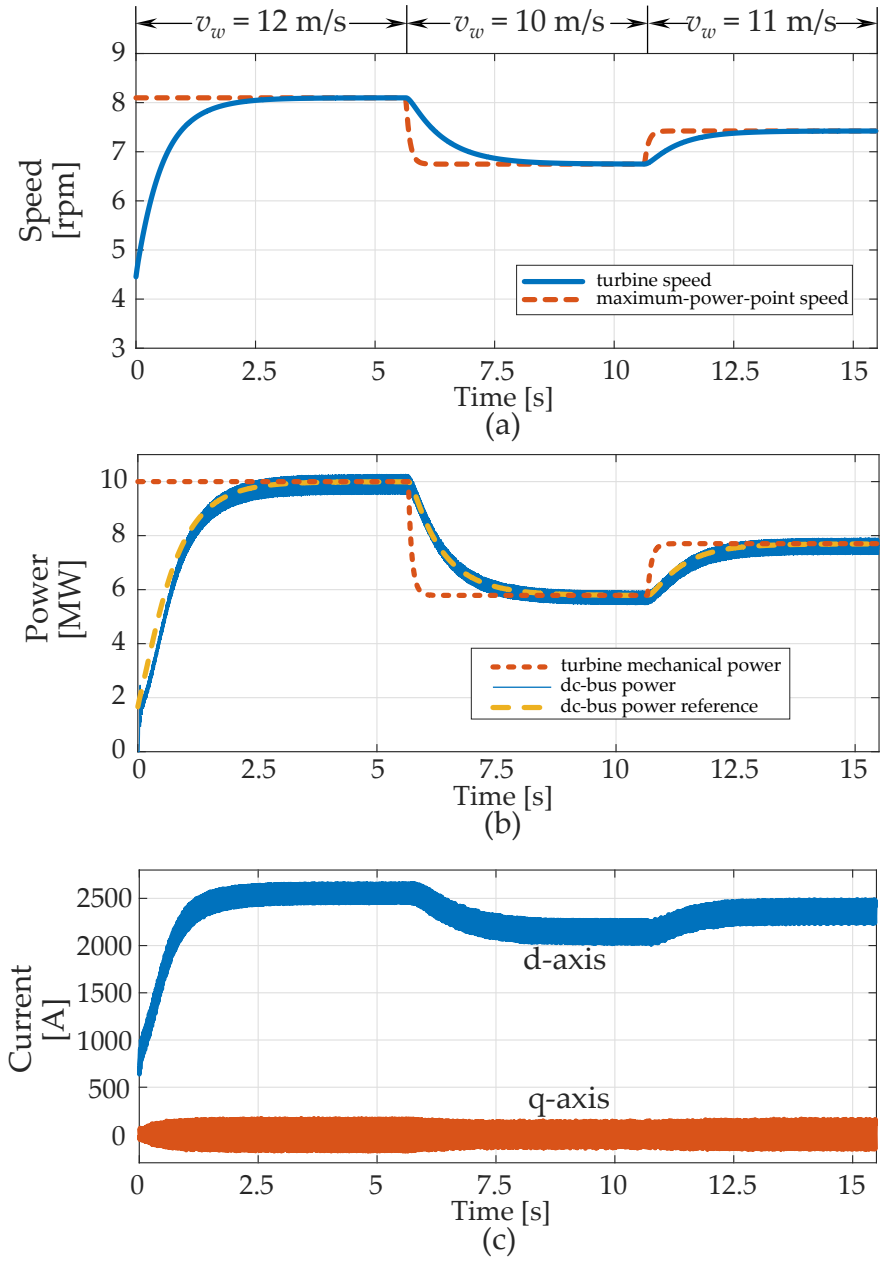


Figure 5.9: Key waveforms to illustrate the system maximum power point tracking capability. (a) At each wind speed, the turbine speed (solid-blue line) successfully tracks the optimal speed to generate maximum power. (b) The dc-bus power and the turbine mechanical power versus time. (c) The d-axis and q-axis current to achieve the maximum power point tracking.

5.3.3 PMSG power quality and torque ripple assessment

This section quantifies the impacts of the distorted ac currents due to the diode-bridge operation on the total PMSG power quality as well as estimates the generator torque ripple.

Fig. 5.10(a) shows the phase-A back emfs corresponding to Port-1, Port-2, and Port-3 at the 20-Hz rated electrical frequency. At 10-MW rated power drawn by the dc-bus, the phase-A currents of the three ac ports are shown in Fig. 5.10(b). The currents corresponding to the diode bridges are non-sinusoidal, as expected. The total PMSG input power is calculated by adding instantaneous power output of all the back emf sources, as shown in Fig. 5.10(c). The total input power is slightly greater than 10 MW to account for the generator resistive losses. 60% of the total power is processed by the passive rectifiers connected to Port-1 and Port-2. The ripple factor, *defined as the ratio between ripple-power rms value and the dc power value*, is used to quantitatively assess the input power ripple. At the rated condition, the ripple factor is 0.4%.

Operation at the minimum generator speed is considered next to evaluate the ripple factor variation as a function of the generator input power. The back emf amplitude and frequency are proportional to the generator speed. Therefore, both decrease for a minimum operating speed that equals to 55% of the rated value, as shown in Fig. 5.10(d). The ac-port currents vary, as illustrated in Fig. 5.10(e), to deliver the amount of power shown in Fig. 5.10(f). For a wind turbine, the input power is proportional to the cube of the generator speed [43], resulting in the input power to be 1.7 MW at the minimum operating speed. Unlike Fig. 5.10(c), majority of the power is processed by the active rectifier connected to Port-3, as shown in Fig. 5.10(f). The ripple factor is 2.4%. Fig. 5.11 shows the ripple factor for the entire operating speed range as a function of the input power. Due to high inertia of a wind turbine, the mechanical speed can be considered to be relatively constant within the time scale of the electrical dynamics. Consequently, this power ripple is equivalent to the torque ripple. The integrated generator-rectifier system exhibits a ripple factor lower than the acceptable level of 5% to 10% [63, 64].

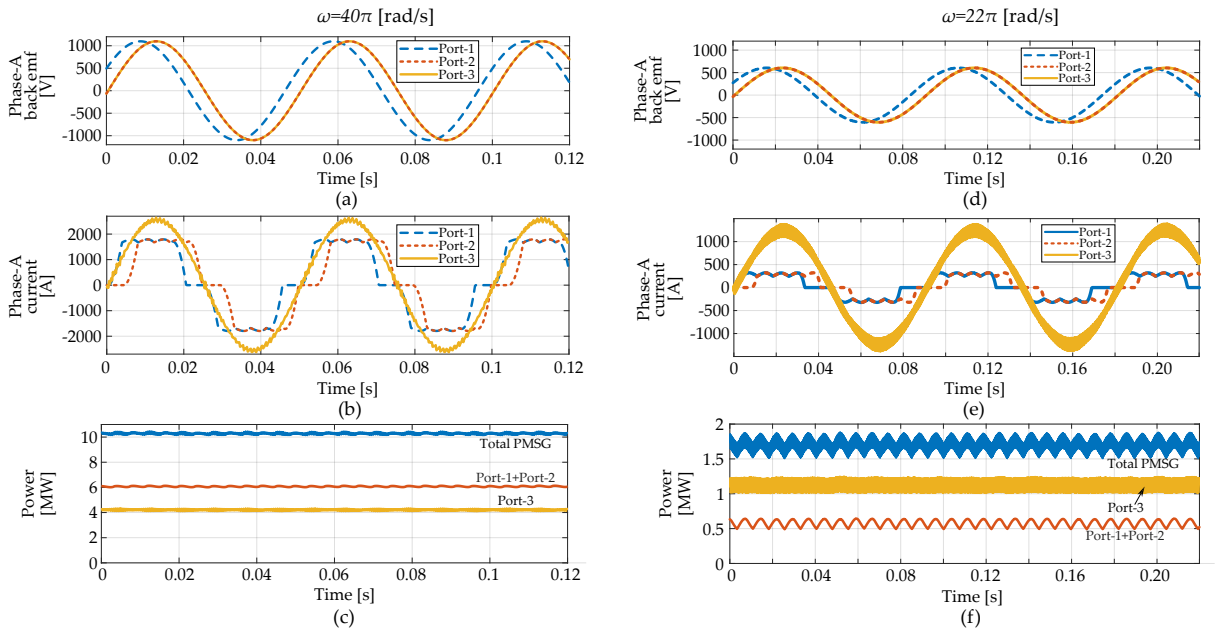


Figure 5.10: Generator phase-A back emf, phase-A current, and power of the passive and active rectifiers at different operating speeds. (a) Sinusoidal and phase-shifted back emfs at the rated generator speed. (b) The corresponding phase-A currents. (c) Sharing of PMSG input power between ac ports powering active versus passive rectifiers. (d) Back emfs at the minimum operating speed that is equal to 55% the rated speed. (e) Phase-A currents corresponding to the minimum speed. (f) Power sharing between the ac ports powering active and passive rectifiers at the minimum operating speed.

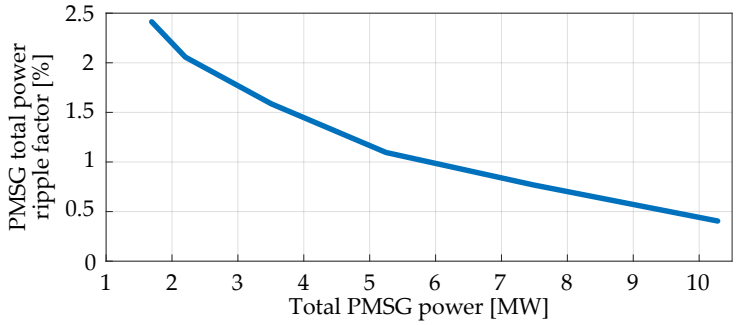


Figure 5.11: Ripple factor of the total PMSG power is always below 2.5% and decreases as the output power increases.

5.4 Experimental results

Similar to the simulation results section, this section first verify the current-power relationship and then illustrate that MPPT is achievable on an experimental setup. The multi-port generator is experimentally emulated using three Samsung DC96-01218D PM machines that have three phases and 48 poles, as shown in Fig. 5.12(a). The machine assembly is shown in Fig. 5.12(b). Each phase has an equivalent series resistance of $2\ \Omega$ and an equivalent series inductance of 6.5 mH, measured at 60 Hz. The machine produces a sine-wave back emf with a back emf constant 0.131 V(peak line to neutral)/rpm.

Three ac-port assemblies, named Port-1, Port-2, and Port-3, are axially joined using shaft couplers to form a generator, as shown in Fig. 5.12(b). The couplers allow free adjustment of the rotor relative angular position, resulting in a phase-shifted back emf between different ac ports. A $\frac{\pi}{6}$ electrical radian phase shift is created between Port-1 and Port-2 to minimize the dc-bus voltage ripple. The setup illustrates only the phase-shifting concept, and does not reflect a real multi-port PMSG design for off-shore wind.

Port-1 and Port-2 feed passive rectifiers MT3516A. Dc outputs of the rectifiers are serially stacked to form a dc bus. Port-3 powers the active rectifier Rec-3, made from a Texas Instruments High Voltage Motor Controller and PFC Developer's Kit. The dc bus is regulated by the electronic load Magna Power ARx operating in constant voltage mode. The PMSG is driven by a programmable prime mover that can operate in constant speed, constant torque, or wind turbine emulator mode.

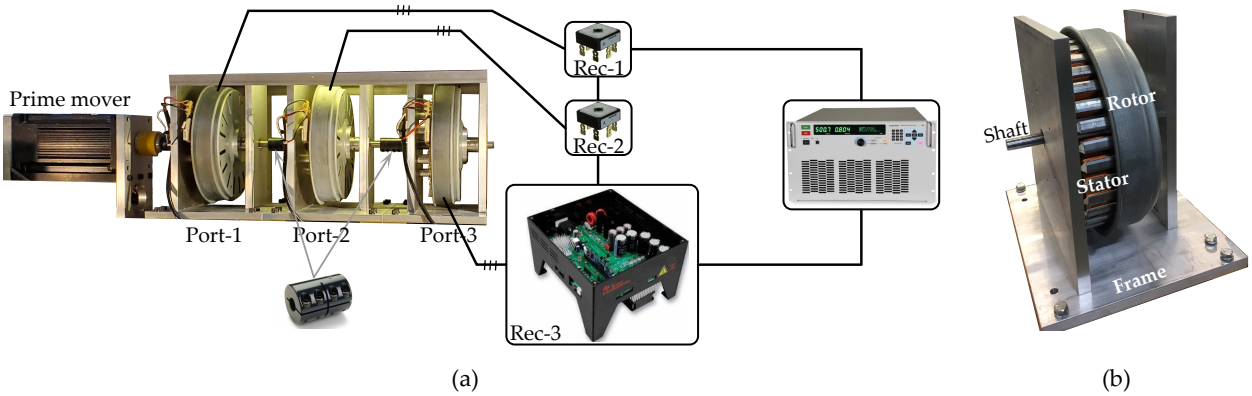


Figure 5.12: Experimental setup. (a) Single ac port assembly. (b) Three ac-port assemblies are joined using couplers, allowing phase shifting between ports. Port-1 feeds the active rectifier while Port-2 and Port-3 power passive rectifiers. Dc outputs are serially stacked and connected to a constant dc bus maintained by an electronic load operating in constant voltage mode. Note that the PMSG setup is used only to validate the phase-shifting concept and does not reflect a real PMSG design for off-shore wind.

5.4.1 Dc-bus power – active rectifier current relationship

The relationship between the active rectifier d-axis current and the dc-bus power is validated experimentally. A prime mover operating in speed-regulation mode drives the generator at three operating points: 150 rpm, 300 rpm, and 450 rpm. These three values correspond to dc-bus voltages of 100 V, 200 V, and 300 V, respectively, to be maintained by the electronic load. The dc-bus voltages are chosen to be the minimum values that ensure controllability of the active rectifier, i.e., the sum of the maximum open-circuit line-to-line back emf of all the ac ports. Although a higher dc-bus voltage is possible, the volt-ampere rating requirement on the active rectifier is increased [35].

Figure 5.13(a) shows the active, the passive, and the dc-bus current waveforms. The active rectifier drives sinusoidal current out of Port-3. The phase currents of Port-1 (and also Port-2) are non-sinusoidal, as expected due to operation of the passive-rectifier. The current flowing to the dc-bus is constant with a low ripple due to the phase shift between Port-1 and Port-2. Figure 5.13(b) validates the theoretical and experimental relationship between the d-axis current and the dc-bus power. The theoretical values are predicted by equation (5.6). The dc-bus power is measured at the output of the generator set.

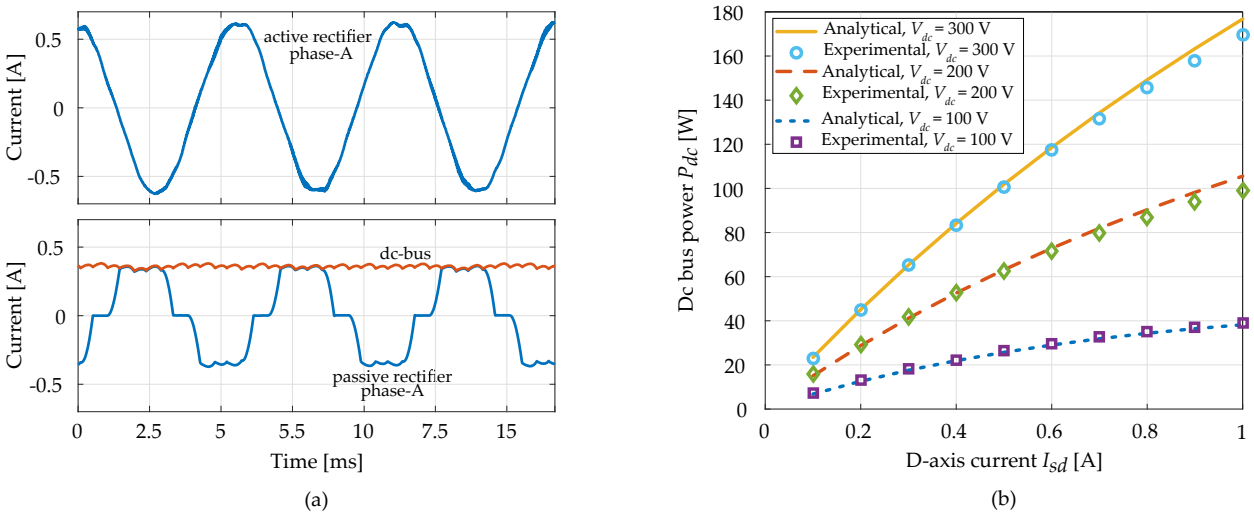


Figure 5.13: (a) Current waveforms from the experimental setup: (top) phase current of Port-1, feeding active rectifier, (bottom) phase current of Port-2, feeding passive rectifier, and dc-bus current. The power factor at the active rectifier is 1 and at the passive rectifier is 0.91. (b) Theoretical relationship between the active rectifier d-axis current and dc-bus power is validated by experimental measurements. The lines illustrate the theoretical predictions in equation (5.6), while the experimental measurements are recorded by the discrete markers.

5.4.2 MPPT validation

The prime mover is programmed to emulate a wind turbine with mechanical power characteristics shown by the solid blue curve in Fig. 5.14(a). The amount of electrical power extractable at the dc-bus, shown by the orange dots, is lower than the programmed values due to the power train losses, approximately 35%. These experimental measurements are achieved by setting the active rectifier d-axis current to the values of the orange dots in Fig. 5.14(b). The maximum power point is tracked by utilizing the d-axis current profile versus the rotational speed shown by the solid blue line in Fig. 5.14(b). The intersection at the speed corresponding to the maximum power point ensures MPPT.

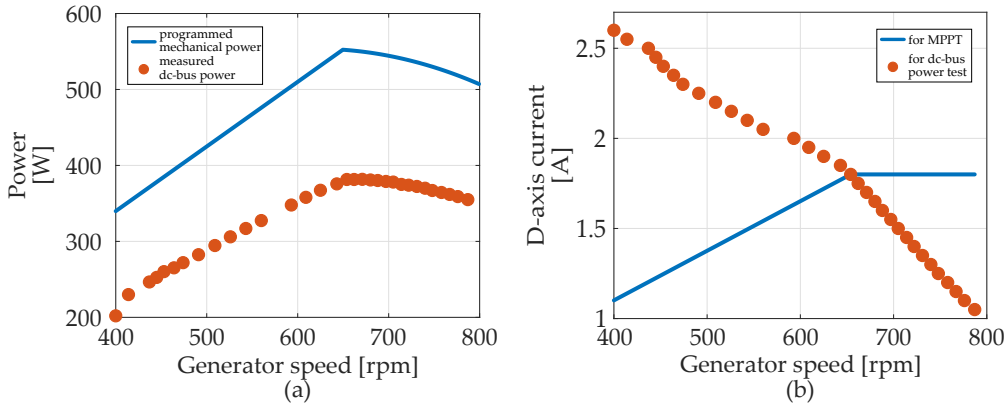


Figure 5.14: Power characteristics of the wind turbine. (a) The amount of power delivered to the dc-bus has a peak value of 381 W at a generator speed of 656 rpm. (b) The power is experimentally measured by applying a torque profile following the solid-orange line. The dashed-blue curve is used to achieve MPPT.

Figure 5.15 illustrates the waveforms of the MPPT operation. Before 1.2 seconds, the prime mover rotates at a constant 391 rpm. At 1.2 seconds, the prime mover enters the turbine emulator mode. The generator speeds up and eventually settles at 656 rpm, as shown in Fig. 5.15(a). Figure 5.15(b) shows the passive rectifier voltage increases with the rotational speed. Meanwhile, the active rectifier dc-side voltage is reduced due to a constant dc-bus voltage. At the optimal rotational speed, the dc-bus power is 381 W, coinciding with the maximum power point shown in Fig. 5.14.

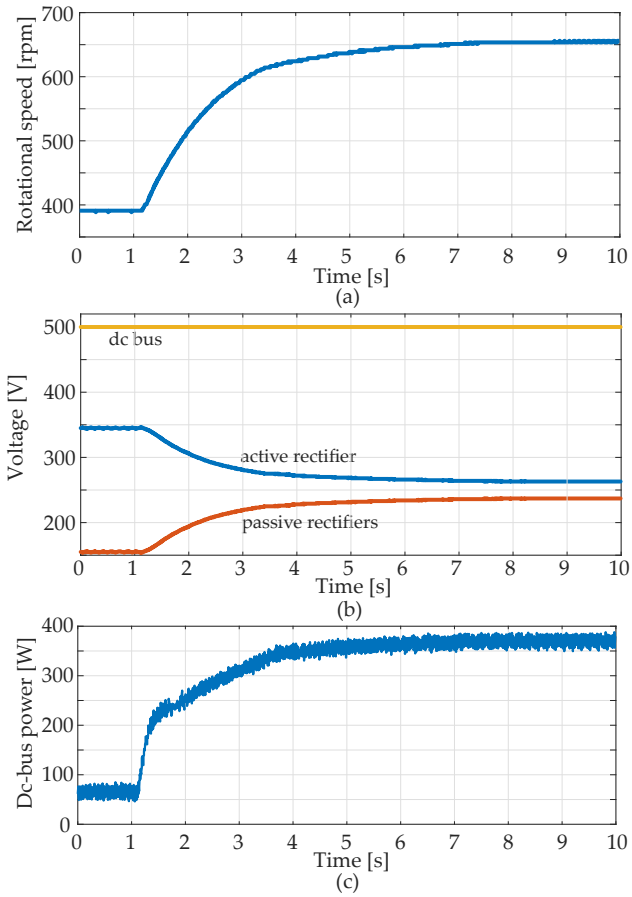


Figure 5.15: Waveforms of the MPPT operation. (a) The turbine starts at 391 rpm and settles at 636 rpm, the speed for maximum power generation. (b) The passive rectifier dc-side voltage increases as the rotational speed increases. The active rectifier dc-side voltage behave oppositely. The dc-bus voltage is constant at all the rotational speed. (c) The dc-bus power successfully track the maximum value of 381 W.

5.5 Conclusions

This chapter has illustrated the MPPT capability of the integrated generator-rectifier system in wind-turbine applications. Although multiple uncontrollable diode presents in the system, power-flow control capability is still achievable through the active rectifier due to the serially-connected configuration. In essence, the active rectifier operates as a controllable current source while the diode bridges behaves as generator-speed-dependent voltage sources. Adjustment of the current variation of the passive-rectifier power output.

Chapter 6

WINDING LAYOUT CONSIDERATIONS FOR AN INTEGRATED GENERATOR-RECTIFIER SYSTEM

The design, analysis, and control of the integrated generator-rectifier system previously considered the multi-port generator as isolated ac ports modeled using a series resistance, inductance, and a speed-dependent voltage source (RLE). However, the generator-rectifier interaction is complex, especially when the ac ports are magnetically coupled. This chapter presents an analytical framework to capture the interaction between different generator ac ports and the rectifiers by considering the complete generator inductance matrix, capturing all self and mutual inductances. Requirements on the inductance matrix are derived to ensure the isolated-RLE model's validity from a design and control perspective even in the presence of magnetic coupling among different ac ports. The analysis reveals a trade-off between the dc bus power ripple and the power imbalance between the active and passive sections of the generator. Finally, a fractional-pole-pitch winding layout is proposed as an example to provide a required 20-degree phase shift among the passive ports, while achieving a complete magnetic decoupling from an equivalent circuit standpoint. The desired properties are verified using a generator finite-element-analysis (FEA) model at a 10-MW power level. A simulation coupling the FEA model to the rectifier circuit proves that a low dc-bus power ripple and a low generator torque are simultaneously achieved. The fractional-pole-pitch structure is also experimentally implemented at a low power level. The analysis paves the way for development of other machine topologies that are guaranteed to work with the integrated rectifier system.

The rest of this chapter is organized as follows: Section 6.1 provides the theoretical analysis of the generator requirements to meet the power converter demand. Section 6.2 discusses a compatible generator configuration that axially splits the sections for the active and passive rectifiers. Section 6.3 verifies the proposed topology via a sample design at a 10-MW power level. Finally, a low-power experimental setup is exhibited in Section 6.4.

6.1 Framework for Generator and Rectifier Integration

This section presents a generalized circuit representation of the integrated generator-rectifier system considering the magnetic coupling across all the generator phases. Conditions for the magnetic decoupling are derived assuming that the neutral points of all the ac ports are electrically isolated. Under these constraints, the active rectifier could be controlled as a dc current source and the passive-rectifier ac ports are representable using RLE equivalent circuits. A per-unit circuit is then constructed to evaluate the dc-bus power ripple and the output-power imbalance between one passive and the active ports. Finally, a trade-off is established between these two quantities. This trade-off curve can be used as an additional input to the generator design to achieve a specific dc-bus power ripple and output power ratio between the active and passive ports.

6.1.1 Generalized circuit representation of the integrated generator-rectifier system

Fig. 6.1 shows the generalized circuit representation of an integrated generator-rectifier system based on a k-port generator with the magnetic coupling represented using current-dependent voltage sources. Port P_1 powers an active rectifier, and the others are each connected to a three-phase passive rectifier without an output capacitor. Each phase in an ac port is modeled by a speed-dependent back emf source, a self inductance, a resistance, and the current-dependent voltage source, all connected in series. In general, the phase-A back emf of port P_i is

$$E_{PiA} = E_i \sin(\omega t + \theta_i) \tag{6.1}$$

where E_i is the amplitude, ω is the electrical frequency, and θ_i the relative phase shift between port P_i and port P_2. The phase-B and phase-C back emfs of each port lag the phase-A back emf by $2\pi/3$ and $4\pi/3$, respectively. An appropriate θ_i among different passive ports reduces the total passive port voltage ripple, thereby, eliminating the need for bulky dc-side filter capacitors to smooth the output power [65]. It will be shown in Section 6.2 that the necessary phase shift is achieved using a specific winding layout.

The current-dependent voltage source in each phase captures the induced voltage on the phase

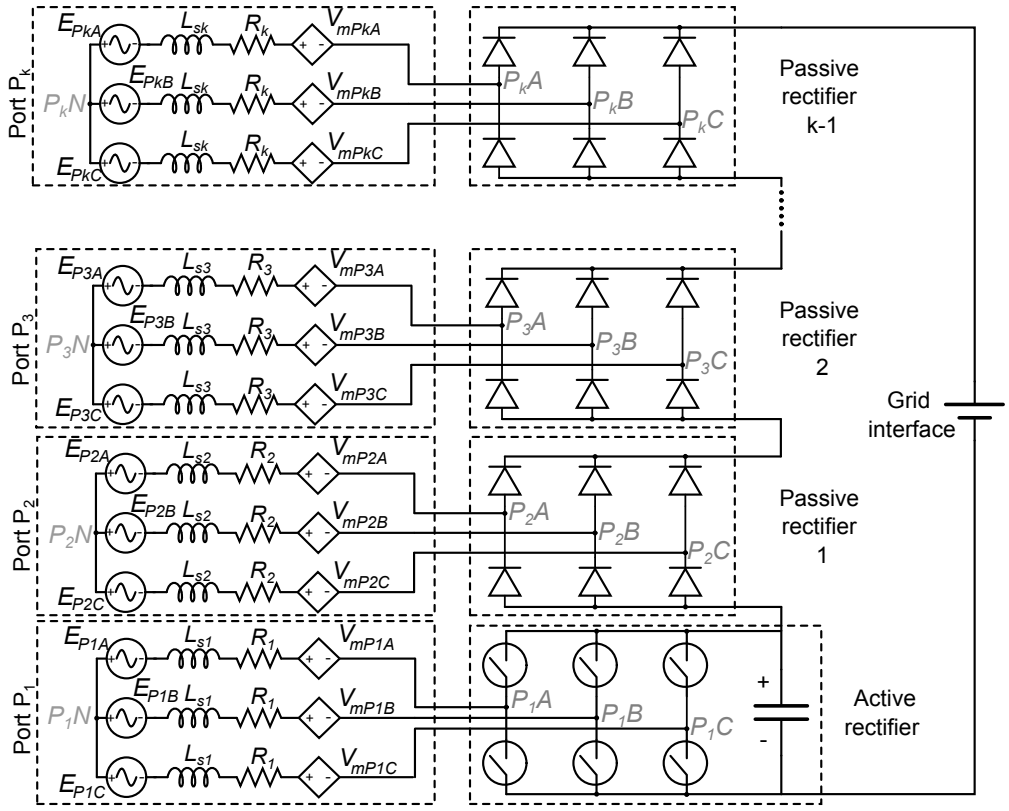


Figure 6.1: Electrical circuit representation of an integrated generator rectifier system.

due to current variation in all the other phases, including the one from different ac ports. For example, the induced voltage on port P_i phase-A is:

$$V_{mPiA} = \underbrace{L_{PiA,PiB}\frac{dI_{PiB}}{dt} + L_{PiA,PiC}\frac{dI_{PiC}}{dt}}_{V'} + \underbrace{\sum_{j=1...k\ j\neq i,\ X\in\{A,B,C\}} L_{PiA,PjX}\frac{dI_{PjX}}{dt}}_{V''} \tag{6.2}$$

where j indexes all other ports, $L_{PiA,PjX}$ represents the mutual inductance between phase A of the P_i port and phase X of the P_j port (X could be either A, B, or C), and I_{PjA} denotes the phase-A current in port P_j.

6.1.2 Conditions to decouple different generator ac ports

From a circuit standpoint, the phases are decoupled if the current-dependent voltage source in one phase is representable only as a function of the current in the same phase. Evident from (6.2), the voltage comprises two components, one due to different phases within the same ac port, and the other from the different ac ports. The currents in each port are always balanced due to the neutral point isolation, e.g., $I_{PiA} + I_{PiB} + I_{PiC} = 0,\ \forall i = 1..k$. Dependency of V' on other phase currents is eliminated by keeping the mutual inductances between any two phases within the same ac port equal, e.g., $L_{PiA,PiB} = L_{PiA,PiC}$. V'' is eliminated by ensuring identical mutual inductances between any two ac ports, e.g., $L_{PiA,PjA} = L_{PiA,PjB} = L_{PiA,PjC}$. With these conditions, equation (6.2) reduces to

$$V_{mPiA} = -M_i\frac{dI_{PiA}}{dt} \tag{6.3}$$

Table 6.1: Required inductance matrix for RLE representation of all generator phases

Phase	A_{P1}	B_{P1}	C_{P1}	A_{P2}	B_{P2}	C_{P2}	...	A_{Pk}	B_{Pk}	C_{Pk}
A_{P1}	L_{s1}	M_1	M_1	M_{12}	M_{12}	M_{12}	...	M_{1k}	M_{1k}	M_{1k}
B_{P1}	M_1	L_{s1}	M_1	M_{12}	M_{12}	M_{12}	...	M_{1k}	M_{1k}	M_{1k}
C_{P1}	M_1	M_1	L_{s1}	M_{12}	M_{12}	M_{12}	...	M_{1k}	M_{1k}	M_{1k}
A_{P2}	M_{12}	M_{12}	M_{12}	L_{s2}	M_2	M_2	...	M_{2k}	M_{2k}	M_{2k}
B_{P2}	M_{12}	M_{12}	M_{12}	M_2	L_{s2}	M_2	...	M_{2k}	M_{2k}	M_{2k}
C_{P2}	M_{12}	M_{12}	M_{12}	M_2	M_2	L_{s2}	...	M_{2k}	M_{2k}	M_{2k}
...	...	...	...	...	...	...	...	...	...	...
A_{Pk}	M_{1k}	M_{1k}	M_{1k}	M_{2k}	M_{2k}	M_{2k}	...	L_{sk}	M_k	M_k
B_{Pk}	M_{1k}	M_{1k}	M_{1k}	M_{2k}	M_{2k}	M_{2k}	...	M_k	L_{sk}	M_k
C_{Pk}	M_{1k}	M_{1k}	M_{1k}	M_{2k}	M_{2k}	M_{2k}	...	M_k	M_k	L_{sk}

	Active port	Passive port
Active port	$\mathbf{L_{AA}}$	$\mathbf{L_{AP}}$
Passive port	$\mathbf{L_{AP}^T}$	$\mathbf{L_{PP}}$

where M_i is the mutual inductance between any two phases of port P_i. Therefore, the per-phase voltage between nodes P_iN and P_iA in Fig. 6.1 becomes

$$\begin{aligned} V_{PiN,PiA} &= E_{PiA} + L_{si}\frac{dI_{PiA}}{dt} + R_i I_{PiA} - M_i I_{PiA} \\ &= E_{PiA} + L_i\frac{dI_{PiA}}{dt} + R_i I_{PiA} \end{aligned} \tag{6.4}$$

where $L_i = L_{si} - M_i$ represents the equivalent inductance with L_{si} being the self inductance of the P_i port. This voltage equation represents an RLE model for phase-A of port P_i.

The magnetic decoupling could be achieved for all the other phases if the inductance matrix follows the form in Table 6.1. Under this condition, the integrated generator-rectifier system is representable by the simplified circuit in Fig. 6.2. The active rectifier can draw constant power because the equivalent inductances and resistances of all the phases are identical. Therefore, it is represented by an ideal current source in parallel with a capacitor [65]. In addition, all the mutual voltages are eliminated. Parameters for the circuit are derived next.

6.1.3 Per-unit equivalent circuit

A per-unit equivalent representation eliminates the need for actual voltage and actual power for circuit analysis. This circuit is useful because the generator per-unit reactance is terminal-voltage and output-power independent [66]. The generator stack length and number of turns could be scaled to meet the power and voltage levels without affecting the rectifier system features, such as the power percentage processed by the active rectifier, the power imbalance between the ac ports, and the dc-bus power ripple percentage.

The first step to develop the circuit is to define the base quantities. The base voltage is defined

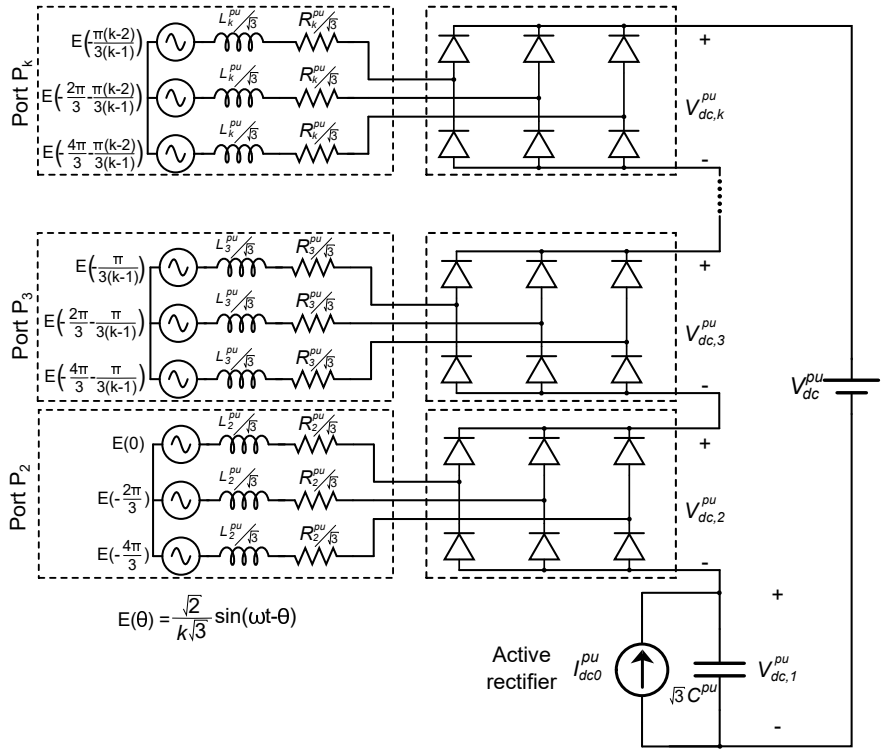


Figure 6.2: Equivalent circuit of the integrated generator-rectifier system considering the control strategy. The circuit parameters are expressed in per-unit.

as

$$V_{base} = \sum_{i=1..k} \frac{E_i\sqrt{3}}{\sqrt{2}} \quad , \quad \text{and} \;\; P_{base} = P_{rated} \tag{6.5}$$

where E_i is the line-to-neutral peak back emf of port P_k and P_{rated} is the rated output power. The derived base current and impedance are

$$I_{base} = \frac{P_{base}}{\sqrt{3}V_{base}} \quad , \quad \text{and} \;\; Z_{base} = \frac{V_{base}}{\sqrt{3}I_{base}}. \tag{6.6}$$

The second step is to normalize the actual equations by the base values. For example, normalizing both sides of (6.4) by the defined V_{base}, normalizing current terms by the defined I_{base} and factoring out the base impedance, the per-unit representation is

$$V_{P_kN,P_kA}^{pu} = E_{Pka}^{pu} + \frac{L_k^{pu}}{\sqrt{3}}\frac{dI_{Pka}^{pu}}{dt} + \frac{R_k^{pu}}{\sqrt{3}}I_{Pka}^{pu} \tag{6.7}$$

The same normalization is applied for all other RLE branches from Fig. 6.2. The development is completed with the capacitor equation:

$$I_C = C\frac{dV_C}{dt} \tag{6.8}$$

where C is the capacitance of the high-frequency filter capacitor. Normalizing both sides of (6.8) by I_{base} and V_C by V_{base}, as well as collecting the terms using Z_{base}:

$$I_C^{pu} = \frac{\sqrt{3}C}{Z_{base}}\frac{dV_C^{pu}}{dt} = \sqrt{3}C^{pu}\frac{dV_C^{pu}}{dt}. \tag{6.9}$$

The per-unit equation is identical to the original equation only with the factor $1/\sqrt{3}$ appears with each per-unit inductance and resistance term, and the factor $\sqrt{3}$ appears with the per-unit capacitance term, as shown in Fig. 6.2. The back emfs of all phases are assumed to be identical. Therefore, each has the normalized amplitude of $\frac{\sqrt{2}}{k\sqrt{3}}$ with the appropriate phase shift.

6.1.4 Trade-off between the ac ports power imbalance and the dc-bus power ripple

The circuit shown in Fig. 6.2 captures both power ripple on the dc-bus and the amount of power delivered by each ac port. Quantification of these values requires the active-rectifier dc-output current I_{dc0}^{pu} and the per-unit dc-bus voltage V_{dc}^{pu}. Due to the base power being delivered at the dc bus, $V_{dc}^{pu}V_{base}I_{dc0}^{pu}I_{base} = P_{base}$. By definition (6.6), the product between the per-unit dc-bus voltage and the per-unit active-rectifier dc-side current is constant:

$$V_{dc}^{pu}I_{dc0}^{pu} = \sqrt{3}. \tag{6.10}$$

The dc-bus voltage is calculated to ensure the active-rectifier has sufficient dc voltage to operate. In the serially-connected system, each passive rectifier generates a dc voltage

$$\underbrace{V_{dc,i}^{pu}}_{i\,=\,2..k} = \underbrace{\frac{3}{\pi}\frac{\sqrt{2}}{k}}_{\text{back emf contribution}} - \underbrace{\frac{3}{\pi}\frac{\omega L_i^{pu}}{\sqrt{3}}I_{dc0}^{pu}}_{\text{commutation drop}} - \underbrace{2\frac{R_i^{pu}}{\sqrt{3}}I_{dc0}^{pu}}_{\text{resistive drop}}. \tag{6.11}$$

where ω is the rated electrical frequency [47]. The active-rectifier dc-side voltage must be the peak line-to-line back emf to maintain controllability under the space-vector-modulation scheme while minimizing the voltage rating, or

$$V_{dc,1}^{pu} = \frac{\sqrt{2}}{k}. \tag{6.12}$$

By KVL, the dc-bus voltage is

$$V_{dc}^{pu} = \sum_{i=1..k} V_{dc,i}^{pu}. \tag{6.13}$$

Substituting (6.11) and (6.12) into (6.13) as well as using (6.10), the per-unit dc-bus voltage follows:

$$V_{dc}^{pu} = \frac{\sqrt{2}}{k} + \frac{3}{\pi}\frac{\sqrt{2}}{k}(k-1) - \sum_{i=2..k}\left(\frac{3}{\pi}\frac{X_{Li}^{pu}}{V_{dc}^{pu}} + 2\frac{R_i^{pu}}{V_{dc}^{pu}}\right) \tag{6.14}$$

where $X_{Li}^{pu} = \omega L_i^{pu}$ represents the per-unit equivalent reactance of each phase in port i. The per-unit dc-bus voltage is calculated by solving the quadratic equation (6.14). The dc-bus average current is calculated using (6.10) to complete the parameters in Fig. 6.2.

Fig. 6.3 shows the dc-bus power ripple and the output power ratio between one passive port and the active port as a function of X_{Li}^{pu} using the per-unit circuit in Fig. 6.2. The results are generated assuming a four-identical-ac-port machine, i.e., $k = 4$, with $R_i^{pu} = 0.011$. The filter capacitor is $C^{pu} = 0.01$. As the per-unit reactance increases, the dc-bus power ripple decreases because the rate of current commutation in the ac port is reduced. In addition, less power is delivered through the passive rectifier because the output dc-bus voltage is reduced as the inductance increases, as shown in equation (6.11). Therefore, the ratio between the output power of the active port and that of the passive port increases.

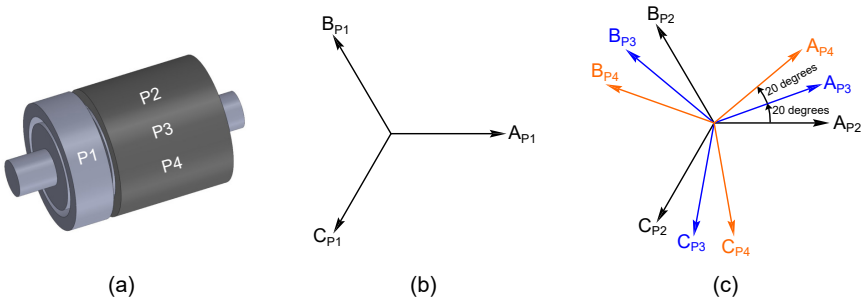


Figure 6.4: (a) An axially-split machine general configuration, (b) voltage vectors of the active-rectifier port P_1, (c) voltage vectors of passive-rectifier ports P_2, P_3, and P_4.

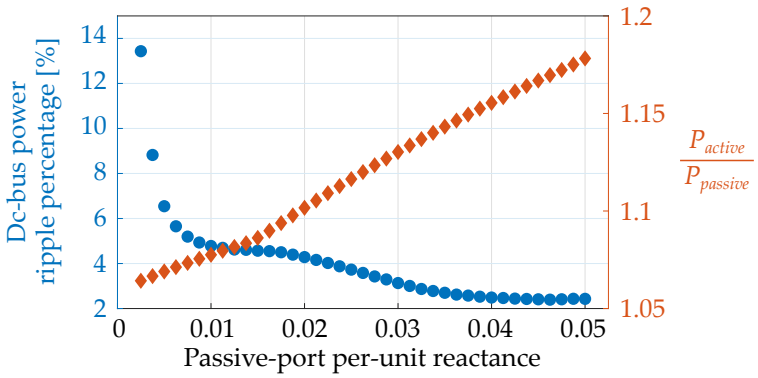


Figure 6.3: Consider a 4-port generator with $R_i^{pu} = 0.011$, and $C^{pu} = 0.01$. Dc-bus power ripple decreases as the per-port per-unit reactance increases. Simultaneously, the active rectifier delivers more power compared to the passive rectifier, expressed by the increasing trend of the orange diamonds.

6.2 An exemplary generator winding layout satisfying the inductance matrix requirement

This section proposes a winding layout that meets the inductance matrix requirement in Table 6.1 for a four-port generator. Fig. 6.4 shows a conceptual design, comprising two structures that are axially split. The left section creates one ac port powering the active rectifier. The right section creates three ac ports, 20-electrical-degree phase-shifted from each other, powering three passive rectifiers. The axial split eliminates the mutual inductance between the active-rectifier ac port and passive-rectifier ac ports. Mutual inductances among the passive-rectifier ac ports are eliminated by designing a winding layout based on fractional-pole-pitch coils.

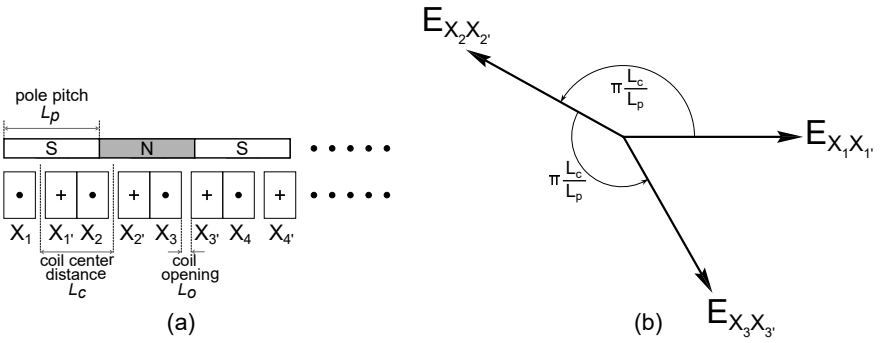


Figure 6.5: (a) Winding configuration of the passive-rectifier ac port. (b) The corresponding back emfs vectors.

6.2.1 Passive-rectifier port winding configuration

Non-overlapping fractional-pole-pitch coils are selected to achieve multiple passive-rectifier ac ports with appropriate phase shift and zero mutual inductance. The top view of the coil structure is shown in Fig. 6.5 with X denoting the going and X' denotes the returning coil side. Assuming the back emf on the coil X_1X_1' is

$$E_{X_1X_1'} = E_0 \cos(\omega t), \tag{6.15}$$

where E_0 is the amplitude and ω is the electrical frequency. The coil pitch, distance between two adjacent coil centers, is denoted by L_c and the pole pitch is denoted by L_p. The back emf of the k-th coil is:

$$E_{X_kX_k'} = E_0 \cos\left(\omega t - \pi(k-1)\frac{L_c}{L_p}\right) \tag{6.16}$$

where coil 1 is selected as the reference, e.g., having zero phase angle. Fig. 6.5(b) shows back emfs of coils 1, 2, and 3. Back emfs of other coils could also be expressed but are omitted for simplicity.

The relationship between the magnet pole pitch and coil pitch sets the machine periodicity [67]. The total magnet pitch and coil pitch must be the same to wrap the linear structure shown in Fig.

6.5 into a cylindrical structure. Therefore, the coil pitch and the magnet pitch are related by

$$nL_c = pL_p \tag{6.17}$$

where n is an integer and p is an even integer number, denoting number of coils and number of magnetic poles, respectively.

The phase windings are constructed by appropriately connecting the individual coils to achieve the voltage vectors shown in Fig. 6.4(c). For example, consider $\frac{L_c}{L_p} = \frac{26}{18}$. Using equation (6.16), the angular position of the k-th coil back emf is $(k-1)\pi\frac{26}{18}$ radian or $(k-1)260$ degrees. Using equation (6.17), the machine needs to have 18 coils and 26 poles, or an integer multiple of these numbers. All the back emfs cover 360 electrical degrees with any two adjacent vectors to be 20-electrical-degree apart, as shown in Fig. 6.6(a). The available back emf are connected to form three three-phase sets following Fig. 6.6(b). For example, phase A_{P2} is $E_1 - E_{10}$, formed by connecting coils X_1X_1' and $X_{10}X_{10}'$ in opposite polarity, as shown in 6.6(c). Similar connections are made to form other phases.

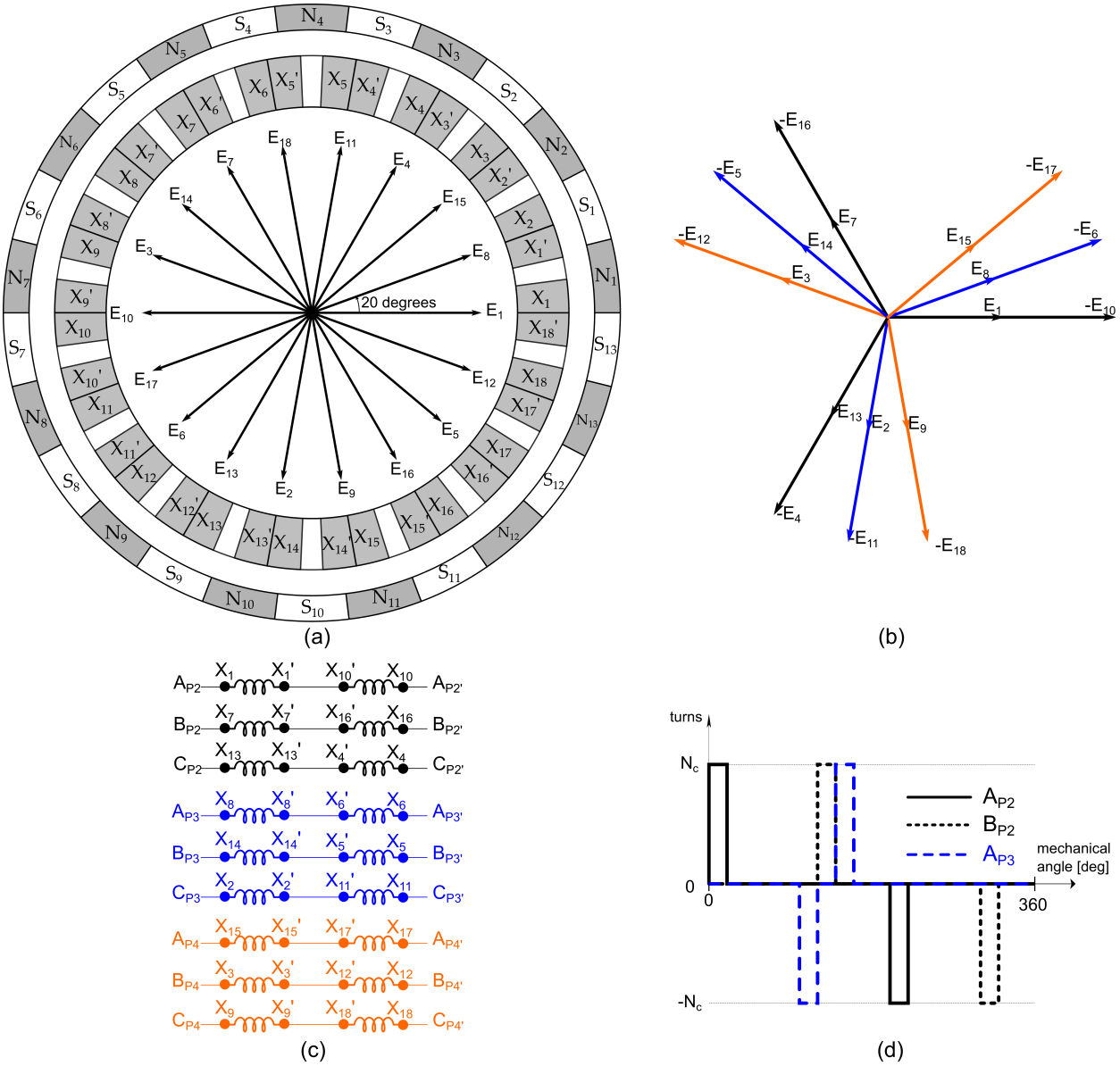


Figure 6.6: (a) A structure with $\frac{L_c}{L_p} = \frac{26}{18}$ and the associated available voltage vectors, (b) formation of three three-phase winding sets with 20-degree phase shift, (c) physical connection pattern, (d) non-zero part of the winding functions for different phases do not overlap.

The foregoing method for coil connection leads to zero mutual inductance. Mutual inductance between two windings depends on the average of the product between the two corresponding winding functions [68, 69]. Winding functions for phases A_{P2}, B_{P2}, and A_{P3} with the given connection pattern are shown in Fig. 6.6(d). The winding function for each phase consists of two non-zero, bi-polar intervals. In the proposed configuration, the product of any two winding functions is zero, leading to the zero mutual inductance. The inductance matrix corresponding to

the passive ports, matrix $\mathbf{L_{PP}}$, is diagonal, meeting the requirement in Table 6.1 with zero mutual M-terms.

6.2.2 Active-rectifier winding configuration

The active rectifier is axially split from the passive rectifier to eliminate the mutual coupling between the passive-rectifier phases and active-rectifier phases, i.e., all entries in the matrix $\mathbf{L_{AP}}$ are zero. A standard distributed winding is employed for the active-rectifier ac ports, as shown in Fig. 6.7(a). This winding approach results in a balanced three-phase back emf as shown in Fig. 6.7(b).

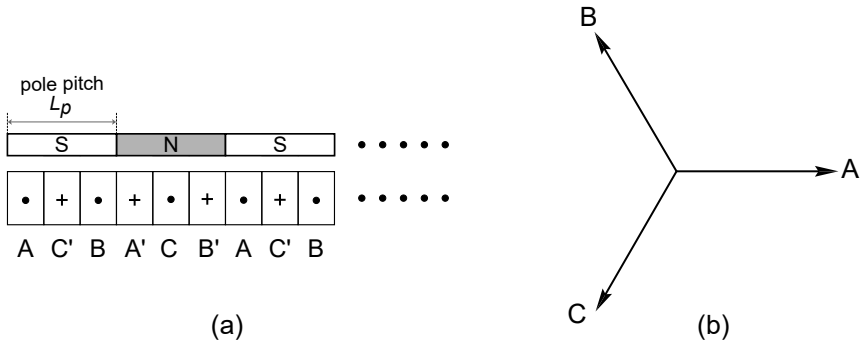
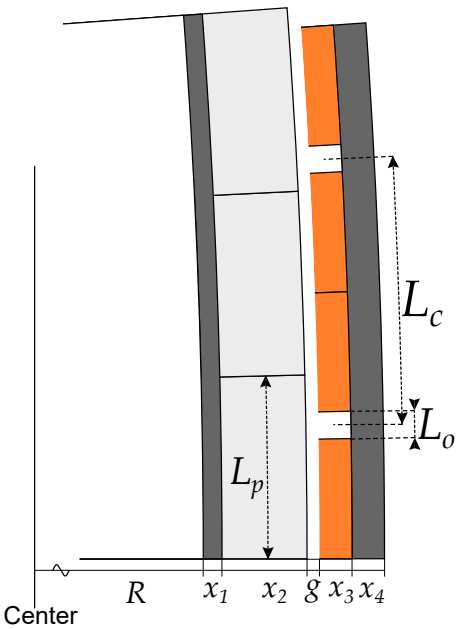


Figure 6.7: (a) Active-rectifier ac port winding configuration. (b) The corresponding voltage vectors.

Section 6.3 corroborates the feasibility of the proposed winding layout by showing the implementation using an FEA model of a 10 MW generator, suitable for offshore wind turbines. The FEA model is then coupled to a circuit simulator to verify the impact of magnetic coupling among the different phases on the dc-bus power ripple as well as the generator torque ripple.

6.3 FEA verification of the proposed winding layout for a 10 MW generator

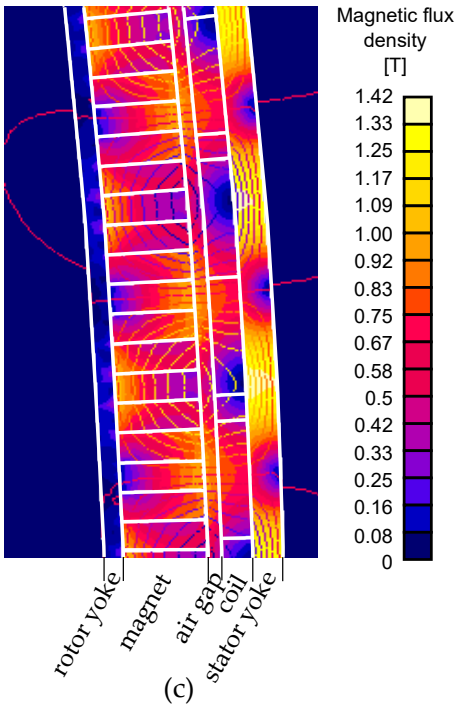
This section presents an FEA verification of the proposed generator topology. The design focuses on the passive rectifier portion because of the non-conventional winding configuration. A generator design is first created using Altair Flux^{TM} following the structure shown in Fig. 6.8(a). For the direct-drive generator, the inner rotor radius R is preferred to be as large as possible to increase



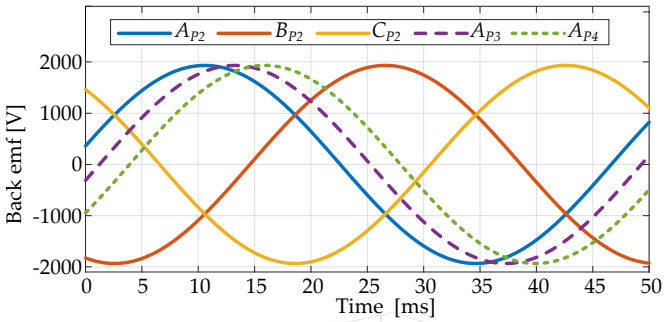
(a)

Quantity	Notation	Unit	Value
Magnet pole pitch	L_p	mm	147
Center-coil distance	L_c	mm	213.6
Coil-opening pitch	L_o	mm	22
Stack length	L_s	mm	1250
Rotor inner radius	R	mm	6000
Rotor yoke width	x_1	mm	15.6
Magnet width	x_2	mm	68
Air-gap width	g	mm	12
Coil width	x_3	mm	25.7
Stator yoke width	x_4	mm	25.7
Number of poles	N_p		260
Number of coils	N_c		280
Phase peak back emf	E_i	V	1934
Rated frequency	f_0	Hz	20.8
Base voltage	V_{base}	V	9475
Base power	P_{base}	MW	10
Base impedance	Z_{base}	Ω	9
Dc-bus voltage	V_{dc}	kV	11.5
Dc-bus current	I_{dc0}	A	869
Phase reactance	X_{Li}^{pu}	pu	0.043
Phase resistance	R_i^{pu}	pu	0.011
Filter capacitance	C	mF	90

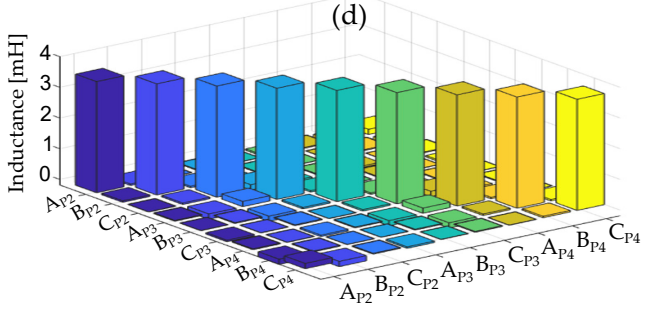
(b)



(c)



(d)



(e)

Figure 6.8: FEA verification of the proposed structure in Fig. 6.6: (a) Configuration of the generator FEA model. (b) Generator dimensions and the corresponding electrical quantities. (c) Flux density of the FEA model. (d) The induced back emf that has 120-degree shift between phases in the same port and a 20-degree phase-shift among different ports. (e) The inductance matrix is dominated by diagonal elements —self inductance— showing the magnetic decoupling between different phases.

the generator tip speed, thereby improving the power density. Due to the transportation limitation, a six-meter radius is the practical constraint. The airgap length is chosen to be 12 mm, following the design rule by the National Renewable Energy Laboratory (NREL) [70]. 260 poles are chosen for convenience because one fundamental period of the machine requires 26 poles. This selection leads to the pole pitch of 145 mm, well within the range reported by NREL [70]. Each group or 26 poles corresponds to 18 stator coils to form the back emf vectors as shown in Fig. 6.6(a).

For each group of 18 consecutive coils, the connection pattern laid out in Fig. 6.6 is implemented to form nine phases. The same phase from each of the ten periods is serially connected to form the complete one machine phase. The generator rated speed is chosen to be 9.6 rpm, typical for 10-MW direct-drive wind turbines. The current density is set as 4 A/mm^2 to facilitate air cooling. The magnets are Halbach type to reduce the rotor yoke size. The magnet thickness is selected to achieve 0.045 pu phase reactance. Using equation (6.14), the dc-bus voltage is 1.2 pu assuming $R_i^{pu} = 0.011$. As the dc-side voltage of the active rectifier is 0.35 pu, according to constraint (6.12), the active rectifier provides 2.9 MW of the total 10 MW power. The stack length is calculated for the passive-rectifier section to provide 7.1 MW. The dimensions are summarized in Fig. 6.9(b) and flux density of the structure is shown in Fig. 6.9(c).

Back emfs of port P_1, phase A of port P_2 and P_3 are shown in Fig. 6.8(d), confirming the desired 120-electrical-degree phase shift between phases in the same port and 20-electrical-degree phase shift between different ports. Fig. 6.8(e) shows the inductance matrix measured from the FEA model. The proposed connection pattern eliminates the mutual coupling between different phases, as seen by the dominance of diagonal matrix elements.

A circuit simulation is created following Fig. 6.2 with the ac ports replaced by the Altair Flux^{TM} FEA model to evaluate the generator performance in the presence of the power electronics. Electrical parameters are calculated based on the back emf produced by the FEA model as shown in Fig. 6.8(c), the measured inductance as shown in Fig. 6.8(d), the base power of 10 MW, and the equations in Section 6.1. Parameter values are summarized in Fig. 6.8(b).

The FEA verification shown in Fig. 6.9 confirms feasibility of the proposed generator configuration. The currents in port P_1 are shown in Fig. 6.9(a). The small ripple component during the conduction period of each phase is due to the phase-shifting effects. There is no substantial perturbation due to mutual coupling between different phases. The dc-bus current is shown in Fig. 6.9(b)

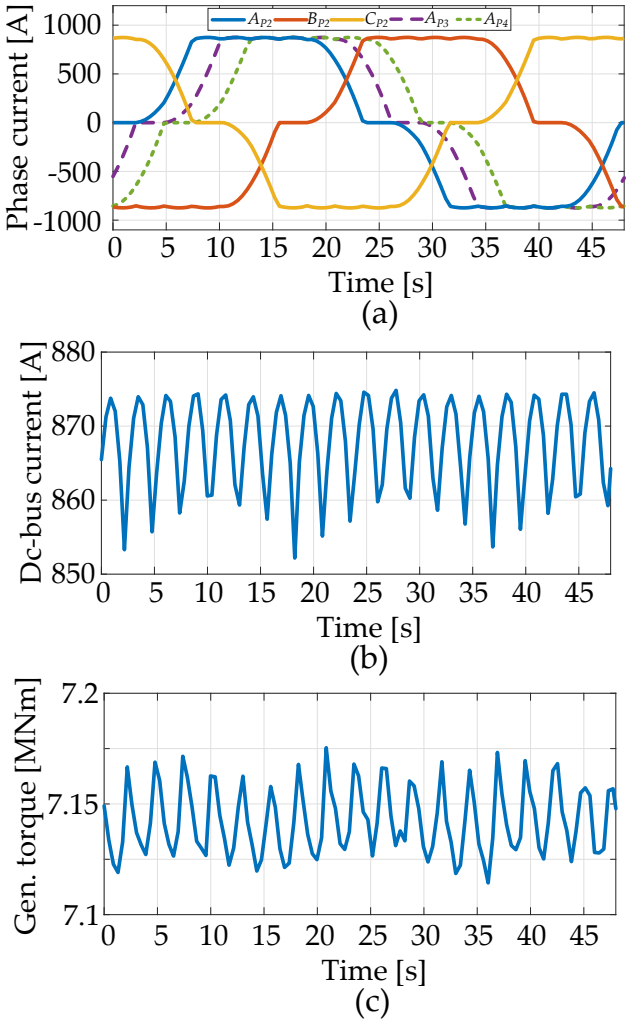


Figure 6.9: Current and torque characteristics: (a) Currents in the passive rectifiers are trapezoidal and phase shifted. (b) Dc-bus current has 2.4% peak-to-peak ripple at 18 times the fundamental back-emf frequency. (c) The peak-to-peak torque ripple is 0.86% of the average value.

with the ripple component at 18 times the back-emf fundamental frequency. The peak-to-peak ripple is 2.6% of the average current value, which agrees with the prediction using the per-unit circuit for the case $X_{Li}^{pu} = 0.047$, as shown in Fig. 6.3. The generator instantaneous torque is shown in Fig. 6.9(c). The peak-to-peak torque ripple is measured as 0.86% the average value. Next, Section 6.4 shows an experimental verification to further corroborate the proposed winding layout.

6.4 Experimental results

6.4.1 Experimental setup

A low-power experimental setup was developed to verify the proposed generator topology, as shown in Fig. 6.10. The generator includes two assemblies, which are modified Samsung DC96-01218D PM motors mounted on custom-built frames. The original stator has 36 coils as shown in Fig. 6.10(b).

The assembly that powers the passive rectifier needs to provide a set of back emfs as shown in Fig. 6.4(c). The requirement is met with a custom-built 34-pole rotor. The magnets are enclosed by retaining rings, as shown in Fig. 6.10(c). The whole assembly is embedded inside the rotor frame, as shown in Fig. 5.12(d). Combined with the 36-coil stator, the modified machine has $L_c/L_p = p/n = 17/18$, according to equation (6.17) with $n = 36$ and $p = 34$. The phase difference between the back emfs of two consecutive coils is $\pi\frac{L_c}{L_p}$ or 170 degrees, following equation (6.16). As the 170-degree phase difference between two consecutive coils repeats 36 times, the 360-degree interval is covered by vectors that are 10 degrees apart, as illustrated in Fig. 6.10(e). The coil connection pattern to form the required three three-phase sets with a 20-electrical-degree phase-shift is shown in Fig. 6.10(f). Each phase is formed by serially connecting four coils, including out-of-phase pairs to eliminate mutual inductance. For example, phase A_{P1} is formed by serially connecting coils 1 and 18 in the same polarity and coil 19 and 36 in the opposite polarity. As a result, the total back emf is $E_{AP1} = E_1 + E_{18} - E_{19} - E_{36}$. Other phases are constructed in a similar manner.

Fig. 6.6(g) shows the complete experimental setup. The generator includes two assemblies S1 and S2. The S1 is the original machine with 48 magnetic poles powering the active rectifier Rec-1.

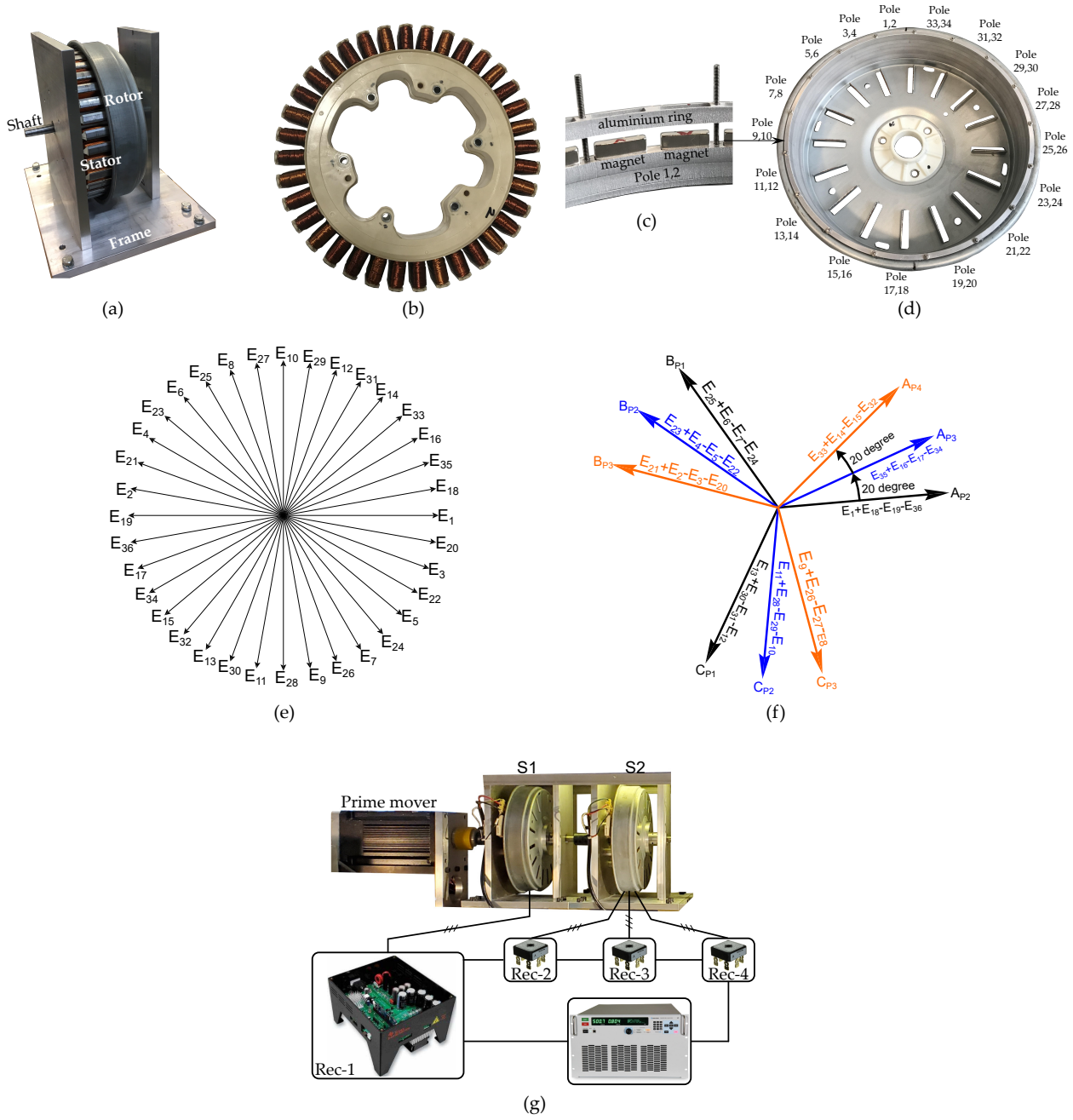


Figure 6.10: Experimental setup: (a) machine assembly, (b) stator with 36 coils, (c) assembly view of the magnet ring, (d) complete magnet ring mounted on the original rotor frame, (e) back emf vectors of the 36-coil 34-pole combination, (f) connection pattern to achieve three three-phase sets shifted by 20 electrical degrees from each other, (g) complete experimental setup.

The assembly S2 is the modified machine with 34 magnetic poles to form three phase-shifted ac ports. The three ports power three passive rectifiers, namely Rec-2, Rec-3, and Rec-4. Dc outputs of the active and the active rectifiers are serially connected to deliver power to a resistive load.

6.4.2 Generator characteristics

The experimentally measured back emfs of the modified machine verify the space vectors in Fig. 5.12. The back emfs of individual coils 1, 2, 3, and 4 are shown in Fig. 6.11(a). Back emfs of two consecutive coils (e.g., 1 and 2, or 2 and 3, etc.) are phase-shifted by 170 degree, as predicted by equation (6.16). The connection pattern in Fig. 5.12(f) is implemented. Back emfs of phases A_{P2}, A_{P3}, and A_{P4} are recorded in Fig. 6.11(b), showing a 20-degree phase shift between different ac ports. In addition, the back emfs of phases A_{P2}, B_{P2}, and C_{P2} in Fig. 6.11(c) show a 120-electrical-degree phase-shift within the same ac port.

The inductance matrix of the assembly S2 has dominant diagonal elements, as visualized in Fig. 6.11(d) The diagonal matrix verifies that the proposed generator configuration satisfies the RLE model (see Table 6.1) and is appropriate to use in the integrated generator-rectifier system to reduce the dc-bus voltage ripple without requiring the bulky filter capacitors.

6.4.3 Integrated generator-rectifier operation

The ac-dc conversion using the integrated generator-rectifier system is illustrated in Fig. 6.12. The outputs of the rectifiers are serially connected and deliver power to a resistive load. The prime mover turns the generator at 150 rpm and the load is set to 1500 Ohm. The active rectifier regulates sinusoidal current in the corresponding ac port and operates at unity power factor to minimize the volt-ampere rating. Fig. 6.12(a) shows the active rectifier phase-A current.

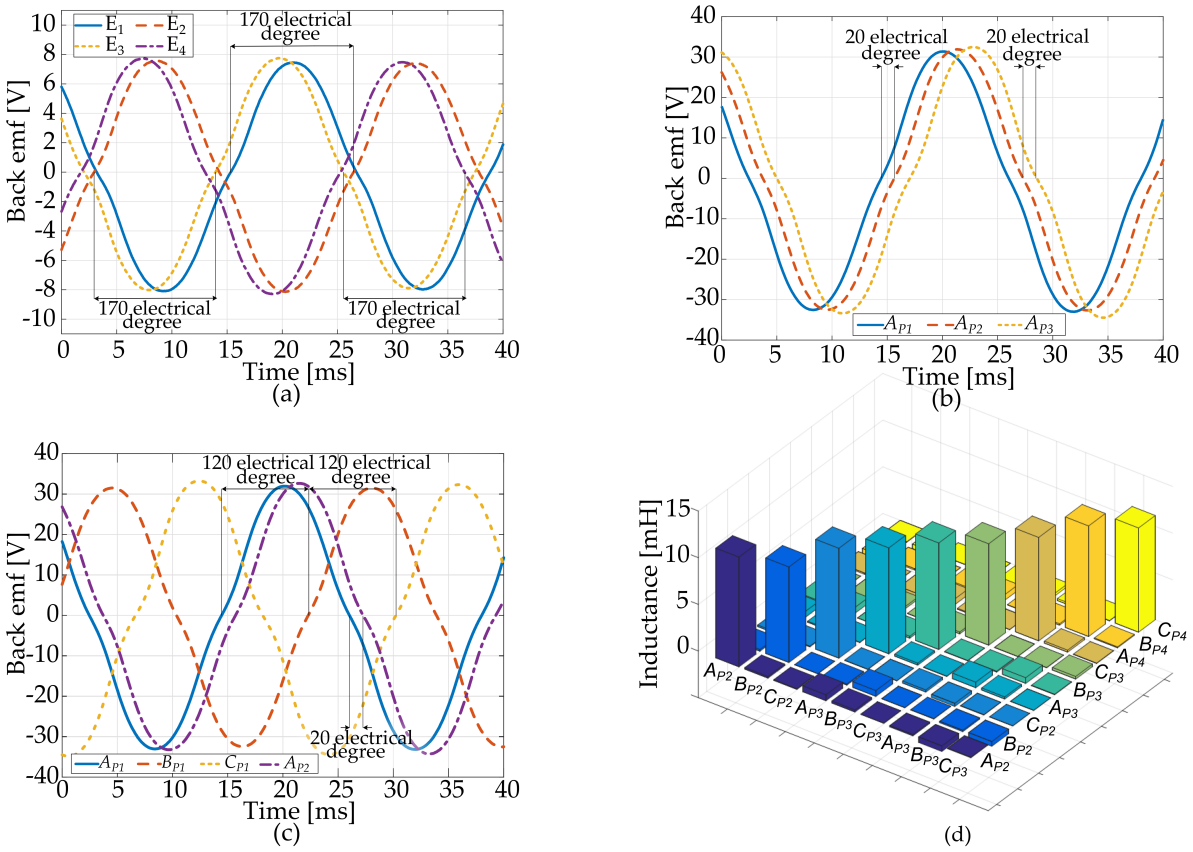


Figure 6.11: Electrical characteristics of the fractional-pole-pitch machine. (a) The consecutive coils shows 170-degree electrical phase shift. Connection patterns in Fig. 5.12(f) result in (b) back emfs of phases A_{P2}, A_{P3}, and A_{P4} being phase-shifted by 20 electrical degrees from each other; and (c) back emfs of phases A_{P1}, B_{P1}, and C_{P1} being phase-shifted by 120 electrical degrees from each other.

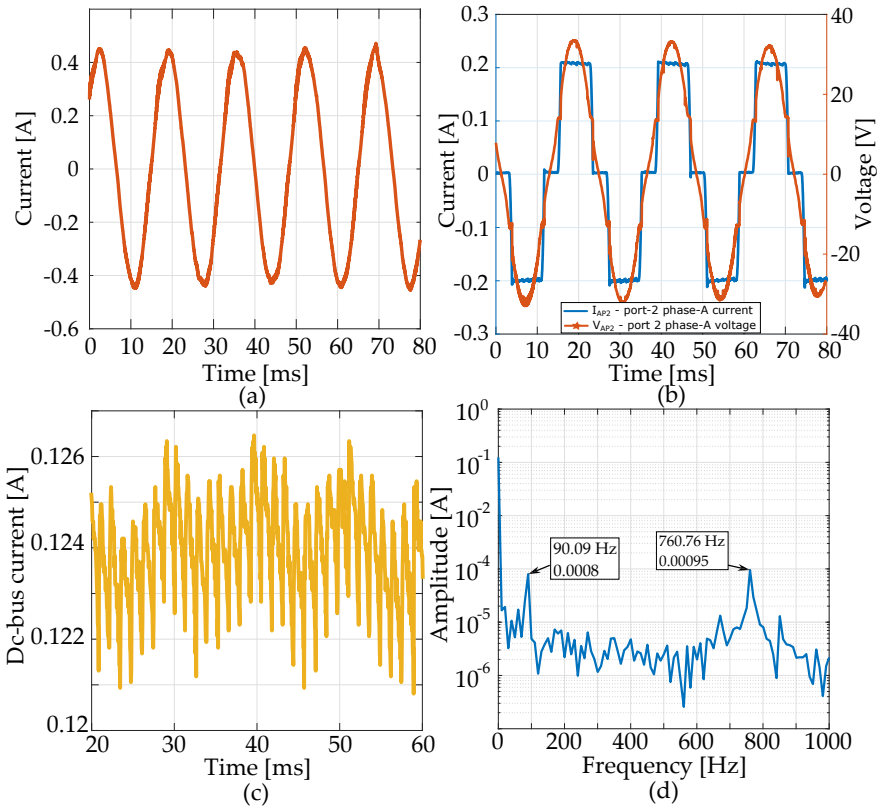


Figure 6.12: Electrical characteristic of the integrated generator-rectifier system. (a) Current is sinusoidal in the active port. (b) While the passive port back emf is sinusoidal, the phase current is trapezoidal due to operation of the capacitor-less diode bridge. (c) The dc-bus experiences a low ripple current.

Dc-side current of the active-rectifier sets the current in the passive-rectifier ac ports [65]. Fig. 6.12(b) shows the current and voltage (relative to the neutral point) of port-2 phase-A. The current is trapezoidal because of the diode-bridge operation, closely mimics the simulation results in Fig. 6.12(a). The voltage and current are in phase due to elimination of the dc-side filter capacitor. The calculated power factor is 0.95, mostly due to the distortion factor.

Although the filter capacitors are eliminated, the dc-bus current has a very low ripple component due to the phase shift between different passive rectifier ac ports, as shown in Fig. 6.12(c). There are two observable ripple components, one at 90 Hz and another one at 760 Hz –18 times the line frequency, as shown in Fig. 6.11(d). The first one is due to the generator imperfections, as shown by slight imbalance between back emfs in Fig. 6.11, while the second component is due to the back-emf phase shifting. A better construction of the machine would eliminate the first factor, resulting in a lower dc-bus power ripple. The total dc-bus current peak-to-peak ripple is 4.3% of

the average value.

6.5 Conclusions

This chapter proposes a generalized framework to quantify the effect of interaction between power electronic converters and a multi-port generator using an inductance matrix. Constraints on this matrix ensure the isolated RLE model's validity from a control and design perspective, even when the generator ports are magnetically coupled. A trade-off is shown between the dc bus power ripple and the power imbalance between the generator's active and passive ports. Intuitively, a higher generator inductance causes more voltage drop during the diode commutation leading to lower power being delivered by the passive ports. In contrast, a lower generator inductance increases the current commutation slope, resulting in a higher dc bus power ripple. A 10 MW design using an exemplary winding layout shows the accuracy of the generalized framework. Further, a laboratory prototype using a fractional-slot winding proves the decoupling between different generator passive ports even when they locate on the same generator's magnetic structure. Table 6.1 can be used as a guideline to create new winding layouts suited for the integrated generator-rectifier systems.

Chapter 7

IMPROVEMENT IN THE ANNUAL ENERGY PRODUCTION USING THE INTEGRATED GENERATOR-RECTIFIER SYSTEM

Ultimately, the integrated generator-rectifier system must improve the economic figures of merit. This chapter focuses on annual energy production (AEP) in offshore wind applications because the evaluation does not rely on fictitious assumptions. The procedure to pair generators and rectifiers is first discussed to facilitate the AEP calculation.

7.1 Per-unit generator reactance as the handshake parameter

A conventional approach typically pre-defines the terminal voltage to ensure the compatibility between the generator and the power electronics designs. In contrast, the pairing in the integrated generator-rectifier system is based on the per-unit generator inductance. From the power-electronics design perspective, the generator per-unit reactance X_L^{pu} is the most critical parameter on which the whole design process relies, as discussed in Chapter 3. For example, this parameter sets the per-unit dc-bus voltage, as shown by equation 3.6. In addition, it determines the number of ac ports to minimize the active-rectifier VA rating, as illustrated by Fig. 3.5.

From the generator perspective, the per-unit reactance is independent of the stack length and the number of turns in each coil once other dimensions are fixed. The stack length is freely chosen to set the power level. The number of turns is freely chosen to match the voltage requirement from the power electronics. To explain the independence, consider a three-phase generator that has N turns per coil, L_s stack length, and P_{base} output power, and operates at the rated electrical frequency ω_0. This generator has an per-phase inductance of L, an rms line-line voltage V_{base}. The

per-unit reactance is defined as

$$X_{pu}^{L} = \frac{\omega_0 L P_{base}}{V_{base}^2}. \tag{7.1}$$

The inductance L is proportional to N^2 and L_s while the power P_{base} is proportional to L_s. Therefore, the numerator of equation (7.1) is proportional to $N^2 L_s^2$. In the denominator, the voltage is proportional to the product of N and L_s. As a result, the denominator is proportional to $N^2 L_s^2$. These properties of both the numerator and denominator makes the generator per-unit inductance independent of the output power level and the terminal voltage.

From the system design perspective, generator and rectifier can be co-designed based on a common per-unit reactance. The generator stack length and the power-electronics switches are later chosen based on the required power level. The base voltage of the generator is then calculated based on the chosen switch voltage rating and a desired safety margin. The number of turns in each generator's coil is finally calculated to match the base voltage requirement.

7.2 System design example

This section creates a 10 MW, 9.6 r/min, direct-drive, integrated generator-rectifier system for an offshore wind turbine. The rated power and speed are chosen based on ongoing trend in the industry [71].

In the intial generator-design stage, a slotless topology with Halbach-array NdFeB magnets is being considered, as shown in Fig. 7.1. This topology can be designed to have a low inductance, which is preferred for the integrated generator-rectifier system to limit the imbalance in power processed by the active and the passive rectifiers. Four geometric variables are chosen to set up the multi-objective optimization along with their bounds, $x_1 ... x_4$, as shown in Table 7.1. An airgap length of 10 mm is selected, because it is common at these power levels [72–75]. Number of poles is selected to be 240. Boundaries for the shaft radius x_1 are picked to ensure the generator size does not exceed the transportation size limit. The current density limit J is chosen to ensure that forced air cooling is sufficient. A flux-density limit of 1.8 T is considered as the magnetic saturation limit. Each electromagnetic design is reinforced by a mechanical structure designed to

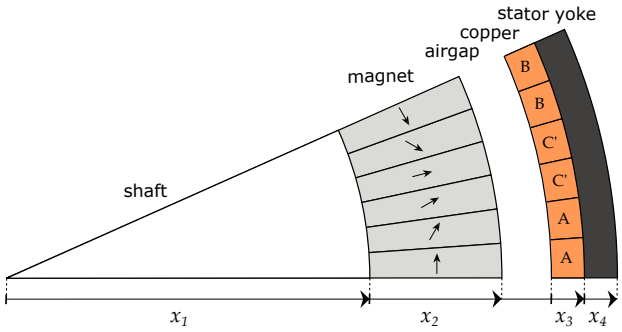


Figure 7.1: Geometric parameters used for optimization of the slotless generator.

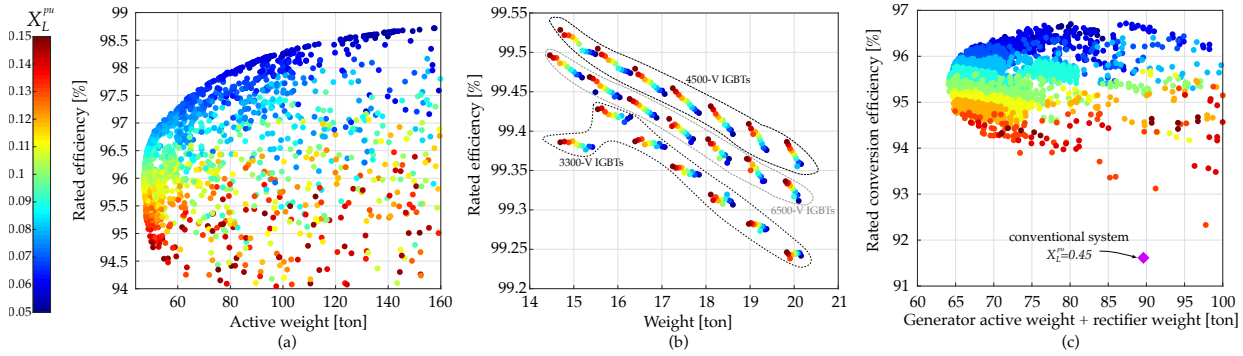


Figure 7.2: Weight versus efficiency characteristic of the designed (a) generators, (b) rectifiers, and (c) integrated system for different X_{pu}^{L} values.

have a gravitational airgap deflection less than 10% the nominal length and a torsional deflection of less than 0.05^o.

Figure 7.2(a) shows the optimization results for the initial generator-design stage. Each design point is accompanied by an X_L^{pu}, which is shown by the color bar. As expected, the feasible design space shows the classic trade-off between the generator efficiency and the active weight. The design points with lower X_L^{pu} use thicker magnets. Thus, the required current density is reduced to meet the rated power, which leads to a higher efficiency. For example, a feasible generator design could weigh 55 tons with a rated efficiency of 97%. In comparison, a conventional design weighs 67 tons with a 93.5% rated efficiency [72].

The next step is to design the power electronic converter for a compatible X_L^{pu}. From an active-rectifier topology selection perspective, a three-level neutral-point clamped converter is chosen to balance complexity and conversion efficiency. This topology is a typical industry choice for megawatt-scale power converter [76]. The selection of the minimum generator speed is an influ-

Table 7.1: Variable and constraints for slotless-NdFeB generators.

Variable	Notation	Unit	Lower bound	Upper bound
Shaft radius	x_1	mm	5000	6000
Magnet thickness	x_2	mm	10	70
Copper thickness	x_3	mm	25	100
Stator yoke thickness	x_4	mm	10	60
Current density	J	A/mm^2	1	4
Stator flux density	ψ_s	T	-	1.8

encing parameter that trades off the active rectifier VA rating with the annual energy production. In the proposed co-design, the minimum speed is varied between 0.25 pu and 0.55 pu to capture this effect. The 0.25 pu value corresponds to the 3 m/s cut-in speed normalized by the 12m/s rated wind speed for a typical offshore wind site [77]. A typical minimum speed for a conventional DFIG system, which exhibits similar trade-offs [3], is 0.55 pu.

Three types of IGBTs are investigated for the active rectifier design: 3300 V, 4500 V, and 6500 V. A Simulink model is created to determine the voltage and current waveforms across each power electronics switch. These waveforms are combined with the losses characterization from the datasheet to estimate the conversion losses. The active-rectifier weight is estimated using a specific power of 0.55 kVA/kg [76]. The passive rectifier is assumed to have five times higher specific power. Fig. 7.2(b) shows the power electronics design in terms of weight and rated efficiency for a corresponding X_L^{pu}.

In contrast to a conventional trade-off characteristic between power density and efficiency in the power converter design, the proposed co-design shows a lower weight corresponding to a higher efficiency design. A lower-weight system is the result of a narrower operating speed range, which allows a higher dc-bus voltage. Therefore, the current required to deliver an identical power is reduced. The total conversion losses are lowered because the conduction loss is proportional to square of the current while the switching losses remain unchanged. For example, an attainable power-electronics design for any X_L^{pu} could exceed 99.5% conversion efficiency while weighing less than 15.5 tons. To put these numbers in perspective, a conventional, off-the-shelf, three-level full-power-rated converter has a conversion efficiency and weight of 97.9% and 22.7 tons,

respectively [76].

The generator and power electronic designs for an identical X_L^{pu} are next assembled to compute the overall system weight and efficiency as illustrated in Fig. 7.2(c). Comparing the plausible designs of the proposed architecture with a reference design [72], shown by the diamond-purple marker, a reductions of 25 tons and a 61% conversion losses are achievable. As a final step for the co-design, the generator number of turns are computed for each attainable design point.

7.3 Annual energy production

The electrical power output of a wind turbine as a function of the wind speed is essential for AEP calculation. The wind-turbine mechanical power depends on wind and rotational speeds, as illustrated in Fig. 7.3 for a 10-MW wind turbine. At each wind speed, the maximum mechanical power should be extracted. For a direct-drive system, maximum power extraction requires the per-unit generator speed and per-unit wind speed to be identical, as marked by the green stars in Fig. 7.3. In an integrated generator-rectifier system, the minimum generator speed may not be identical with the per-unit cut-in wind speed, because expanding the speed range increases the volt-ampere rating of the active rectifier [35]. A minimum generator speed should be judiciously selected to balance the rectifier cost and additional benefits of extending the speed range. When the wind speed is lower than minimum generator speed, the generators must be forced to rotate at the minimum speed and extract the amount of power marked by orange stars in Fig. 7.3.

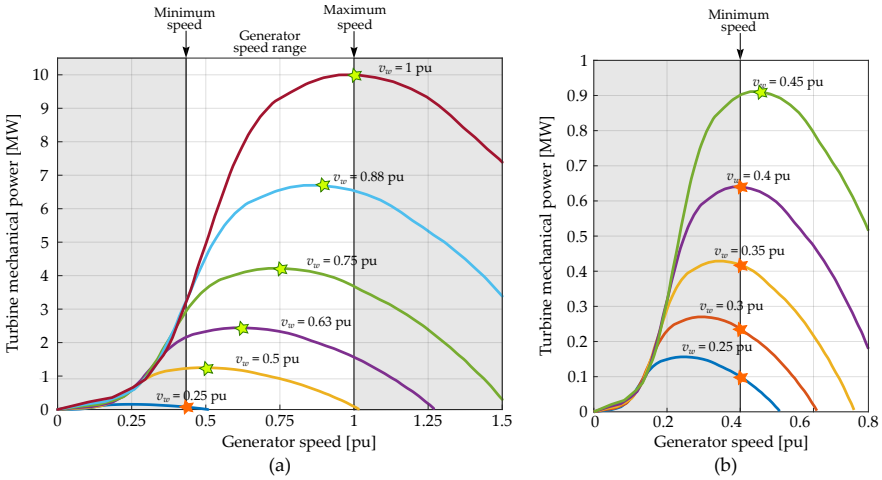


Figure 7.3: (a) Mechanical power versus rotational speed of a 10-MW wind turbine. (b) Magnified section of the mechanical power at low wind speeds. The wind speed is normalized by the rated value, typically 12 m/s for offshore wind.

The generator and rectifier conversion efficiency translates available mechanical power to electrical-power output. At partial-speed conditions, conversion efficiency is different from that at the rated condition. For example, Fig. 7.4 illustrates the conversion efficiencies of rectifiers and generators with a speed range from 0.4 to 1 pu for a typical conventional system and an integrated generator-rectifier system. The product of the power electronics and the generator efficiency curves is the system mechanical-to-electrical power conversion efficiency, as illustrated by the solid-yellow curves.

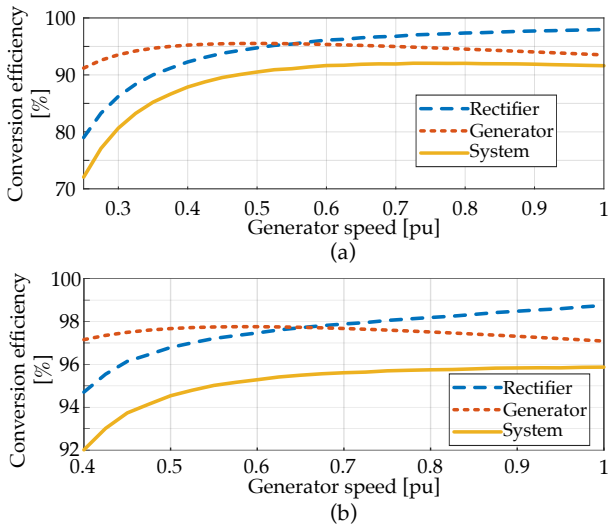


Figure 7.4: Conversion efficiency of (a) a conventional full-power-rated rectifier [72], and (b) a sample design of the integrated generator-rectifier system as a function of generator speed.

Information about wind-speed probability distribution is essential for the AEP computation. As an example, the wind-speed probability of the Buoy 44028, off the coast of Massachusetts is used [77]. Annual energy production ϵ is calculated by

$$\epsilon = A_v \mathbb{E}\big[P_e(v_w)\big], \tag{7.2}$$

where A_v is the wind turbine availability, $\mathbb{E}$ is the expected value operator, P_e is the output electrical power as a function of wind speed v_w. Fig. 7.5(a) shows the AEP based on the integrated generator-rectifier systems assuming $A_v = 1$. For the same weight, the integrated generator-rectifier system could increase the annual energy production by 5.2% compared to the conventional system, from $26,700$ MWh/year to $28,100$ MWh/year. At point A on the Pareto front, the total weight is reduced by 25%, from 89 to 67 tons, while the energy yield is increased by 4.5%, from $26,700$ MWh/year to $27,900$ MWh/year. Similar comparisons are illustrated in Fig. 7.5(b,c) for Buoy 46063 (California) and 51001 (Hawaii). In all the cases, the integrated generator-rectifier system improves the AEP, promising to reduce the overall levelized cost of electricity.

7.4 Conclusions

This chapter explains the per-unit generator reactance X_L^{pu} as the handshake parameter between the generator and the integrated rectifiers. A per-unit handshake parameter allows the design procedure to be independent of the voltage and power levels. Once a generator is paired with a rectifier system, the stack length, the number of turns in each phase, and the actual power electronics switch are selected to meet the actual power and voltage requirement. An exemplary design process is carried out at a 10-MW power level using three popular high-power IGBT types. AEP evaluation using the feasible generator-rectifier systems based on the wind profile at multiple locations highlights an economic benefit due to the integrated systems' improved conversion efficiency.

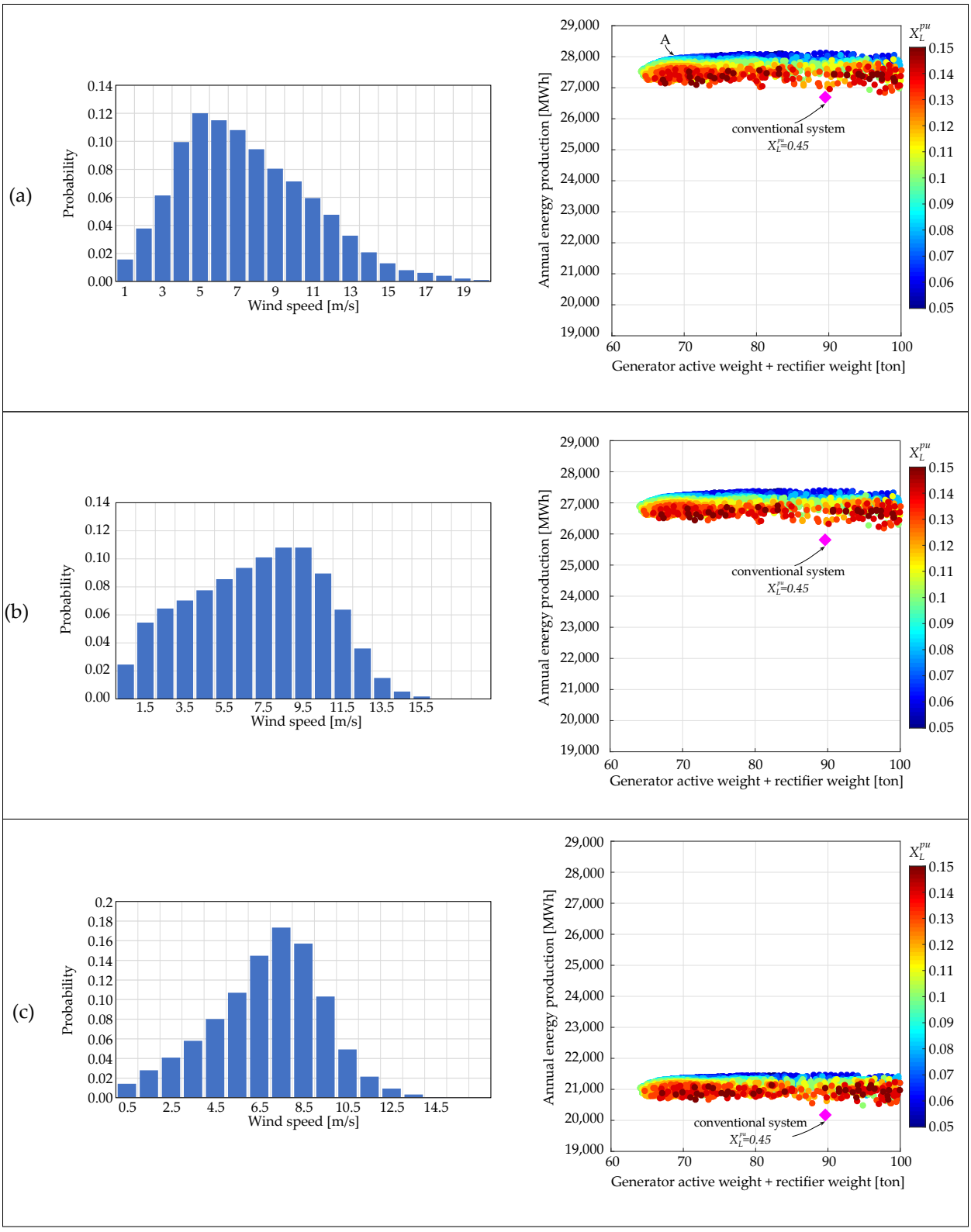


Figure 7.5: Annual energy production of the integrated generator-rectifier system with the accompanying wind-speed probability distribution at: (a) Buoy 44028 (Rhode Island), (b) Buoy 46063 (California), and (c) Buoy 51001 (Hawaii).

Chapter 8

CONCLUSIONS AND POTENTIAL RESEARCH DIRECTIONS

8.1 Conclusions

This dissertation proposes an integrated generator-rectifier system and shows the technical feasibility of performing high-power ac-to-dc conversion. The proposed system relies on multi-port PMSG and series stacked active and passive rectifiers. Dc-output of one active rectifier is serially connected with multiple passive rectifiers to form a relatively high-voltage dc bus, compared to the individual rectifier voltage rating. Most of the power is processed on high efficient diode bridges, leading to conversion-efficiency improvements. Reliance on diodes eliminates the need for gate driving circuits, sensors, and control boards—these features, together with the diode's low failure rate, increase the overall system reliability. The design process and quantification of potential benefits, such as conversion efficiency improvement and active-rectifier size reduction, are discussed in Chapters 2 and 3.

Filter capacitors in the passive rectifiers are eliminated by creating appropriate phase shifting between the ac-port back emfs or actively controlling the active rectifier. The first approach requires a special generator design. The second solution requires injection of harmonic into the active-rectifier d-axis current, as discussed in Chapter 4. Lead-lag and proportional-resonant controllers are utilized to create a closed-loop active voltage ripple compensator. The compensator extracts the ripple voltage at a selected frequency from the passive-rectifier output. A ripple d-axis current command is generated to create an active-rectifier voltage ripple opposite to the passive rectifiers. Elimination of filter capacitor gets rid of a reliability weak point and further improves the overall system compactness.

Having an active rectifier in the series-stacked architecture allows control of the total generator output power, leading to practical applications. In grid-forming applications, the active rectifier

regulates the total dc-bus voltage. The dc-side is set to the voltage difference between the dc-bus reference and passive-rectifier dc-side. A controller architecture is proposed in the second half of Chapter 4 to simultaneously achieve dc-bus voltage ripple correction and average value regulation.

In wind energy, the dc-bus voltage is stiff due to connection to a dc grid or an ac-grid-tie converter. This condition allows the active rectifier to be controlled as a current source. Due to the rectifier's series connection, regulation of the active-rectifier dc-side current directly regulated the dc-bus current and, consequently, the total output power of the generator. As a result, the generator output power could be set as a function of the rotational speed. This capability leads to maximum power-point tracking of the wind turbine as detailed in Chapter 5.

From the control perspective, an integrated generator-rectifier system requires all the generator phases to be represented by a resistor, an inductor, and a back emf source, all in series (RLE model). The generator winding layout would typically lead to mutual magnetic coupling –represented by mutual inductances– among different phases due to a shared magnetic structure. General requirements on the generator inductances are derived in Chapter 6 to ensure the RLE model's validity even in the presence of the magnetic coupling. These requirements guide the future development of generators compatible with the integrated rectifiers to enhance the overall system power density further.

Finally, the integrated generator-rectifier system benefits are quantified in offshore wind applications' annual energy production. The calculation shows improvement in the amount of harvesting energy considering the wind profiles at multiple locations. These figures corroborate the potential of the integrated system in making offshore wind energy resources economically viable.

8.2 Potential Research Directions

This dissertation covers the design and control fundamentals for the integrated generator-rectifier systems and reveals the potential benefits in offshore-wind applications. Based on this foundation, additional research topics could be explored to realize the potential fully. Some of the research directions are

- **System power density enhancement**: A light electro-mechanical conversion system would

reduce the wind-turbine supporting structure's requirements, the most cost-dominant component. Innovation in the generator design will play an essential role because it is the heaviest in the electro-mechanical conversion system. The theoretical analysis in Chapter 6 points out the generator's inductance requirements to be successfully integrated with the rectifiers. This finding guides the future high-power-density generators development to reduce the offshore wind turbine investment cost.

- **Balancing output power of the passive and active rectifiers**: Chapter 6 points out that the active rectifier delivers more output power than the passive rectifier even though the ac ports are identical. This condition means the ac port for the passive rectifiers is underutilized. Equal utilization of all the ac ports could potentially improve the overall system power density.

- **Back emf shaping**: The current in the passive-rectifier ac port features by trapezoidal shape as shown in Chapter 5 and 6. From the power extraction perspective, the third current harmonic in the trapezoidal current is not useful because the back emf is purely sinusoidal. However, the amplitude of the third harmonic is not negligible. Change the back emf shape to take advantage of the third-harmonic current for power extraction would constitute an interesting research direction. Preliminary evaluation shows trapezoidal back emf as a potential candidate [78].

- **Reliability and economic assessments**: The system reliability is likely to exceed the conventional system because the highly-reliable diodes process most of the power. Besides, the cost of the converter is expected to be reduced due to a smaller-size active rectifier. Research on reliability and economics is essential to unveil all the potential of the integrated generator-rectifier system.

BIBLIOGRAPHY

[1] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," *Proceedings of the IEEE*, vol. 103, no. 5, pp. 740–788, May 2015.

[2] C. Meyer, M. Hoing, A. Peterson, and R. W. D. Doncker, "Control and design of dc grids for offshore wind farms," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1475–1482, Nov 2007.

[3] R. Pena, J. C. Clare, and G. M. Asher, "Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind-energy generation," *IEE Proceedings - Electric Power Applications*, vol. 143, no. 3, pp. 231–241, May 1996.

[4] H. Polinder, F. F. A. van der Pijl, G. J. de Vilder, and P. J. Tavner, "Comparison of direct-drive and geared generator concepts for wind turbines," *IEEE Transactions on Energy Conversion*, vol. 21, no. 3, pp. 725–733, Sept 2006.

[5] S. P. Markle, "Naval power and energy systems technology development roadmap," Naval Sea System Command, Tech. Rep., 2019.

[6] G. Sulligoi, A. Tessarolo, V. Benucci, A. M. Trapani, M. Baret, and F. Luise, "Shipboard power generation: Design and development of a medium-voltage dc generation system," *IEEE Industry Applications Magazine*, vol. 19, no. 4, pp. 47–55, July 2013.

[7] F. Mura, R. W. D. Doncker, B. Persigehl, P. Jeschke, and K. Hameyer, "Analysis of a gearless medium-voltage variable speed gas turbine," VGB, Tech. Rep., 2011.

[8] G. Sulligoi, A. Tessarolo, V. Benucci, M. Baret, A. Rebora, and A. Taffone, "Modeling, simulation, and experimental validation of a generation system for medium-voltage dc integrated power systems," *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1304–1310, July 2010.

[9] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441–1451, May 2011.

[10] D. Hirschmann, D. Tissen, S. Schroder, and R. W. De Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2511–2517, 2007.

[11] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *IEEE Transactions on Power Electronics*, vol. 6, no. 1, pp. 83–92, Jan 1991.

[12] M. Chinchilla, S. Arnaltes, and J. C. Burgos, "Control of permanent-magnet generators applied to variable-speed wind-energy systems connected to the grid," *IEEE Trans. Energy Convers.*, vol. 21, no. 1, pp. 130–135, March 2006.

[13] J. Lu, S. Golestan, M. Savaghebi, J. C. Vasquez, J. M. Guerrero, and A. Marzabal, "An enhanced state observer for dc-link voltage control of three-phase ac/dc converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 936–942, Feb 2018.

[14] N. He, M. Chen, J. Wu, N. Zhu, and D. X. Ge, "20 kW Zero-Voltage-Switching SiC-MOSFET Grid Inverter with 300 kHz Switching Frequency," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[15] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved VSCs for high-power wind energy conversion systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[16] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[17] A. Yazdani and R. Iravani, "A neutral-point clamped converter system for direct-drive variable-speed wind power unit," *IEEE Transactions on Energy Conversion*, vol. 21, no. 2, pp. 596–607, June 2006.

[18] Z. Zhang, C. M. Hackl, and R. Kennel, "Computationally efficient DMPC for three-level NPC back-to-back converters in wind turbine systems with PMSG," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 8018–8034, Oct 2017.

[19] C. Li, S. Wang, Q. Guan, and D. Xu, "Hybrid modulation concept for five-level active-neutral-point-clamped converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8958–8962, Dec 2017.

[20] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE Journal*, vol. 2, no. 1, pp. 45–50, 1992. [Online]. Available: https://doi.org/10.1080/09398368.1992.11463285

[21] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.

[22] C. Zhao, Y. Li, Z. Li, P. Wang, X. Ma, and Y. Luo, "Optimized design of full-bridge modular multilevel converter with low energy storage requirements for HVDC transmission system," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 97–109, Jan 2018.

[23] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, pp. 6 pp. Vol.3–.

[24] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, 2015.

[25] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[26] H. S. Che, W. P. Hew, N. A. Rahim, E. Levi, M. Jones, and M. J. Duran, "A six-phase wind energy induction generator system with series-connected DC-links," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2012, pp. 26–33.

[27] B. Andresen and J. Birk, "A high power density converter system for the Gamesa G10x 4.5 MW wind turbine," in *2007 European Conference on Power Electronics and Applications*, Sep. 2007, pp. 1–8.

[28] J. Birk and B. Andresen, "Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine," in *2007 European Conference on Power Electronics and Applications*, Sep. 2007, pp. 1–7.

[29] A. Damiano, I. Marongiu, A. Monni, and M. Porru, "Design of a 10 MW multi-phase PM synchronous generator for direct-drive wind turbines," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov 2013, pp. 5266–5270.

[30] Infineon, "D711N," Available: https://www.infineon.com/dgdl/Infineon-D711N-DS-v8_ 1-en_ de.pdf?fileId=db3a304412b407950112b42f99154c5f [Accessed: Feb. 25, 2020].

[31] Infineon, "Highly insulated module with Trench/Fieldstop IGBT3 and Emitter Controlled 3 diode," Available: https://www.infineon.com/dgdl/Infineon-FZ500R65KE3-DS-v03_01-EN.pdf?fileId=db3a30432cd42ee3012cea1a9f4a5639 [Accessed: Dec. 26, 2019].

[32] *Military Handbook: Reliability Prediction of Electronic Equipment: MIL-HDBK-217F*. Department of Defense, 1991.

[33] P. Huynh, P. Wang, and A. Banerjee, "An integrated permanent-magnet-synchronous-generator-rectifier architecture for limited-speed-range applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2018.

[34] P. Huynh and A. Banerjee, "Integrated generator-rectifier for electric ship DC power system," in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*, 2019, pp. 592–598.

[35] P. Huynh, P. J. Wang, and A. Banerjee, "An integrated permanent-magnet-synchronous generator-rectifier architecture for limited-speed-range applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4767–4779, 2020.

[36] P. Huynh and A. Banerjee, "Active voltage-ripple compensation in an integrated generator-rectifier system," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 3199–3206.

[37] P. Huynh and A. Banerjee, "Active voltage-ripple compensation in an integrated generator-rectifier system," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.

[38] P. T. Huynh and A. Banerjee, "Integrated rectifier-generator system for ac-to-dc conversion," Patent, Sep. 17, 2020, uS Patent App. 16/817,322.

[39] P. Huynh, S. Tungare, and A. Banerjee, "Maximum power point tracking for wind turbine using integrated generator-rectifier systems," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 13–20.

[40] P. Huynh, S. Tungare, and A. Banerjee, "Maximum power point tracking for wind turbine using integrated generator-rectifier systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 504–512, 2021.

[41] P. Huynh, A. J. Samarakoon, K. S. Haran, and A. Banerjee, "Winding layout considerations for an integrated generator-rectifier system," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021 [submitted].

[42] P. Huynh, S. Sirimanna, J. Mok, D. Lee, O. Ajala, S. Linares, D. Mulas, K. Haran, A. Dominguez-Garcia, G. Gross, and A. Banerjee, "Integrated generator-rectifier co-design for offshore wind turbines," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4194–4201.

[43] S. M. R. Kazmi, H. Goto, H. Guo, and O. Ichinokura, "A novel algorithm for fast and efficient speed-sensorless maximum power point tracking in wind energy conversion systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 29–36, Jan 2011.

[44] F. Casanellas, "Losses in PWM inverters using IGBTs," *IEE Proceedings - Electric Power Applications*, vol. 141, no. 5, pp. 235–239, Sep 1994.

[45] J. W. Kolar, F. C. Zach, and F. Casanellas, "Losses in PWM inverters using IGBTs," *IEE Proceedings - Electric Power Applications*, vol. 142, no. 4, pp. 285–288, Jul 1995.

[46] Vishay, "Standard Recovery Diodes, (Hockey PUK Version), 3000 A," Available: http://www.vishay.com/docs/93542/vs-sd2500ckseries.pdf [Accessed: Feb. 18, 2020].

[47] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*. Addison-Wesley Publishing Company, 1991.

[48] A. Di Gerlando, G. Foglia, M. F. Iacchetti, and R. Perini, "Analysis and test of diode rectifier solutions in grid-connected wind energy conversion systems employing modular permanent-magnet synchronous generators," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 5, pp. 2135–2146, May 2012.

[49] P. Huynh and A. Banerjee, "Active voltage-ripple compensation in an integrated generator-rectifier system," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 3199–3206.

[50] H. Kim and R. D. Lorenz, "A virtual translation technique to improve current regulator for salient-pole AC machines," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)*, vol. 1. IEEE, 2004, pp. 487–493.

[51] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 708–719, March 2012.

[52] H.-W. Cho, A. Yoon, N. J. Renner, and K. S. Haran, "Detailed electromagnetic analysis of a high specific power slotless permanent magnet motor with imbalanced armature windings," in *21st International Conference on the Computational of Electromagnetic Fields*, 2017.

[53] K. Ogata, *Modern Control Engineering*. Prentice Hall Upper Saddle River, NJ, 2009.

[54] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings-Electric Power Applications*, vol. 153, no. 5, pp. 750–762, 2006.

[55] C. Bak, F. Zahle, R. Bitsche, T. Kim, A. Yde, L. C. Henriksen, M. H. Hansen, J. P. A. A. Blasques, M. Gaunaa, and A. Natarajan, "The DTU 10-MW reference wind turbine," in *Danish Wind Power Research 2013*, 2013.

[56] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, "Analysis of DC-link voltage switching ripple in three-phase PWM inverters," *Energies*, vol. 11, no. 2, p. 471, 2018.

[57] J.-Y. Park, J.-K. Lee, K.-Y. Oh, J.-S. Lee, and B.-J. Kim, "Design of simulator for 3MW wind turbine and its condition monitoring system," in *Proceedings of the International MultiConference of Engineers and Computer Scientists, IMECS*, 2010, pp. 930–933.

[58] K. Tan and S. Islam, "Optimum control strategies in energy conversion of PMSG wind turbine system without mechanical sensors," *IEEE Trans. Energy Convers.*, vol. 19, no. 2, pp. 392–399, June 2004.

[59] S. Li, T. A. Haskew, R. P. Swatloski, and W. Gathings, "Optimal and direct-current vector control of direct-driven PMSG wind turbines," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2325–2337, May 2012.

[60] B. Wu and M. Narimani, *High Power Converters and AC Drives, Second Edition*. Wiley, 2016.

[61] J. Robinson, D. Jovcic, and G. Joos, "Analysis and design of an offshore wind farm using a MVDC grid," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2164–2173, Oct 2010.

[62] C. H. Houpis and M. Garcia-Sanz, *Wind Energy Systems: Control Engineering Design*. CRC press, 2012.

[63] T. M. Jahns and W. L. Soong, "Pulsating torque minimization techniques for permanent magnet AC motor drives-a review," *IEEE Transactions on Industrial Electronics*, vol. 43, no. 2, pp. 321–330, April 1996.

[64] K. Ahsanullah, R. Dutta, and M. F. Rahman, "Analysis of Low-Speed IPMMs With Distributed and Fractional Slot Concentrated Windings for Wind Energy Applications," *IEEE Transactions on Magnetics*, vol. 53, no. 11, pp. 1–10, Nov 2017.

[65] P. Huynh, S. Tungare, and A. Banerjee, "Maximum power point tracking for wind turbine using integrated generator-rectifier systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 504–512, 2021.

[66] P. Huynh, S. Sirimanna, J. Mok, D. Lee, O. Ajala, S. Linares, D. Mulas, K. Haran, A. Dominguez-Garcia, G. Gross, and A. Banerjee, "Integrated generator-rectifier co-design for offshore wind turbines," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020.

[67] N. Bianchi and M. Dai Prè, "Use of the star of slots in designing fractional-slot single-layer synchronous motors," *IEE Proceedings-Electric Power Applications*, vol. 153, no. 3, pp. 459–466, 2006.

[68] J. Faiz and I. Tabatabaei, "Extension of winding function theory for nonuniform air gap in electric machinery," *IEEE Transactions on Magnetics*, vol. 38, no. 6, pp. 3654–3657, 2002.

[69] N. L. Schmitz and D. W. Novotny, *Introductory Electromechanics*. University Microfilms, 1984.

[70] W. Musial, P. Beiter, P. Spitsen, J. Nunemaker, and V. Gevorgian, "2018 offshore wind technologies market report," National Renewable Energy Laboratory, https://www.energy.gov/eere/wind/downloads/2018-offshore-wind-market-report, Tech. Rep., 2018.

[71] C. Bak, F. Zahle, R. Bitsche, T. Kim, A. Yde, L. C. Henriksen, M. H. Hansen, J. P. A. A. Blasques, M. Gaunaa, and A. Natarajan, "The DTU 10-MW reference wind turbine," in *Danish Wind Power Research 2013*, 2013.

[72] L. Sethuraman, M. Maness, and K. Dykes, "Optimized generator designs for the DTU 10-MW offshore wind turbine using GeneratorSE," in *35th Wind Energy Symposium*, 2017, p. 0922.

[73] K. O. Merz, "Dogger bank reference wind power plant: Layout, electrical design, and wind turbine specification," SINTEFF Energy Research, Tech. Rep., 2016.

[74] H. Polinder, D. Bang, R. Van Rooij, A. McDonald, and M. Mueller, "10 MW wind turbine direct-drive generator design with pitch or active speed stall control," in *2007 IEEE International Electric Machines & Drives Conference*, vol. 2. IEEE, 2007, pp. 1390–1395.

[75] Y. Duan and R. G. Harley, "Present and future trends in wind turbine generator designs," in *2009 IEEE Power Electronics and Machines in Wind Applications*, June 2009, pp. 1–6.

[76] Toshiba, "T300MVi/MTX medium-voltage adjustable-speed motor drive," Available: https://www.toshiba.com/tic/datafiles/manuals/IF08CZ00_T300MVi-MTX_Instruction_Manual_3-31-2012_7437.pdf [Accessed: Dec. 28, 2019].

[77] E. C. Morgan, M. Lackner, R. M. Vogel, and L. G. Baise, "Probability distributions for offshore wind speeds," *Energy Conversion and Management*, vol. 52, no. 1, pp. 15 – 26, 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S019689041000227X

[78] Q. Jin, P. Huynh, and A. Banerjee, "Generator back-electromotive-force shaping for DC output with low ripple voltage," in *2019 IEEE International Electric Machines Drives Conference (IEMDC)*, 2019, pp. 539–546.

Appendix A

DIODES AND IGBTS DATA

Table A.1 lists IGBT ratings and Table A.2 lists diode ratings and market prices. Information is from Digikey catalog, accessed in February 24, 2020.

Table A.1: IGBT data

Name	Mnf.	Voltage rating	Current rating	Price	Price density	MVA rating
		[V]	[A]	[$]	[$/MVA]	[MVA]
FZ500R65KE3NOSA1	Infineon	6500	1000	1924.41	296.06	6.50
FZ500R65KE3NOSA1	Infineon	4500	1000	1924.41	427.65	4.50
FZ1200R45HL3BPSA1	Infineon	4500	1000	2282.85	507.30	4.50
FZ1200R45HL3BPSA1	Infineon	4500	1000	2282.85	507.30	4.50
FZ1200R45HL3BPSA1	Infineon	4500	1000	2282.85	507.30	4.50
FZ800R45KL3B5NOSA2	Infineon	4500	1600	1969.21	273.50	7.20
FZ800R45KL3B5NOSA2	Infineon	4500	1600	1969.21	273.50	7.20
FZ800R45KL3B5NOSA2	Infineon	4500	1600	1969.21	273.50	7.20
FZ800R45KL3B5NOSA2	Infineon	4500	1600	1969.21	273.50	7.20
FZ1200R33KF2CNOSA1	Infineon	3300	2000	2081.23	315.34	6.60
FZ1200R33KF2CNOSA1	Infineon	3300	2000	2081.23	315.34	6.60
FZ1200R33KF2CNOSA1	Infineon	3300	2000	2081.23	315.34	6.60
FZ1200R33HE3BPSA1	Infineon	3300	2300	1521.16	200.42	7.59
FZ1200R33HE3BPSA1	Infineon	3300	2300	1521.16	200.42	7.59
FZ1200R33HE3BPSA1	Infineon	3300	2300	1521.16	200.42	7.59
FF1400R17IP4P	Infineon	1700	1400	1024.62	430.51	2.38

Table A.2: Diode data

Name	Mnf.	Voltage rating	Current rating	Price	Price density	MVA rating
		[V]	[A]	[$]	[$/MVA]	[MVA]
D1481N58T	Infineon	5800	2200	354.50	27.78	12.76
D711N60TXPSA1	Infineon	6000	1070	380.98	59.34	6.42
D711N65TXPSA1	Infineon	6500	1070	444.49	63.91	6.96
D711N68TXPSA1	Infineon	6800	1070	495.27	68.07	7.28
RBK86025XX	Powerex	6000	3200	571.86	29.78	19.20
RBK86525XX	Powerex	6500	3200	580.42	27.90	20.80
D1481N68TXPSA1	Powerex	6800	2200	582.51	38.94	14.96
D931SH65TXPSA1	Powerex	6500	1220	892.68	112.57	7.93
D3001N60T	Infineon	6000	3910	918.73	39.16	23.46
D3001N65T	Infineon	6500	3910	1062.29	41.80	25.42
D1131SH65TXPSA1	Infineon	6500	1100	1163.88	162.78	7.15
D3041N65TXPSA1	Infineon	6500	4090	1219.42	45.87	26.59
D3041N60TXPSA1	Infineon	6000	4090	1242.98	50.65	24.54
D3041N68TXPSA1	Infineon	6800	4090	1285.40	46.22	27.81
D2601NH90TXPSA1	Infineon	9000	1790	1333.91	82.80	16.11
D3001N68TXPSA1	Infineon	6800	3910	1334.95	50.21	26.59
D2601N85TXPSA1	Infineon	8500	3040	1334.95	51.66	25.84
D2601N90TXPSA1	Infineon	9000	3040	1334.95	48.79	27.36
VS-SD1100C12CGI	Vishay	1200	1400	62.06	36.94	1.68
VS-SD400C16C	Vishay	1600	800	62.22	48.61	1.28
SD300C20C	Vishay	2000	650	65.74	50.57	1.30
SD400C20C	Vishay	2000	800	69.20	43.25	1.60
VS-SD1100C22C	Vishay	2200	1100	69.56	28.74	2.42
SD1100C25C	Vishay	2500	1100	84.53	30.74	2.75
VS-SD300C30C	Vishay	3000	540	100.72	62.17	1.62
VS-SD1100C30L	Vishay	3000	910	111.17	40.72	2.73
R7203006XXOO	Powerex	3000	600	131.17	72.87	1.80
R7203506XXOO	Powerex	3500	600	136.84	65.16	2.10
VS-SD800C40L	Vishay	4000	1065	194.61	45.68	4.26