A TEMPERATURE-COMPENSATED RC OSCILLATOR USING TEMPERATURE SENSOR

BY

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THESIS

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ABSTRACT

Highly stable clock reference is critical to many applications, including communication, timing, frequency synthesis, and synchronization. This thesis introduces a practice of utilizing a temperature sensor to compensate for an RC oscillator based on FLL (frequency-locked loop), on the same die of the temperature sensor, with the assistance of a frequency counter and a computer. The TCO (temperature-compensated oscillator) and the temperature sensor are presented by Khashaba et al. (2020). The additional digital circuitry for compensation can be further integrated on-chip. The achieved output frequency at 37.5 MHz varies by 875 ppm (parts per million) across the whole temperature range from -30 °C to +80 °C.

We live only to discover beauty. All else is a form of waiting.

—*Sand and Foam* by Kahil Gibran

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BOM	Bill of Materials
DCO	Digital-Controlled Oscillator
DCU	Digital Compensation Unit
FLL	Frequency-Locked Loop
FVC	Frequency-to-Voltage Converter
LIN	Local Interconnect Network
MCU	Microcontroller Unit
MEMS	Microelectromechanical System
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PTAT	Proportional to Absolute Temperature
polyfit	polynomial curve fitting
ppm	parts per million
RO	Ring Oscillator
SAW	Surface Acoustic Wave
SCR	Switched-Capacitor Resistor
TCO	Temperature-Compensated Oscillator
TDC	Time-to-Digital Converter
UART	Universal Asynchronous Receiver-Transmitter
VCO	Voltage-Controlled Oscillator

CHAPTER 1

INTRODUCTION

1.1 Motivation

Crystal oscillators have long been the most prevalent choice of stable oscillators in many systems. However, crystal oscillators are bulky (from several mm^3 to several tens of mm^3) and power-hungry. In addition, crystal oscillators require designer effort to match the resonator to the oscillator. The demands for crystal-less design are increasingly high in recent years in applications whose space budget and power budget are tight, like IoT sensor nodes and biomedical devices. Also, in some wireless networks, whose duty cycle for operation is low, the power consumption during the long sleep time is dominated by the sleep timer, so low power but accurate timers are especially desirable.

Among all the substitutes to crystal oscillators, MEMS (microelectromechanical system) or SAW (surface acoustic wave) oscillators offer the best frequency stability but still require additional volume and PCB (printed circuit board) space, not to mention the fact that their prices are probably the highest. Table 1.1 shows the comparison between different types of oscillators. As an integrated substitute, stable on-chip oscillators are desirable for better power efficiency, lower BOM (bill of materials) cost, shorter start-up time, and higher robustness against mechanical shock. Among all the types of on-chip oscillators, LC oscillators, using on-chip inductors, have frequency

Table 1.1: Comparison of different types of oscillators

Type	Crystal	MEMS	LC	Ring	Relaxation
Integrability	External	In-package	On-chip	On-chip	On-chip
Frequency(Hz)	1k-100M	200k-200M	1G-100G	10M-10G	1k-15M
Accuracy(±ppm)	1-100	<50	<200	<50000	<10000
Cost	Medium	High	Low	Low	Low
Current(A)	100n-50m	5m-50m	∼10m	10μ-100m	10n-100μ

stability comparable to crystal oscillators while requiring reasonable areas only at the GHz level. Ring oscillators occupy the smallest area but they are vulnerable to voltage and temperature variation. RC relaxation oscillators or FLL-based RC oscillators have the advantage of adequate robustness against voltage variation at the kHz to MHz range.

The biggest challenge for on-chip RC-based oscillators is the temperature characteristic of the RC product across the whole temperature range. Table 1.2 explains the temperature ranges for different applications. Since the on-die resistors are much more sensitive to temperature than on-die capacitors, the frequency instability of the capacitors can be neglected. For example, at 65 nm technology node, the resistance can vary by more than 20% from -45 °C to +85 °C. Therefore, the conventional RC-based oscillators, whose output frequencies are normally proportional to reference resistance, are not suitable for applications requiring ±250 ppm for real-time clock application or even ±40 ppm accuracy for wireless communication standards like Zigbee or WiFi. Several works published in recent years contributed to improving the temperature stability of the RC-based oscillators using different techniques and pushed the temperature variation to a smaller and smaller value. The reported performances are qualified for applications like UART (universal asynchronous receiver-transmitter) with ±1% requirement or LIN (local

Table 1.2: Comparison of different types of oscillators

Standard	Military	Automotive	Industrial	Commercial
T_{min}(°C)	-55	-40	-20/-40(Extended)	0
T_{max}(°C)	125	125	85	70

interconnect network) for automotive with ±5000 ppm requirement.

1.2 Outline

This thesis is organized as follows. Chapter 2 explains the fundamental operation of the conventional RC-based oscillator, and previous work on the RC-based oscillators. Chapter 3 introduces the TCO in [1] and the temperature sensor [2] and covers the theory and implementation of using the temperature sensor to combat the temperature variation for the TCO. The measurement results and discussions are presented in Chapter 4. Our conclusions and future work are summarized in Chapter 5.

CHAPTER 2

BACKGROUND ON RC-BASED OSCILLATORS

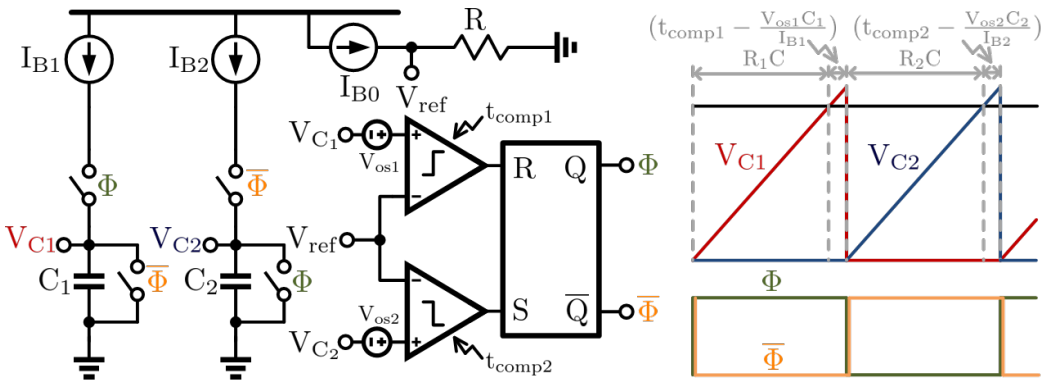
2.1 Relaxation Oscillators

There are two types of conventional relaxation RC oscillators: The first one in Fig. 2.1a with two comparators and the second one in Fig. 2.1b with only one comparator. Both oscillators have a reference voltage V_{ref} generated by a resistor R and a current source I_{B0}. It is reasonable to assume $I_{B0} = I_{B1} = I_{B2} = I_B$ and $C_1 = C_2 = C$ with proper layout.

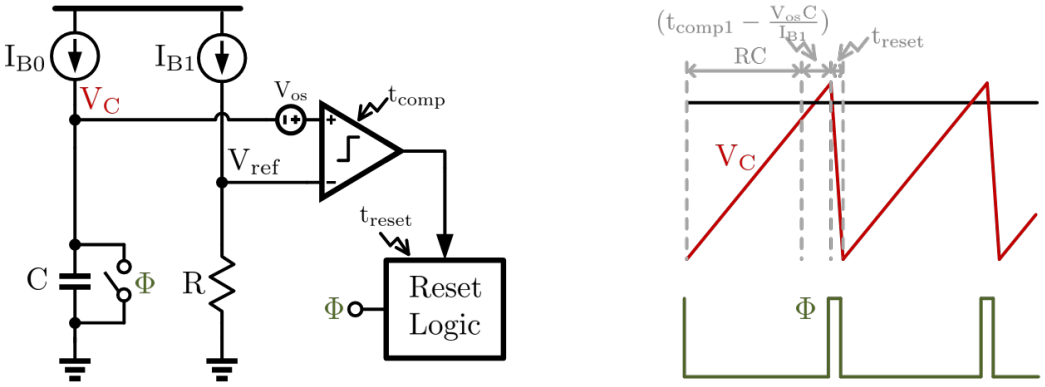
The circuitry in Fig. 2.1a has two charging branches alternatively charging the two capacitors, C_1 and C_2, from 0 V to $(V_{ref} - V_{os1,2})$. Comparators detect when V_{C1} and V_{C2} reach their upper limits. An RS flip-flop takes the outputs of the comparators to generate Φ and its complementary signal $\overline{\Phi}$, controlling the alternation between the two charging branches. Φ or $\overline{\Phi}$ has output oscillation period:

$$\begin{aligned} T_{osc,a} &= \frac{1}{2}[\frac{RC_1I_{B1}}{I_{B0}} + \frac{RC_2I_{B2}}{I_{B0}} + t_{comp1} + t_{comp2} - \frac{V_{os1}C_1}{I_{B1}} - \frac{V_{os2}C_2}{I_{B2}}] \\ &\approx \frac{1}{2}[2RC + t_{comp1} + t_{comp2} - \frac{(V_{os1} + V_{os2})C}{I_B}] \end{aligned} \tag{2.1}$$

The circuitry in Fig. 2.1b has only one charging branch and the reset logic block generates its switch control signal. Unlike the previous circuitry in Fig. 2.1a, where the capacitor discharging time does not contribute to its oscillation period due to the alternative charging, the second circuitry,

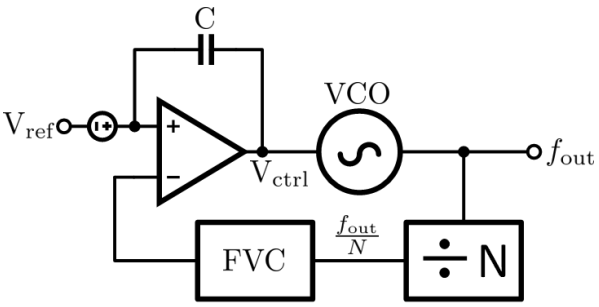


(a) With two comparators

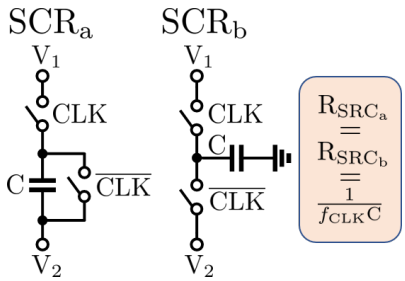


(b) With one comparator

Figure 2.1: Circuitries of conventional relaxation RC oscillators



(a) Conventional analog FLL-based oscillator



(b) Switch capacitor resistors

Figure 2.2: FLL-based oscillator architecture and SCR-based FVTs

whose oscillation period is expressed in Eqn. 2.2, has a dependence on t_{reset} to account for the capacitor discharging time and reset logic delay. Compared to the circuitry in Fig. 2.1a, the circuitry in Fig. 2.1b does not suffer from the mismatches between the two capacitors, or between the two comparators, but t_{reset} contributes extra temperature dependence.

$$\begin{aligned} T_{osc,b} &= \frac{RCI_{B1}}{I_{B0}} + t_{comp} - \frac{V_{os}C}{I_B 0} + t_{reset} \\ &\approx RC + t_{comp} - \frac{V_{os}C}{I_B} + t_{reset} \end{aligned} \tag{2.2}$$

2.2 FLL-based Oscillators

The architecture of FLL-based oscillators dates back to 1987, when analog and radio-frequency IC pioneer Prof. Asad A. Abidi proposed an early model of analog FLL in [3], using a SCR (switched-capacitor resistor) to convert frequency to voltage. To generalize, analog FLL-based oscillators commonly use an FVC (frequency-to-voltage converter) to translate frequency information into voltage domain. As shown in Fig 2.2a, an integrator integrates the difference between reference voltage and the voltage representation of the divided output frequency, and then outputs the control voltage V_{ctrl} for the VCO (voltage-controlled oscillator). The temperature-dependent offset voltage of a integrator can be cancelled by an auto-zeroing circuit or averaged out by chopping. If the FVC is linear, by defining K_{VCO} ($\frac{Hz}{V}$) as the VCO gain and $V_{FVC}(f_{out})$ ($\frac{V}{Hz}$) as the FVC function, the s-domain expression can be written as:

$$f_{out} = (V_{ref} - V_{FVC}(\frac{f_{out}}{N}))\frac{K_{VCO}}{sC_{int}} \tag{2.3}$$

The steady state expression of the output frequency is shown in Eqn. 2.4.

$$f_{\text{out}} = \text{N}\text{V}_{\text{FVC}}^{-1}(\text{V}_{\text{ref}}) \tag{2.4}$$

The closed-loop oscillator architecture provides good immunity to supply voltage variation and relieves the linearity requirement of the VCO. A digital counterpart is very similar, with a digital integrator, a DCO (digital-controlled oscillator) and a phase-to-digital converter. Digital FLLs have an advantage in performing accurate calculations, which is essential for high-order temperature compensation.

2.3 Prior Art and Proposed Techniques

To date, the best-reported number is ±170 ppm from -45 °C to +85 °C in [4]. In this section, several approaches and architectures implemented in previous works will be introduced.

a) Composite resistor:

Ideally, connecting two resistors with temperature coefficients of opposite signs with an appropriate ratio can fully cancel the 1st order temperature dependence of the total resistance, as shown in Fig. 2.3. However, the process variation of the resistances of R_A and R_B makes the cancellation less effective. To precisely trim the resistances, large switch matrices are required to tune the resistance after fabrication. As a result, the ratio between two types of resistors has limited resolution. Another limitation of this approach is coming from the switch leakage current, contributing high-order temperature dependence. This approach, implemented in [5], cannot achieve better than ± several thousands ppm of frequency stability. When targeting $<$ ±1000

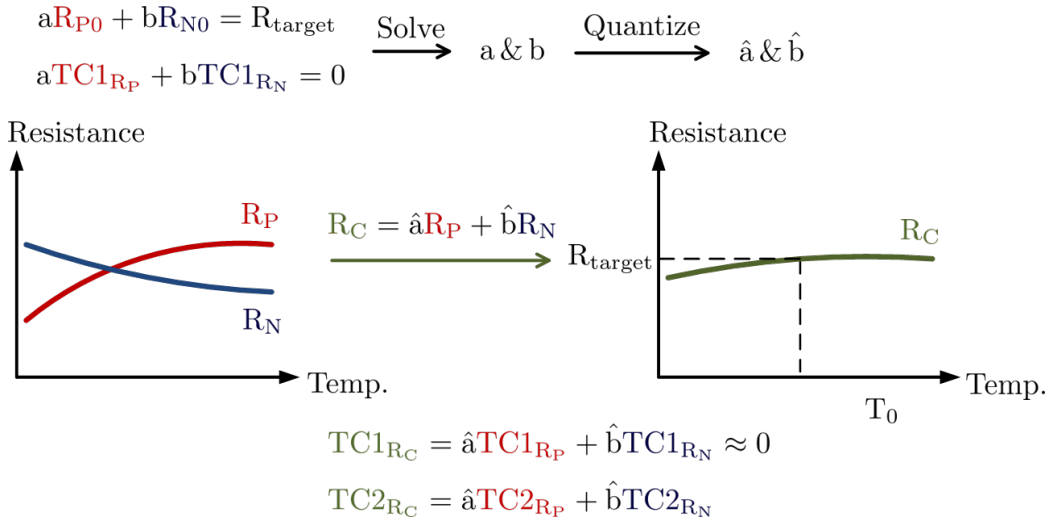


Figure 2.3: Composite resistors

ppm frequency stability, it is wise to rely on composite resistors with switch matrices for coarse tuning rather than fine tuning.

b) Chopping:

The conventional relaxation RC oscillators suffer from the comparator offset voltage V_{os}, the mismatch between two bias currents and the mismatch between two capacitors. In addition, these effects vary with temperature and V_{os} is the major bottleneck for kHz relaxation RC oscillators. Those mismatches translate to a temperature-dependent inaccuracy in the period of the output frequency, shown in Eqn. 2.1 and 2.2. In [6] and [7], chopping is deployed for a voltage-mode comparator and a current-mode comparator, respectively. Chopping for the comparators or amplifiers can strongly attenuate the impact of offset at their differential input pairs. Chopping can be also deployed in two charging branches to average out the mismatch between two bias current sources. More than that, the chopping also kills the low-frequency flicker noise as long as the chopping frequency is much higher than the corner frequency of flicker noise.

c) Comparator delay compensation techniques:

The delay of the comparator t_{comp} is sensitive to temperature variation and is not negligible. Especially for MHz range relaxation RC oscillators, t_{comp} variation is often one of the main challenges, because comparators with higher slew rate are also more power-hungry. Voltage averaging feedback, proposed in [8] and [9], utilizes an analog integrator to capture the average voltage of the output waveform and adjusts the threshold voltage at the input of the comparators correspondingly. V_{avg} is forced to a stable V_{REF} so that t_{comp} variation can be compensated. Another approach, proposed in [10], is to add a digital delay t_{dig}, generated by a delay control unit, to the oscillation period and make $(t_{comp} + t_{dig})$ a constant. The value of t_{dig} is calculated by comparing the oscillation period with a reference pulse width, which are digitized by two TDCs (time-to-digital converters). A third feedforward technique is presented in [11]: Boost the charging current I_{ch} to $2I_{ch}$ for t_{comp} to cancel the influence of the comparator delay. A period controller, containing replica comparators and RS flip-flop, measures t_{comp} and generates a pulse with duration of t_{comp} to trigger the boost current at the beginning of each charging cycle. Figure 2.4 further illustrates these three techniques.

d) Temperature sensing and compensation:

It is not a new technology in industry to use a bipolar-based or thermistor-based temperature sensor to compensate a crystal oscillator. The same idea can be applied to on-chip RC-based oscillators. In [4], [12], [13], and [14], temperature sensors contribute to the temperature compensation of the oscillators. The oscillator system in [11] uses a slow gate leakage powered RO, whose output frequency changes linearly with temperature, to measure the frequency of the faster main oscillator; based on the measurement, the tem-

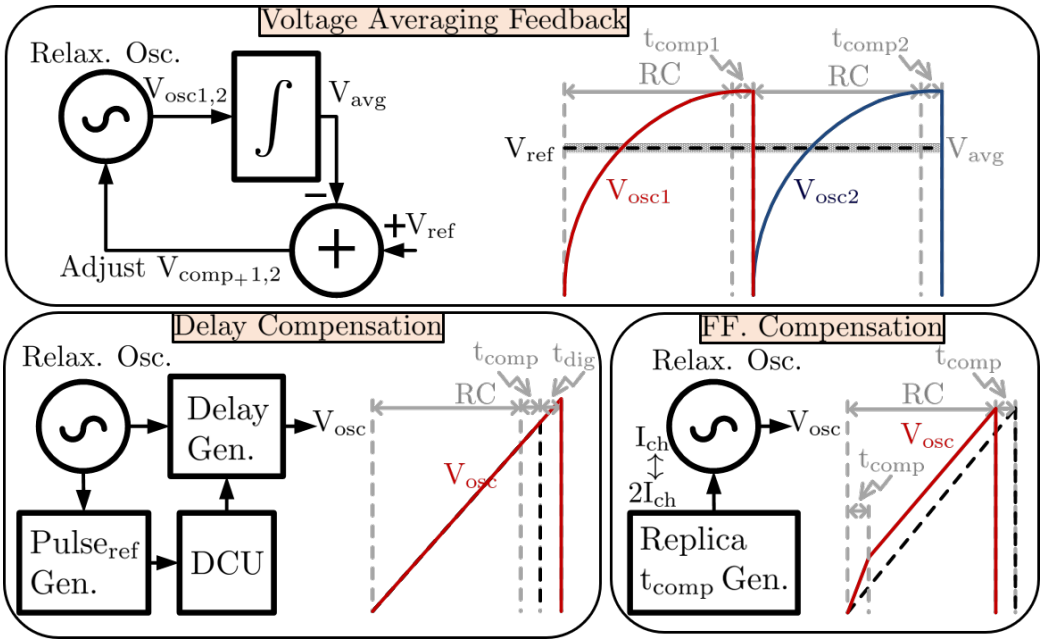


Figure 2.4: Three techniques to compensate t_{comp}

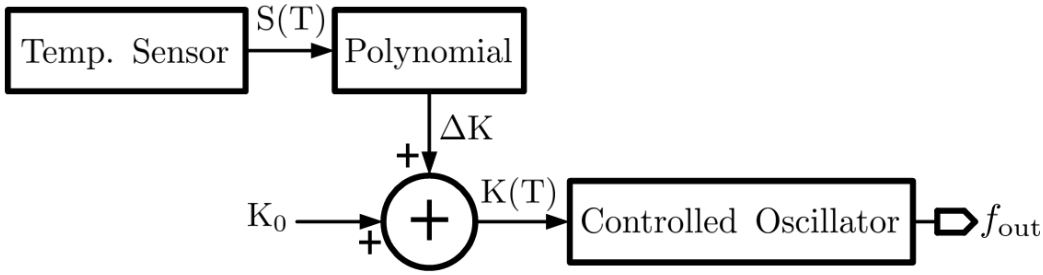


Figure 2.5: Typical temperature-compensated oscillator system with a temperature sensor

perature range is cut into two regions for different tuning setups of the resistor bank and the capacitor bank. The phase information of electrothermal filter and Wien bridge filter, fed with divided output CLK, is digitized through phase-domain $\Delta\Sigma$ modulators as the indication of temperature in [4] and [13], respectively; digital FLLs and DCOs are implemented in both works to generate compensated output frequencies. In [14], two frequency counters measure the frequencies of a PTAT (proportional to absolute temperature) thermometer relaxation oscillator and of a reference relaxation oscillator; the ratio between the two frequencies contains the temperature information, which is fed to a digital FLL. An additional feature in [14] is the addition of an on-chip heater to implement on-chip calibration.

Figure 2.5 shows the block diagram of a typical TCO with a temperature sensor. S(T) is the output of the temperature sensor and K(T) is the control signal of the controlled oscillator. Lower resolution and smaller error of the temperature sensor let S(T) reflect the temperature more accurately. Higher polynomial order used in the polynomial function helps mitigate the temperature variation of higher orders but also increases the complexity of the computation of the coefficients. The resolution of K(T) and the sensitivity of f_{out} to K(T) define how fine the controlled oscillator can be tuned.

e) FLL Implementation:

FLLs in [3], [15] and [16] are implemented in analog domain, with SCR-based FVCs. The temperature dependences of the oscillators in [15] and [16] are limited by the reference composite resistor to over $\pm$3000 ppm. One notable technique implemented in [16] is to add dummy switches in the V_{ref} generation circuitry to compensate for the leakage current of the SCR. The FLLs in [4], [13] and [14] are digital and their signal paths are in phase domain with phase-domain $\Delta\Sigma$ modulators.

CHAPTER 3

TEMPERATURE COMPENSATION

3.1 TCO Architecture

Khashaba et al. presented a FLL-based oscillator with ±530 ppm frequency variation in [1] and Fig. 3.1 shows its architecture. This FLL-based oscillator has a voltage-controlled RO (Ring Oscillator) to generate $\mathrm{CLK_{OUT}}$, whose frequency is f_{TCO}. Shown in Eqn. 3.1, a temperature-independent voltage $\mathrm{V_{REF}}$ is generated by a resistor divider of two same-type resistors, with resistances of $\mathrm{R_D}$ and $\mathrm{xR_D}$.

$$\mathrm{V_{REF}} = \frac{x\mathrm{R_D(T)}}{x\mathrm{R_D(T)} + \mathrm{R_D(T)}}\mathrm{V_{DD}} = \frac{x}{x+1}\mathrm{V_{DD}} \tag{3.1}$$

The output frequency, after being divided by N, is translated to resistance through a SCR with resistance $\frac{\mathrm{N}}{f_{\mathrm{TCO}}\mathrm{C}}$. Pulse-density-modulated $\mathrm{R_1}$, $\mathrm{R_2}$ and $\mathrm{R_3}$ are in parallel and are controlled by the DCU (digital compensation unit). The control words for the three resistors α_1, α_2, and α_3 are quantized by three 1-bit $\Delta\Sigma$ modulators. Their equivalent resistance is $\mathrm{R_{REF}}$:

$$\mathrm{R_{REF}} = (\frac{\alpha_1}{\mathrm{R_1}} + \frac{\alpha_2}{\mathrm{R_2}} + \frac{\alpha_3}{\mathrm{R_3}})^{-1} \tag{3.2}$$

The voltage divider between $\mathrm{R_{SCR}}$ and $\mathrm{R_{REF}}$ gives $\mathrm{V_F}$. $\mathrm{V_F}$ is compared to $\mathrm{V_{REF}}$ and their difference is the error signal of this FLL. This error signal is

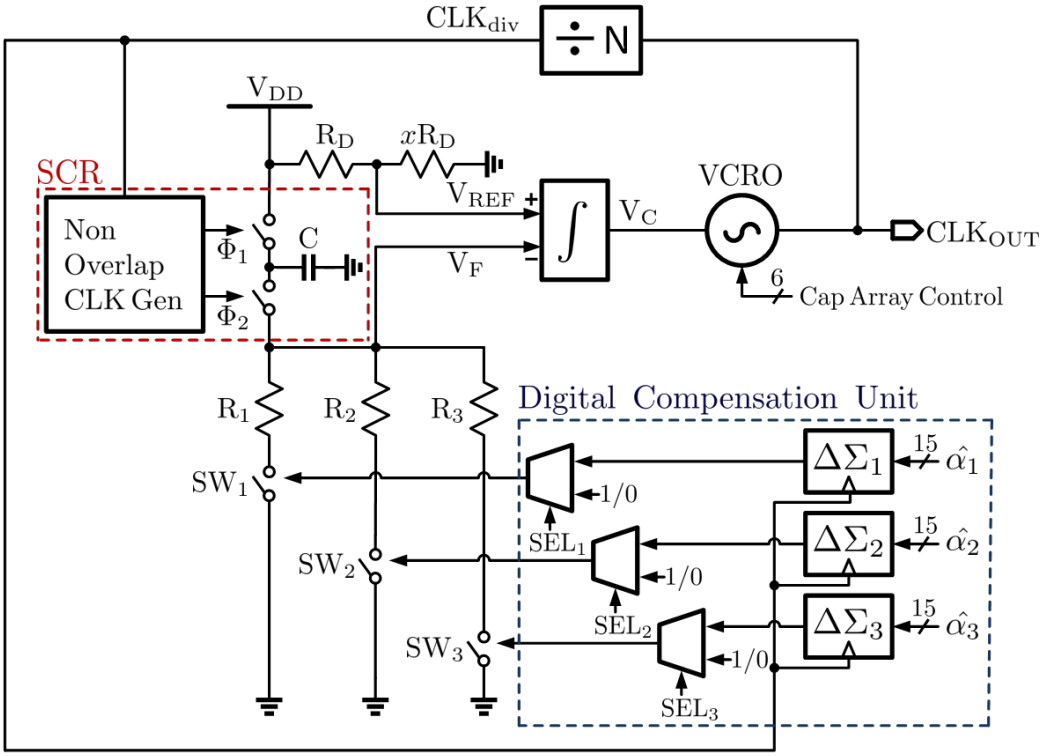


Figure 3.1: Architecture of the TCO used in this work

integrated to be V_C, the control voltage of the voltage-controlled RO. When the FLL is locked, $V_{REF} = V_F$ and this oscillator's output frequency f_{TCO} is shown in Eqn. 3.3, where $f_{1,2,3} = \frac{Nx}{R_{1,2,3}C}$. Eqn. 3.4 shows the s-domain expression of this FLL, where G_m and C_{int} are the design parameters of the Gm-C integrator and K_{VCO} is the VCO gain.

$$\begin{aligned} f_{TCO} &= \frac{Nx}{R_{REF}C} \\ &= Nx\left(\frac{\alpha_1}{R_1C} + \frac{\alpha_2}{R_2C} + \frac{\alpha_3}{R_3C}\right) \\ &= \alpha_1 f_1 + \alpha_2 f_2 + \alpha_3 f_3 \end{aligned} \tag{3.3}$$

$$\begin{aligned} f_{TCO} &= V_{error}\frac{G_m}{sC_{int}}K_{VCO} \\ &= \left(\frac{x}{x+1} - \frac{1}{1+\frac{N}{f_{TCO}C}\left(\frac{\alpha_1}{R_1} + \frac{\alpha_2}{R_2} + \frac{\alpha_3}{R_3}\right)}\right)V_{DD}\frac{G_m}{sC_{int}}K_{VCO} \end{aligned} \tag{3.4}$$

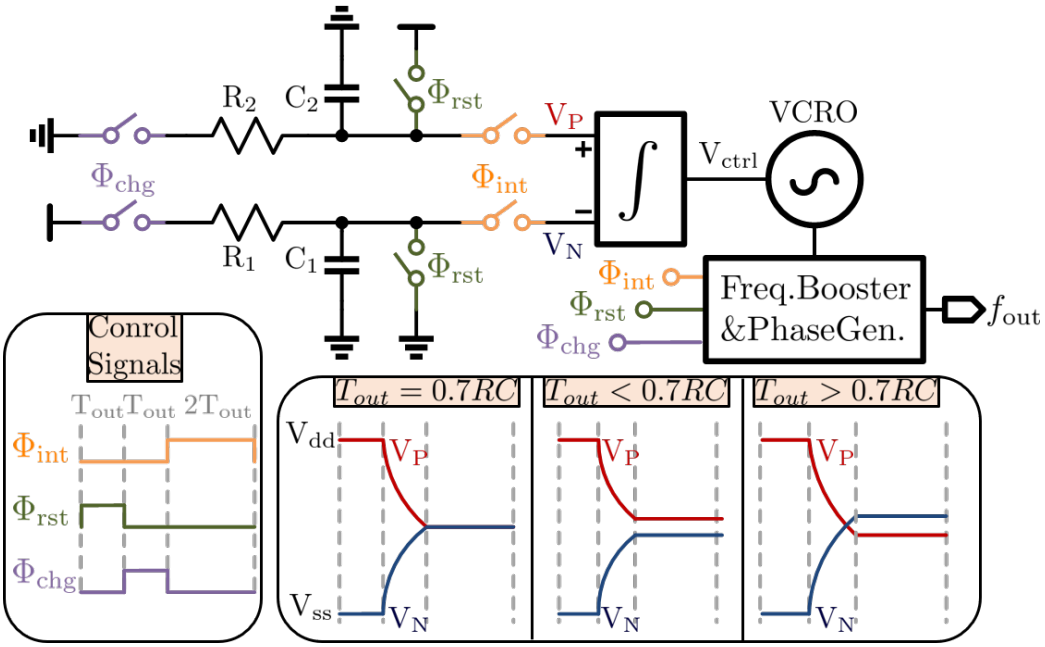


Figure 3.2: Architecture of the temperature sensor used in this work

3.2 Temperature Sensor Architecture

The temperature sensor in [2] is resistor-based, so it offers better conversion energy FoM compared to bipolar-based or MOS-based sensors. Temperature sensors based on Wheatstone bridge or Wien bridge need ΔΣADCs (delta-sigma analog-to-digital converter), which are normally large and power-hungry, to digitize the temperature information. Instead, this sensor operates in voltage-domain and a FLL generates the output as frequency, so the noisy charge pumps needed in phase-domain FLLs are eliminated.

Block diagram and waveforms are shown in Fig. 3.2. There are three stages of operation. During the first reset stage, V_P is charged to V_{DD} and V_N is discharged to 0V. In the second charging stage, V_P discharges while V_N charges; the resulting error signal is shown in Eqn. 3.5. The third stage lets the integrator accumulate V_E and output V_{CTRL}, the control voltage of the VCO. The FLL locks when the VCO output period equals $(-\ln(0.5)RC)$,

which is approximately 0.7RC. The VCO output is fed to a frequency booster to make the output frequency 10 times higher so that the temperature sensitivity becomes higher. This temperature sensor achieves ±0.5°C accuracy with 1-point trimming and ±0.25°C accuracy with 2-point trimming.

$$\mathrm{V_E} = \mathrm{V_P} - \mathrm{V_N}|_{\phi_{\mathrm{int}}} = \mathrm{V_{DD}}(2e^{-\frac{\mathrm{T_{VCO}}}{\mathrm{RC}}} - 1) \tag{3.5}$$

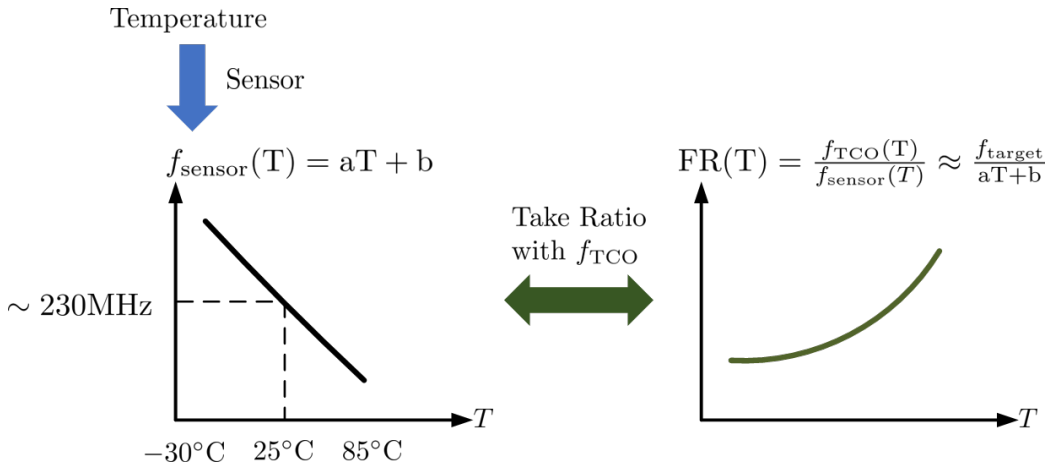
3.3 Compensation Theory

The temperature compensation scheme of an oscillator needs two key elements: The first is a sensitive knob to control the output frequency of the oscillator; the second is an accurate measure of temperature. Both elements will be discussed in this section.

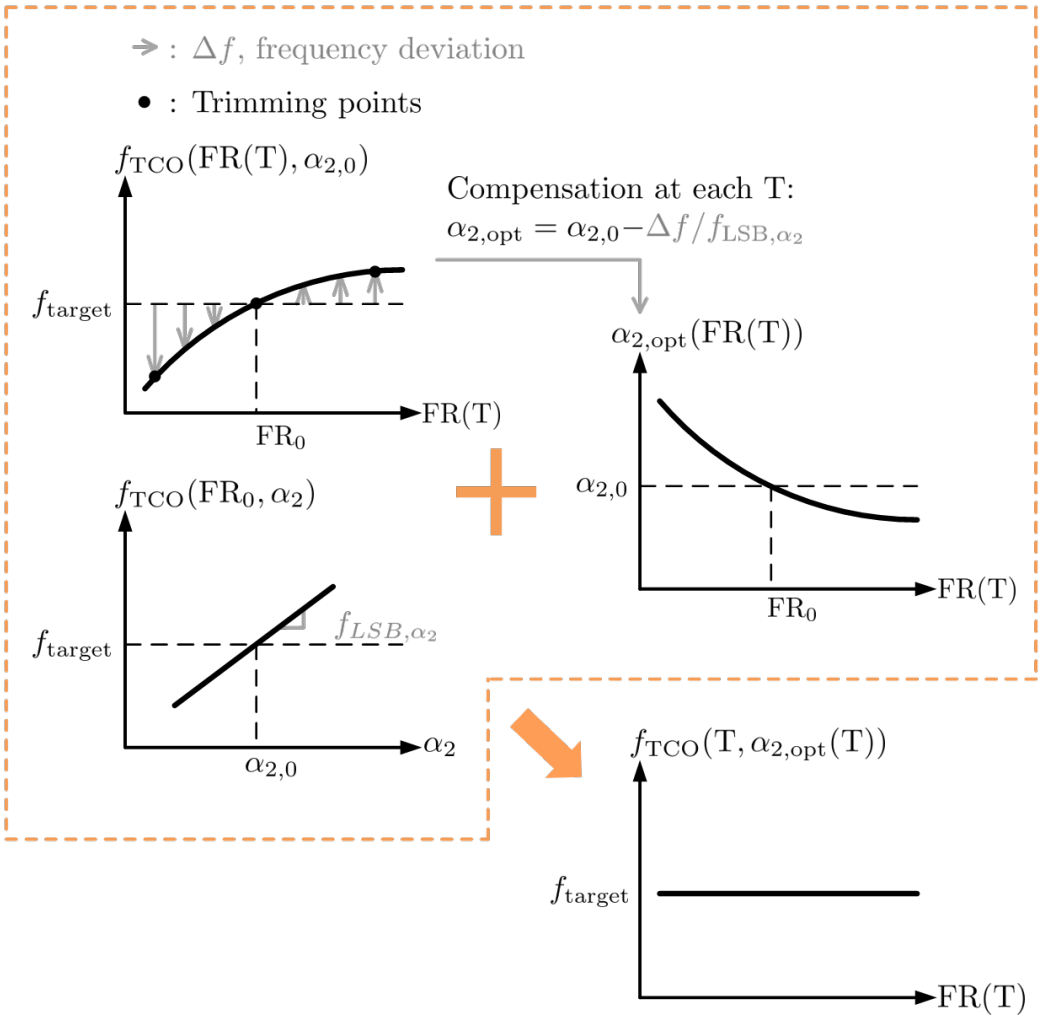
In our system, the TCO in [1] acts like a DCO with a very fine tuning step. As shown in Eqn. 3.3, among all the variables in the expression of the TCO output frequency, only α_1, α_2, α_3 can be adjusted with a 15-bit resolution. Which knob should be tuned in order to achieve the optimal resolution of control needs to be carefully analyzed because half of LSB of the knob is the largest deviation from the best control word. By taking a partial derivative, Eqn. 3.6 indicates that larger R_n and lower N both lead to a smaller change in the TCO output frequency if the control word changes by one LSB.

$$\frac{\delta f_{\mathrm{TCO}}}{\delta \alpha_n}\frac{1}{2^{15}} = \frac{f_n}{2^{15}} = \frac{\mathrm{N}x}{\mathrm{R}_n\mathrm{C}}\frac{1}{2^{15}} = f_{\mathrm{LSB}} \tag{3.6}$$

Another observation from Eqn. 3.3 is that for a given target frequency, the larger the $\Sigma_n \frac{\alpha_n}{\mathrm{R}_n}$, the smaller the N. Among these three resistors, R_2 has the largest resistance. Therefore, the best resolution can be achieved under



(a) Conversion from Temperature to FR(T)



(b) Temperature compensation scheme using $\alpha_{2,\text{opt}}$

Figure 3.3: Temperature compensation plots

this condition: α_1 and α_3 are set to be 1, and α_2 is tuned to combat the temperature variation. Instead of using 100% pulse density modulation for R_1 and R_3, the switch MOSFETs (metal–oxide–semiconductor field-effect transistors) can be forced to be on if $SEL_1 = SEL_2 = 1$ and for each resistor the forcing signal is chosen to be 1. The sensitivity is found to be less than 10 ppm per LSB of α_2 in simulation. Including the contribution of α_2, the TCO output frequency is expressed in Eqn 3.7, where $\Delta\alpha_2$ is the change of α_2 compared to the α_2 giving f_{target} at T_0.

$$f_{\text{TCO}}(\Delta T, \alpha_2) = f_{\text{TCO},0}(1 + TC_{1,\text{TCO}}\Delta T + TC_{2,\text{TCO}}\Delta T^2) + \Delta\alpha_2 f_{\text{LSB},\alpha_2} \tag{3.7}$$

At each temperature, there exists an optimal R_2 control word $\alpha_{2,\text{opt}}$ which can compensate for the temperature drift of the TCO with an ideal maximum inaccuracy of $0.5 f_{\text{LSB},\alpha_2}$.

The next step is to find T from the output CLK of the temperature sensor. In this work, the indication of the temperature information is the frequency ratio FR(T) between $f_{\text{TCO}}(T)$ and $f_{\text{sensor}}(T)$, as shown in Fig. 3.3a. On chip, FR(T) can be easily measured through a simple counter to use the faster CLK_{sensor} to count the slower CLK_{TCO}. Compared to other works, this implementation does not need a power-hungry ADC to digitize the temperature sensor output. Although $f_{\text{TCO}}(T)$ is also a function of temperature, the temperature dependence of $f_{\text{sensor}}(T)$ is much stronger. Across the whole temperature range, $f_{\text{sensor}}(T)$ changes by about $\pm 12.5\%$, while f_{TCO} only varies by approximately $\pm 0.75\%$. From simulations, $TC1_{\text{sensor}}$ is of the order of 10^{-3}, and $TC1_{\text{TCO}}$ is of the order of 10^{-5}, and $TC2_{\text{TCO}}$ is of the order of 10^{-7}. The temperature dependency of FR(T) can be approximated as a

function of form $\frac{c}{dT+e}$:

$$\begin{aligned}\frac{\partial \mathrm{FR(T)}}{\partial \Delta \mathrm{T}} &\approx \frac{f_{\mathrm{TCO},0}}{f_{,0}} \frac{\mathrm{TC_{1,sensor}}}{(2\mathrm{TC_{1,sensor}})\Delta \mathrm{T}+1} \\ &= \frac{f_{\mathrm{TCO},0}}{f_{\mathrm{sensor},0}} \frac{1}{2\Delta \mathrm{T}+1/\mathrm{TC_{1,sensor}}}\end{aligned} \tag{3.8}$$

Figure 3.3b illustrates the overall compensation scheme, where $\mathrm{FR_0}$ equals $\mathrm{FR(T_0)}$ and $\alpha_{2,0}$ is the $\alpha_{2,\mathrm{opt}}$ at $\mathrm{T_0}$. With the information of temperature, the optimal $\mathrm{R_2}$ control word versus FR(T) can be extracted through trimming. A 3-point trimming at three temperatures can extract a 2nd-order polynomial function $\alpha_{2,opt}(\mathrm{FR(T)})$ by solving this matrix:

$$\begin{bmatrix} \mathrm{FR^2(T_1)} & \mathrm{FR(T_1)} & 1 \\ \mathrm{FR^2(T_2)} & \mathrm{FR(T_2)} & 1 \\ \mathrm{FR^2(T_3)} & \mathrm{FR(T_3)} & 1 \end{bmatrix} \begin{bmatrix} \mathrm{C_2} \\ \mathrm{C_1} \\ \mathrm{C_0} \end{bmatrix} = \begin{bmatrix} \alpha_{2,\mathrm{opt@T_1}} \\ \alpha_{2,\mathrm{opt@T_2}} \\ \alpha_{2,\mathrm{opt@T_3}} \end{bmatrix} \tag{3.9}$$

$$\begin{aligned}\alpha_{2,\mathrm{opt}}(\mathrm{T}) &= \alpha_{2,\mathrm{opt}}(\mathrm{FR(T)}) \\ &= \mathrm{C_2FR^2(T)} + \mathrm{C_1FR(T)} + \mathrm{C_0}\end{aligned} \tag{3.10}$$

Eqn. 3.10 shows how to calculate the optimal α_2. Finally, compensated $f_{\mathrm{TCO}}(\Delta \mathrm{T}, \alpha_{2,\mathrm{opt}})$ is very robust against the temperature variation with up to 2nd-order temperature variation suppressed.

3.4 Control Loop

The control loop, shown in Fig. 3.4, takes the difference between the target control word $\alpha_{2,\mathrm{opt}}$ and the current control word $\alpha_{2,\mathrm{curr}}$ as the error signal. This negative feedback loop can settle the control word to the closest point near the current best control word. The tolerance of the α_2 error signal is

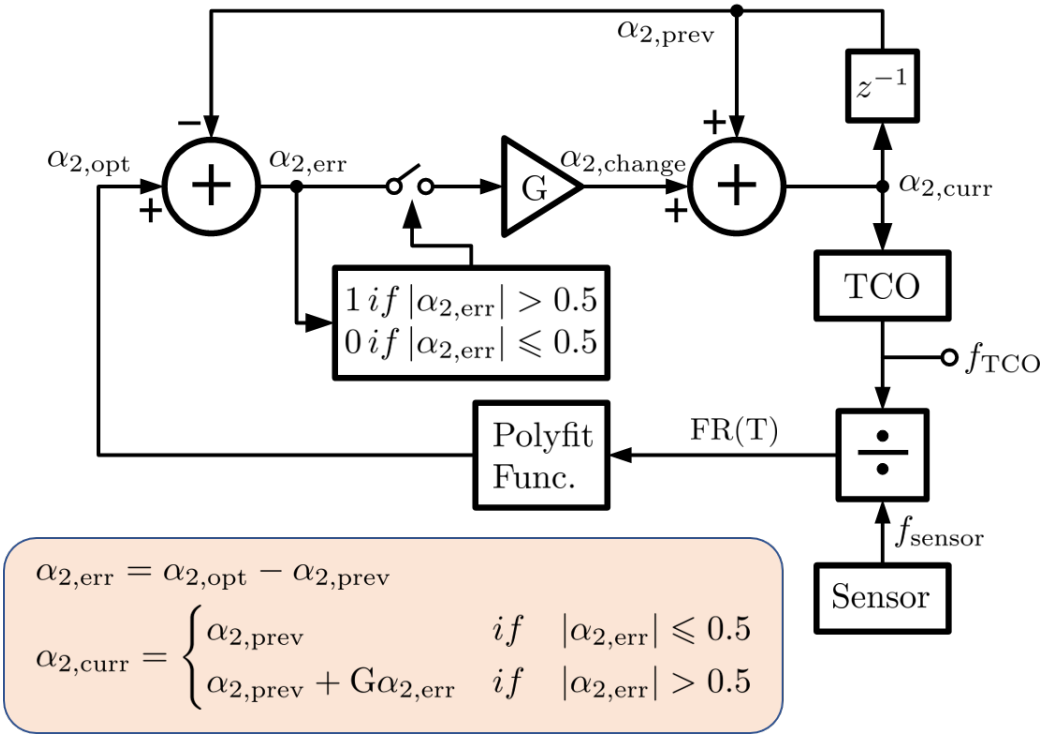


Figure 3.4: Block diagram of the control loop

0.5 in decimal since the digital control word cannot possibly get any closer to an arbitrary non-integer number. The loop period, about several seconds, is defined by the summation of the time for serial communication through the MCU (microcontroller unit), the time for the acquisition of frequency ratio from the frequency counter and the time for control word calculation in Matlab. If the system is moved to fully on-chip, the loop period can be decreased based on the need of user.

When the control loop starts, the default $\alpha_{2,\text{opt}}$ is $\alpha_{2,\text{opt}}(\text{T}_0)$. At a given temperature, if $|\alpha_{2,\text{err}}| > 0.5$, the z-domain expression of $\alpha_{2,\text{curr}}$ is shown in

Eqn. 3.11 and Eqn. 3.12.

$$\begin{aligned}\alpha_{2,\mathrm{curr}}(z,\mathrm{T}) &= \Delta\alpha_{2,\mathrm{curr}} + \alpha_{2,\mathrm{opt}}(\mathrm{T}_0) \\ &= \frac{\mathrm{G}}{1+(\mathrm{G}-1)z^{-1}}\alpha_{2,\mathrm{opt}}(\mathrm{FR}(\frac{f_{\mathrm{TCO}}(\alpha_{2,\mathrm{prev}},\mathrm{T})}{f_{\mathrm{sensor}}(\mathrm{T})})) \\ &= \frac{\mathrm{A}\Delta\alpha_{2,\mathrm{curr}}^2 + \mathrm{B}\Delta\alpha_{2,\mathrm{curr}}z + \mathrm{C}z^2}{z[z+(\mathrm{G}-1)]}\end{aligned} \tag{3.11}$$

$$\begin{aligned}\mathrm{A} &= \frac{\mathrm{C}_2 f_{\mathrm{LSB},\alpha_2}^2}{f_{\mathrm{sensor}}^2(\mathrm{T})} \\ \mathrm{B} &= \frac{2\mathrm{C}_2 f_{\mathrm{LSB},\alpha_2} f_{\mathrm{TCO}}(\mathrm{T})}{f_{\mathrm{sensor}}^2(\mathrm{T})} + \frac{\mathrm{C}_1 f_{\mathrm{LSB},\alpha_2}}{f_{\mathrm{sensor}}(\mathrm{T})} \\ \mathrm{C} &= \frac{\mathrm{C}_2 f_{\mathrm{TCO}}^2(\mathrm{T})}{f_{\mathrm{sensor}}^2(\mathrm{T})} + \frac{\mathrm{C}_1 f_{\mathrm{TCO}}(\mathrm{T})}{f_{\mathrm{sensor}}(\mathrm{T})} + \mathrm{C}_0\end{aligned} \tag{3.12}$$

The region of convergence in z-plane is $|z| > (\mathrm{G}-1)$, so as long as $\mathrm{G}\leq 1$ and $|z| > 0$, the convergence of $\alpha_{2,\mathrm{curr}}$ is guaranteed. In this work, G is chosen to be 0.5.

3.5 Limitations and Sources of Error

There are several nonidealities inside this system that limit the temperature stability of the oscillator.

Firstly, the compensation mechanism is designed to combat the 1st-order and the 2nd-order temperature variation. The compensation scheme cannot compensate for higher order temperature dependence of the on-chip resistors. The SCR cannot be simply characterized by $\frac{\mathrm{N}}{f_{\mathrm{TCO}}C}$ because the leakage current of the switches introduces nonlinearity of higher orders. The pulse-density-modulation switches also have leakage currents that can deteriorate the frequency stability of this system.

Secondly, the measured f_{TCO} and f_{sensor} have error and so does FR(T). The finite resolution and non-linearity of the temperature sensor cause FR(T) to

be less accurate and undermine the overall temperature compensation effect. The noise at the output frequencies of the TCO and the sensor also cause error. In [2], the reported slope $\frac{\partial f_{\text{sensor}}}{\partial \text{T}}$ is 0.22%/°C, so the maximum 0.5 °C error leads to ±1100 ppm error in f_{sensor}. The noise of f_{sensor} and the noise of f_{TCO} are only on the order of ±10 ppm, which can be neglected. Including these aforementioned error sources, the frequency ratio can be approximately expressed as:

$$\begin{aligned} \text{FR}^{'}(\text{T}) = \text{FR}(\text{T}) + \text{FR}_{\text{err}}(\text{T}) &= \frac{f_{\text{TCO}} + f_{\text{TCO,noise}}}{f_{\text{sensor}} + f_{\text{sensor,res}} + f_{\text{sensor,noise}}} \\ &\approx \frac{f_{\text{TCO}}}{f_{\text{sensor}} + f_{\text{sensor,res}}} \end{aligned} \tag{3.13}$$

The error in FR(T) also affects all three coefficients in Eqn. 3.9. Therefore, the maximum error in the compensated f_{TCO} is expressed in Eqn. 3.14 and part of this maximum can be compensated by the 2nd-order temperature compensation.

$$\begin{aligned} f_{\text{TCO,FRerrorMax}}(\text{T}) = \text{C}_{2,\text{err}}\text{FR}^2(\text{T}) + (\text{C}_2 + \text{C}_{2,\text{err}})(\text{FR}^2{}_{\text{err}}(\text{T}) + \text{FR}(\text{T})\text{FR}_{\text{err}}(\text{T})) \\ + \text{C}_1\text{FR}_{\text{err}}(\text{T}) + \text{C}_{1,\text{err}}(\text{FR}(\text{T}) + \text{FR}_{\text{err}}(\text{T})) + \text{C}_{0,\text{err}} \end{aligned} \tag{3.14}$$

CHAPTER 4

EXPERIMENT SETUP AND RESULTS

4.1 Hardware Setup

Figure 4.1 shows the setup of the whole system. Two supply boards, each consisting of 5 LDOs, regulate the 3.3 V supply from the Keithly 2220 DC power supply to either 1.0 V or 1.2 V for the chip. The outputs of the TCO and the temperature sensor are connected to the Keysignt 53230A frequency counter with 50 Ω channel impedance. The computer reads the measured frequencies and the frequency ratio through an IVI-C driver. The computation during the trimming process and the calculation to find $\alpha_{2,\text{opt}}$ are done in Matlab. The control words are sent to the registers inside the chip through Microchip ATXMEGAA3BU MCU. The TestEquity model 107 temperature chamber is used to adjust the ambient temperature of the chip.

4.2 Trimming Process

The goal of the trimming is to find the relationship between the control word $\alpha_{2,\text{opt}}$ and the frequency ratio FR(T). Given that the target frequency is 37.5 MHz, the trimming process can be broken down into 4 steps.

1) Adjust the 6-bits control word for the MOM capacitor bank at the output of the ring oscillator to align the 37.5 MHz in the middle of the tunable range of the ring oscillator.

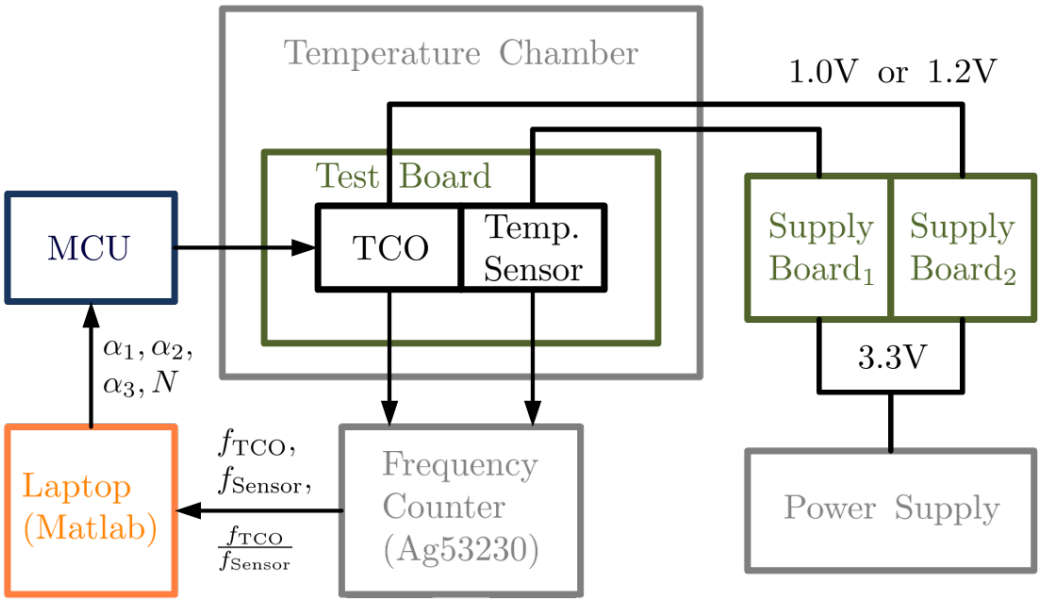


Figure 4.1: Hardware connections

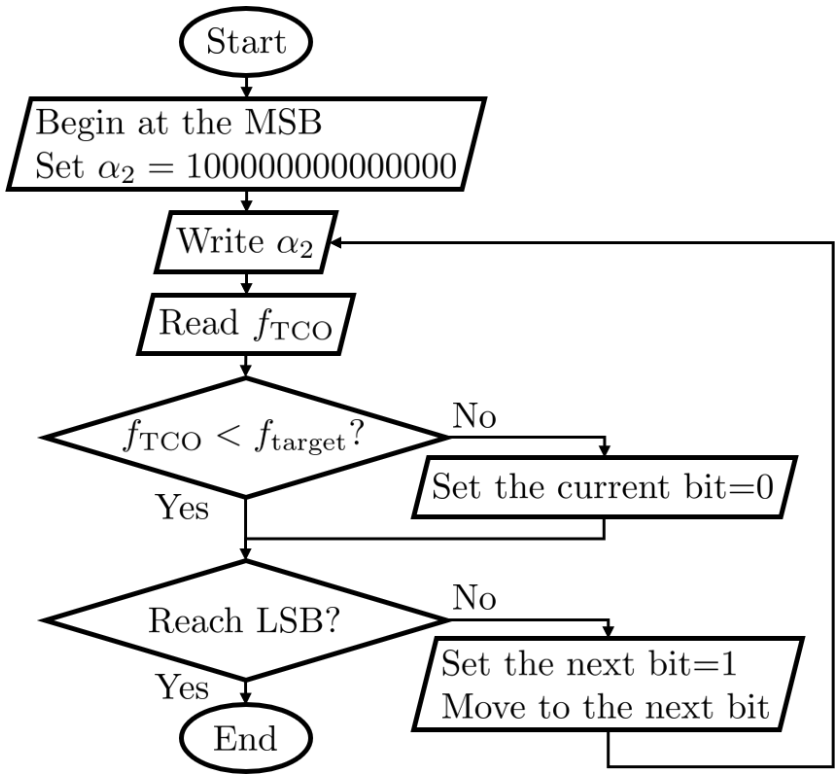


Figure 4.2: SAR algorithm used during trimming process

2) Sweep the 15-bit control word of R_2 and plot the TCO output frequency to make sure the proximity of 37.5 MHz is within the range of linear control.

3) At the three trimming temperatures: -30 °C, 25 °C, and 80 °C, run the SAR algorithm in Fig. 4.2 to find $\alpha_{2,\mathrm{opt}}$(FR(-30 °C)), $\alpha_{2,\mathrm{opt}}$(FR(25 °C)) and $\alpha_{2,\mathrm{opt}}$(FR(80 °C)), respectively.

4) Apply the 2nd-order polyfit (polynomial curve fitting) function in Matlab to find the expression of $\alpha_{2,\mathrm{opt}}$(FR(T))

4.3 Testing Results

All frequency measurements are taken with 1 s gate time. Figure 4.3 shows the f_{TCO} result of sweeping α_2 at the proximity of 37.5 MHz. Between 35.9 MHz and 38.9 MHz there are 15387 LSBs out of 32768 (2^{15}), so each LSB of α_2 corresponds to 173.5 Hz change in f_{TCO}, which is 4.64 pmm out of 37.5 MHz. With the $\alpha_{2,\mathrm{opt}}$ at $T_0 = 25$ °C, f_{TCO} at different temperatures are measured from -30 °C to -80 °C with a step size of 10 °C. From the measured data, a 4th-order polynomial fitting with T_0 at +25 °C is conducted from -40 °C to +90 °C and the results are in Fig. 4.4. Figure 4.5 shows the measurement of f_{sensor} from -40 °C to +90 °C. Due to the unstable serial communication between the MCU and the chip f_{sensor} at negative temperature, the data points from -20 °C to -35 °C are discarded. The results of a 4th-order polyfit function shows the frequency deviation of each order in Fig. 4.6. If the 1st-order and 2nd-order temperature variation can be fully cancelled, the total residue temperature variation is at least 129 ppm. The result of a 2nd-order polyfit is shown in Fig. 4.7. With the information of $\alpha_{2,\mathrm{opt}}$(FR(T)), the compensated TCO runs stably around 37.5 MHz and the residue error across the whole temperature range is 855 ppm, as shown in Fig. 4.8.

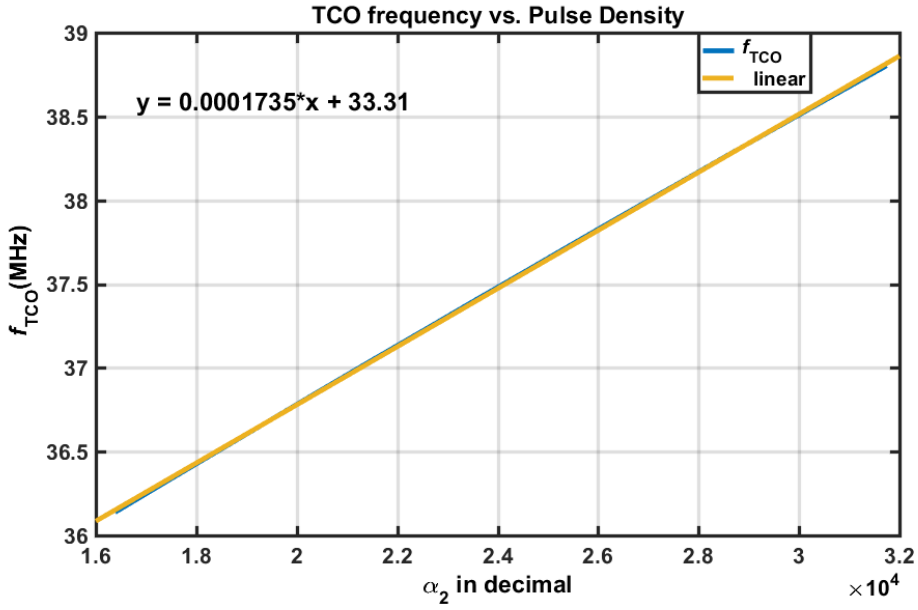


Figure 4.3: TCO frequency versus α_2 at 25 °C

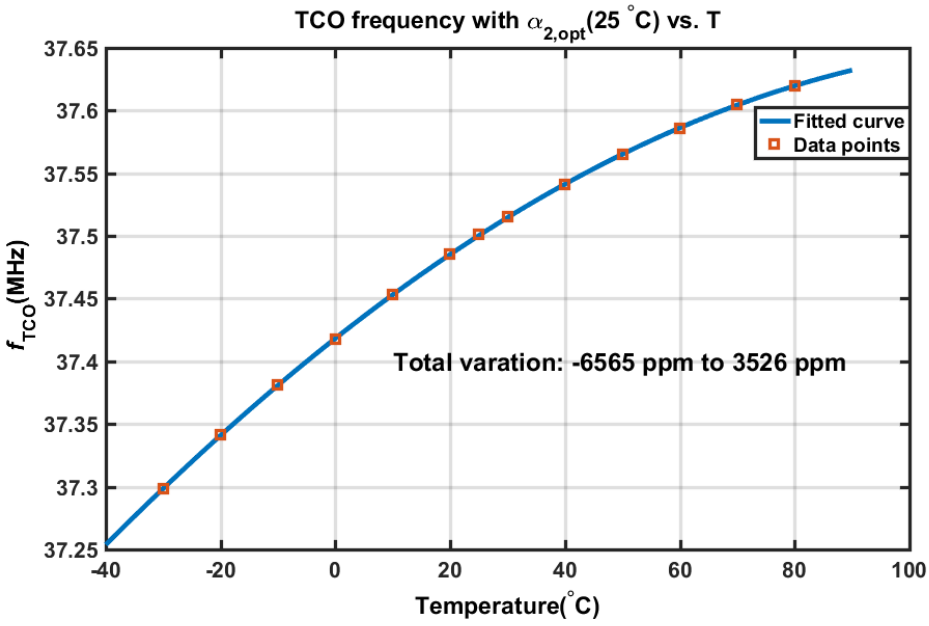


Figure 4.4: TCO frequency versus temperature with α_2=$\alpha_{2,0}$

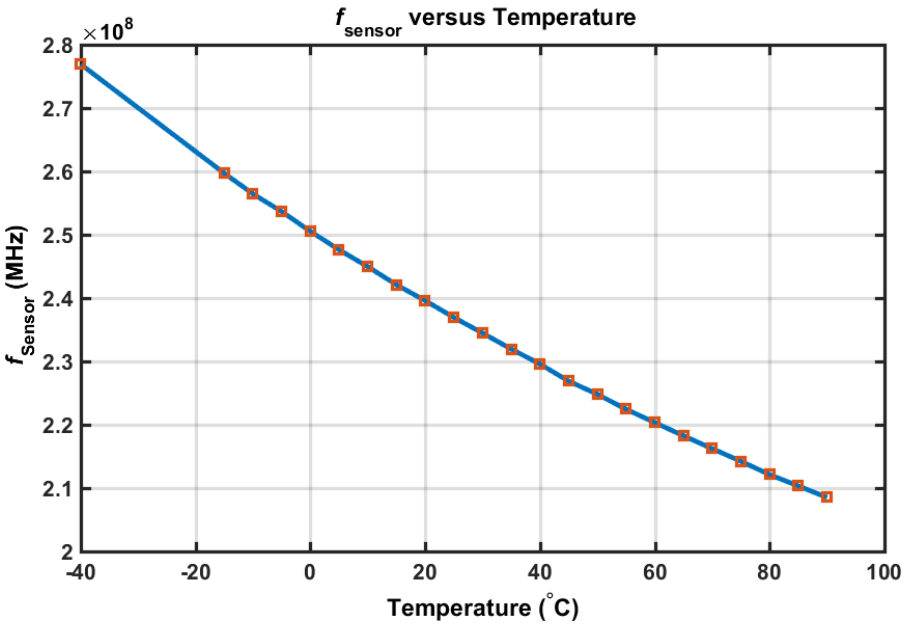


Figure 4.5: Sensor frequency versus temperature

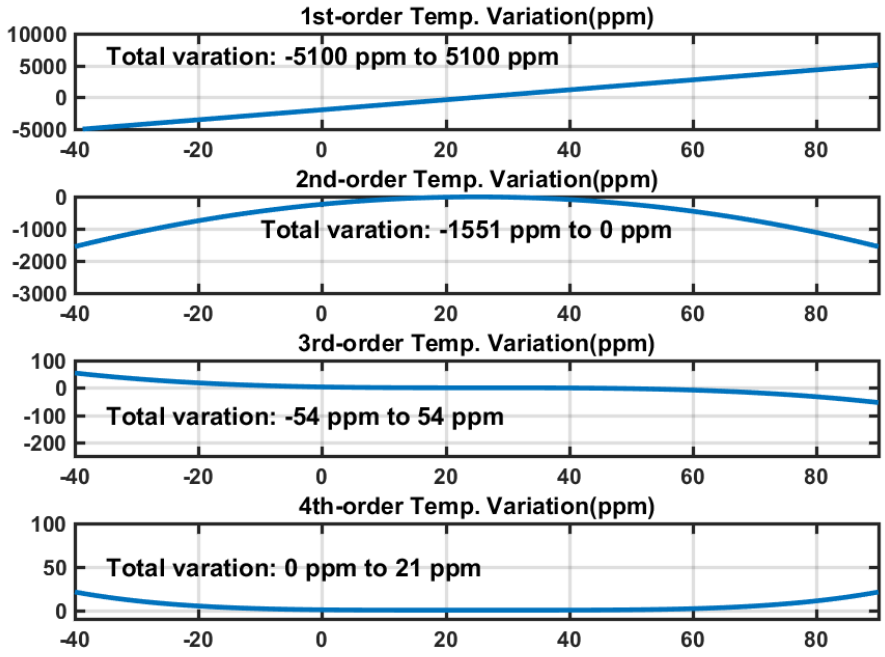


Figure 4.6: TCO frequency temperature variation by order

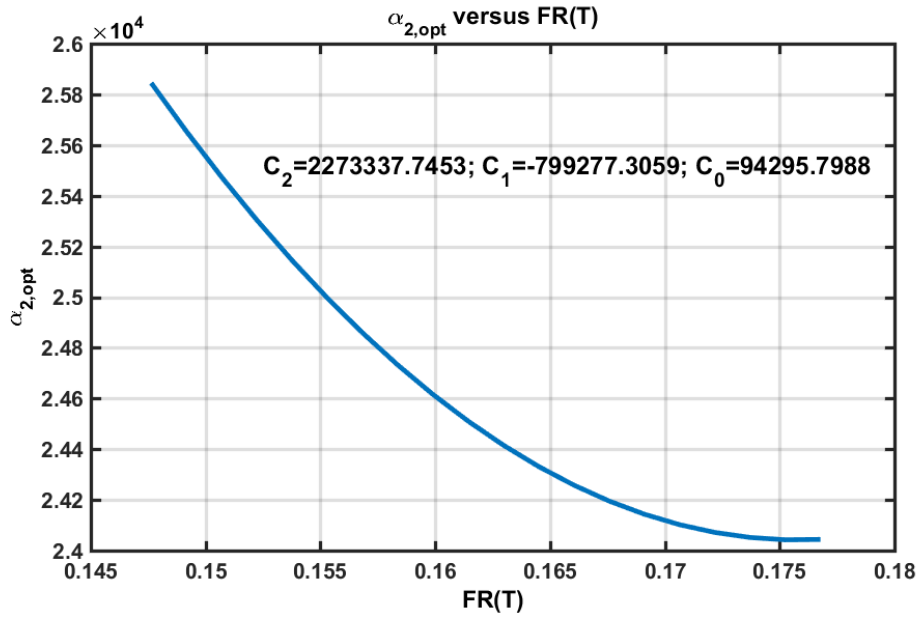


Figure 4.7: $\alpha_{2,\text{opt}}$ versus FR(T)

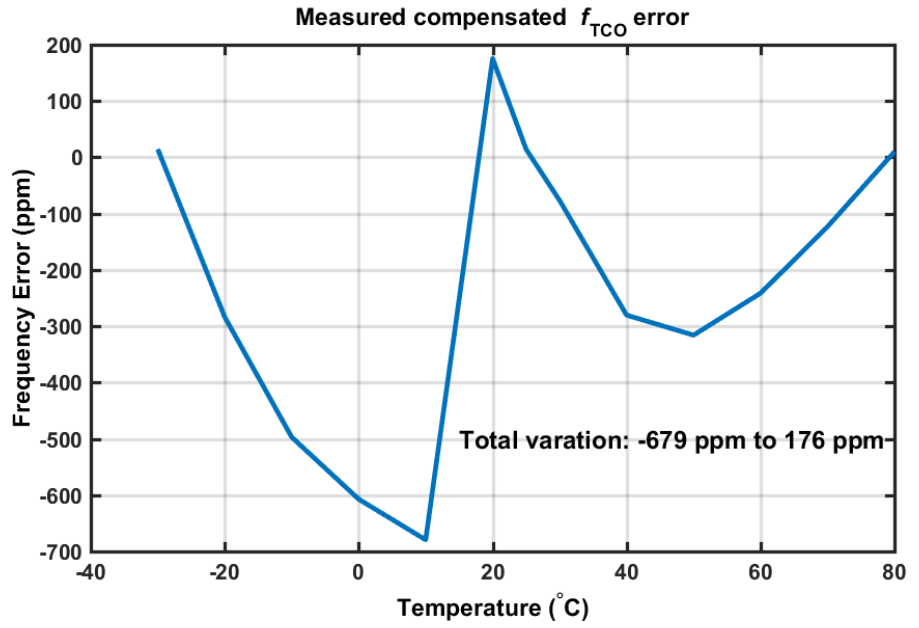


Figure 4.8: $f_{\text{TCO}}(\alpha_{2,\text{opt}}, \text{T})$ error in ppm versus temperature

CHAPTER 5

SUMMARY

5.1 Remaining Challenges

Results of this work demonstrate good stability across a wide temperature range, while there are still two factors not discussed: mechanical stress and aging

The piezoresistive effect of semiconductors makes the on-chip resistor vulnarable to mechanical shocks. To the best of the author's knowledge, only in [8] is the mechanical influence on RC-based oscillator evaluated, and the temperature stability deteriorates from 3.2 ppm/°C to 14.2 ppm/°C.

The aging of analog ICs is well explained in [17]. Effects like time-dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and hot carrier degradation (HCD) can cause aged MOSFETs to behave differently. The aging effect is especially pronounced in advanced technology nodes. The aging for analog blocks can be alleviated by auto-zeroing or chopping, because the major aging effect on analog circuitry is the change in offset voltage. A bigger issue for RC-based on-chip oscillators is the aging of on-chip resistors. Unfortunately, the aging of on-chip resistors is not well explained or modelled to the accuracy of interest of several hundreds of ppm. In a recent research by NXP Semiconductor [18], there is no clear evidence whether the resistances of the aged on-chip resistors will increase or decrease. There are researches on self-healing electronics systems, mainly RF transceiver systems, that can

counteract aging of components, but these systems require large computation units and sophisticated algorithms which are beyond the scope of this work.

5.2 Conclusion

This work shows the effectiveness of using a temperature sensor to compensate an on-chip RC-based oscillator. For one oscillator chip, in total 855 ppm is observed across the whole temperature range, even when the MCU communication has bugs at low temperature. Better results should be expected if the communication problem can be solved. Furthermore, it will be promising to implement this work as one chip without the computer and frequency counter.

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