April 2005

UILU-ENG-05-2207
DAC-102

LINEAR ANALOG FRONT-END CIRCUITS FOR FIBER-OPTIC COMMUNICATION SYSTEMS

Hyeon-Min Bae

Coordinated Science Laboratory
1308 West Main Street, Urbana, IL 61801
University of Illinois at Urbana-Champaign

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	17 March 2005	

4. TITLE AND SUBTITLE
Linear Analog Front-End Circuits for Fiber-Optic Communication Systems

5. FUNDING NUMBERS
INTEL

6. AUTHOR(S)
Bae, Hyeon-Min

7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(ES)
Coordinated Science Laboratory
University of Illinois at Urbana-Champaign
1308 W Main St
Urbana, IL 61801

8. PERFORMING ORGANIZATION REPORT NUMBER
UILU-ENG-05-2207 (DAC 102)

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
INTEL

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

Transmission of 10-Gb/s data rates or higher over fiber links installed as late as the mid-1990s is limited by impairments such as chromatic dispersion (CD) and polarization mode dispersion (PMD). Both forms of dispersion result in intersymbol interference (ISI) in the received signal. Electronic dispersion compensation (EDC) is cost-effective and technically superior to optical approaches. Unlike conventional clock-data recovery circuits (CDRs), an EDC-based architecture requires a *linear* analog front-end. Furthermore, large scale integration requires low supply voltage operation for power reduction. Existing analog front-ends are nonlinear or require high supply voltage, and hence are not suitable for EDC-based receivers.

We propose optical front-end circuits suitable for electronic dispersion compensation (EDC) based fiber-optic communication systems.

First, a CMOS based wideband linear transimpedance front-end design technique is presented. The key idea behind the proposed transimpedance amplifier (TIA) is to compensate for the dominant pole created by the large input node capacitance using transconductance peaking. The proposed technique improves gain-bandwidth product without impacting noise and headroom. A process-insensitive variable gain amplifier (VGA) design is also proposed and integrated with the TIA. Linearity of the VGA is achieved without incorporating degeneration, resulting in wide bandwidth. The overall TIA-VGA circuit demonstrates a tunable transimpedance in the range 57dBΩ to 87dBΩ, a -3-dB bandwidth of 1.4 ± 0.1 GHz, SFDR > 19dB while maintaining an output swing of $500mV_{pp}$ in a standard 2.5-V, 0.25-μm CMOS process.

Second, a variable gain amplifier is designed for electronic dispersion compensation based 10-Gb/s optical links. The design incorporates tunable emitter degeneration, hence satisfying linearity, bandwidth, and supply voltage requirements. Also, an analog multiplexer provides a wide gain tunability and enhanced linearity. The VGA achieves tunable gain from 2.43dB to 44.37dB while being process insensitive; a worst case spurious free dynamic range of 26.46dB with an output swing of $1.4V_{pp}$, and minimum 3-dB bandwidth of 6.5 GHz consumes 102mW of power in a 3.3-V, 0.25-μm SiGe BiCMOS process.

14. SUBJECT TERMS	15. NUMBER IF PAGES
TIA, VGA, optical, SiGe, CMOS, ADC	76
	16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

LINEAR ANALOG FRONT-END CIRCUITS FOR FIBER-OPTIC COMMUNICATION SYSTEMS

BY

HYEON-MIN BAE

B.S., Seoul National University, 1998
M.S., University of Illinois at Urbana-Champaign, 2001

DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2004

Urbana, Illinois

a -3-dB bandwidth of 1.4 ± 0.1 GHz, SFDR > 19 dB while maintaining an output swing of $500\,\mathrm{mV_{pp}}$ in a standard 2.5-V, 0.25-μm CMOS process.

Second, a variable gain amplifier is designed for electronic dispersion compensation based 10-Gb/s optical links. The design incorporates tunable emitter degeneration, hence satisfying linearity, bandwidth, and supply voltage requirements. Also, an analog multiplexer provides a wide gain tunability and enhanced linearity. The VGA achieves tunable gain from 2.43 dB to 44.37 dB while being process insensitive; a worst case spurious free dynamic range of 26.46 dB with an output swing of $1.4\,\mathrm{V_{pp}}$, and minimum 3-dB bandwidth of 6.5 GHz consumes 102 mW of power in a 3.3-V, 0.25-μm SiGe BiCMOS process.

ACKNOWLEDGMENTS

First, I would like to express my gratitude to my advisor, Prof. Naresh Shanbhag, for his constant encouragement and guidance. His support enabled me to expand on my idea and add depth to the work. His assistance and patience were instrumental to the completion of this thesis.

Also, I would like to thank my colleagues with whom I shared many insightful talks and who supported me throughout my graduate years.

Special thanks go to my family - Haeyoung, Soonmi, and Lisa - whose unceasing love and support enabled me to concentrate on my work and make it through.

Lastly, I would like to thank my wife and lifelong friend Wonsun for her faith in me.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION AND MOTIVATION

In this chapter, we discuss general principles and limitations of conventional fiber-optic communication systems. Figure 1.1 shows a generic optical communication link.

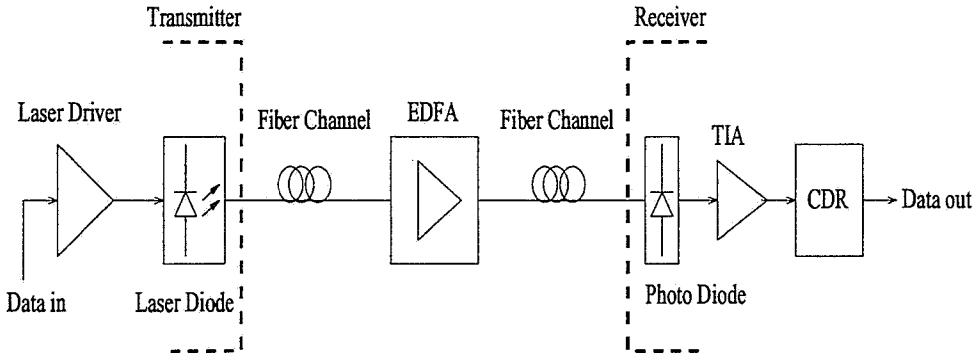


Figure 1.1 An optical communication link.

In the transmitter, the modulator converts binary input data into an optical signal that is launched into the optical fiber. At the receiver, the optical signal from the fiber is incident on an optical-to-electrical converter such as photodiode (PD). The output of the PD is a weak current signal, which is converted to voltage and amplified by a transimpedance amplifier (TIA). The output of the TIA is amplified again by limiting amplifiers because it is not large enough for threshold detection. The clock-data recovery (CDR) unit then recovers the timing information from the signal and employs it to threshold the signal at an appropriate sampling instance in order to determine the trans-

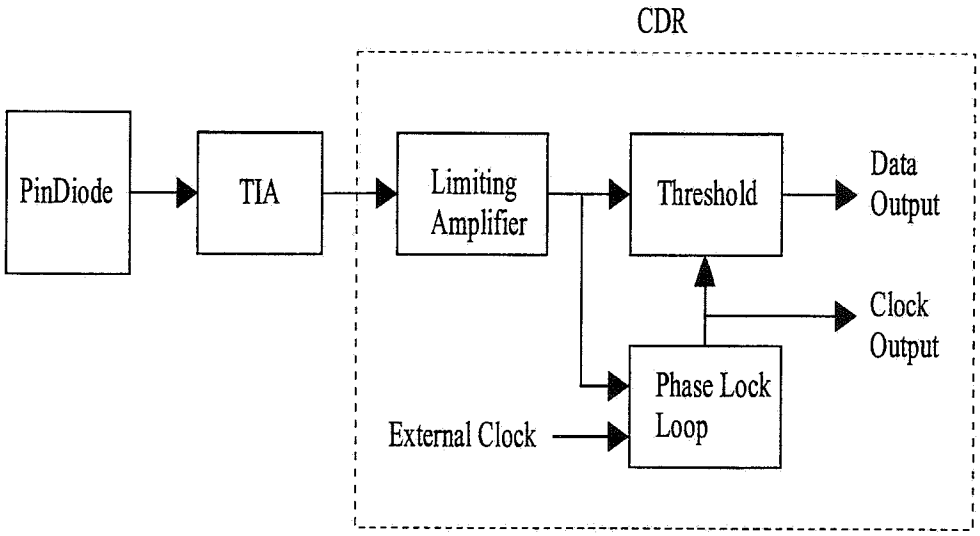


Figure 1.2 A clock-data recoverty system.

mitted data bits. Figure 1.2 shows a generic block diagram of a conventional clock-data recovery system.

Next-generation optical communication systems are expected to employ significant amounts of signal processing techniques at the receiver to overcome optical fiber impairment such as polarization mode dispersion (PMD) and chromatic dispersion (CD) especially at 10 Gb/s and beyond. As PMD is a random effect due to the asymmetry and fluctuating stresses in a fiber, adaptive digital signal processing [1–3] becomes a good candidate for compensation in optical fiber communications.

Transmission of OC-192 (10 Gb/s) data rates over fiber links installed as late as the mid-1990s is limited by impairments such as chromatic dispersion (CD) and polarization mode dispersion (PMD). Both forms of dispersion result in intersymbol interference (ISI) in the received signal. Electronic dispersion compensation (EDC) [1] has recently received significant attention as being cost-effective and technically superior to optical approaches. Architectures for EDC-based receivers include feed-forward equalizer

(FFE), decision-feedback equalizer (DFE), and maximum-likelihood sequence estimator (MLSE). Unlike conventional clock-data recovery circuits (CDRs), an EDC-based architecture (see Fig. 1.3) requires a *linear* analog front-end comprising of a variable gain amplifier (VGA), and potentially an analog-to-digital converter (ADC), in addition to a clock recovery subsystem. Large scale integration requires low supply voltage operation for power reduction. Existing 10-Gb/s limiting amplifier structures [4] are nonlinear, and hence are not suitable for EDC-based receivers. A few variable gain amplifiers [5] are reported; however, they cannot be employed either due to the need for a large supply voltage and nonlinearity.

However, as electronic dispersion compensation (EDC) based optical communication systems require sufficient linearity in front-end designs, conventional nonlinear front-end designs cannot be utilized. Front-end circuits in EDC based fiber-optic communication need to be linear over the entire input power range. This is because CD and PMD are determined by the length of the optical fiber while the optical power is determined by the distance between the erbium-doped fiber-amplifiers (EDFAs) and the receiver, which means that the input signal power and dispersion are not related. In this thesis, we present design techniques to improve the bandwidth while maintaining linearity of the TIA and the VGA shown in Fig. 1.3.

1.1 Introduction

The performance of any communication link can be characterized via the bit-error-rate (BER). An important parameter that is indicative of receiver performance is *receiver sensitivity*, usually defined as the minimum received optical power at which the

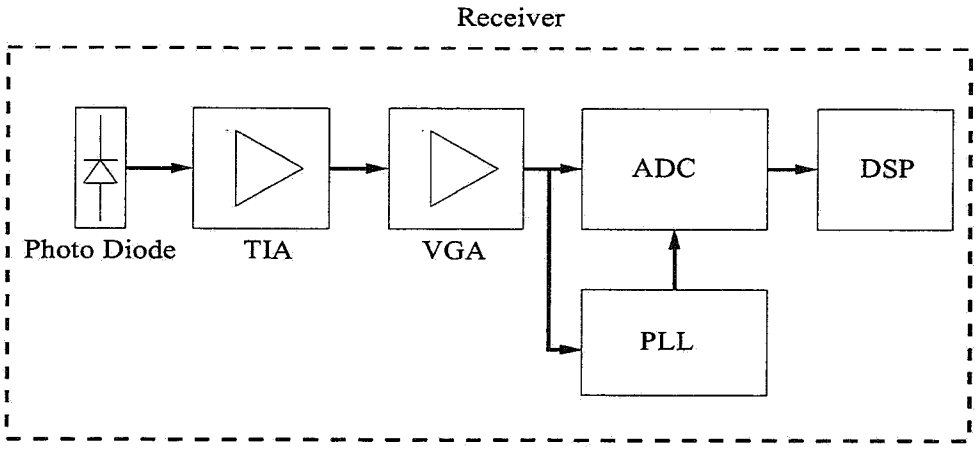


Figure 1.3 A next generation EDC-based receiver for optical links.

BER is 10^{-9}. Receiver sensitivity depends upon the signal-to-noise ratio (SNR), which in turn depends on various noise sources that corrupt the received signal.

1.2 Bit-Error Rate

Figure 1.4 shows the received current signal at the input of the decision circuit. The decision circuit samples its input at the center of the bit period which is determined by the clock recovery unit. The sampled value fluctuates between average values $I(0)$ and $I(1)$ and the decision circuit compares it with threshold value $I(D)$. The BER is defined as

$$BER = p(1)p(0 \mid 1) + p(0)p(1 \mid 0), \tag{1.1}$$

where $p(1)$ and $p(0)$ are the probabilities that the transmitted bit is a '1' or a '0', respectively, $p(0 \mid 1)$ is the probability that the decision device decides a '0' when a '1' was transmitted, and $p(1 \mid 0)$ is the probability that the decision device decides a '1' when a '0' was transmitted. Since '1' and '0' bits are equally likely to occur, $p(0) = p(1) = \frac{1}{2}$.

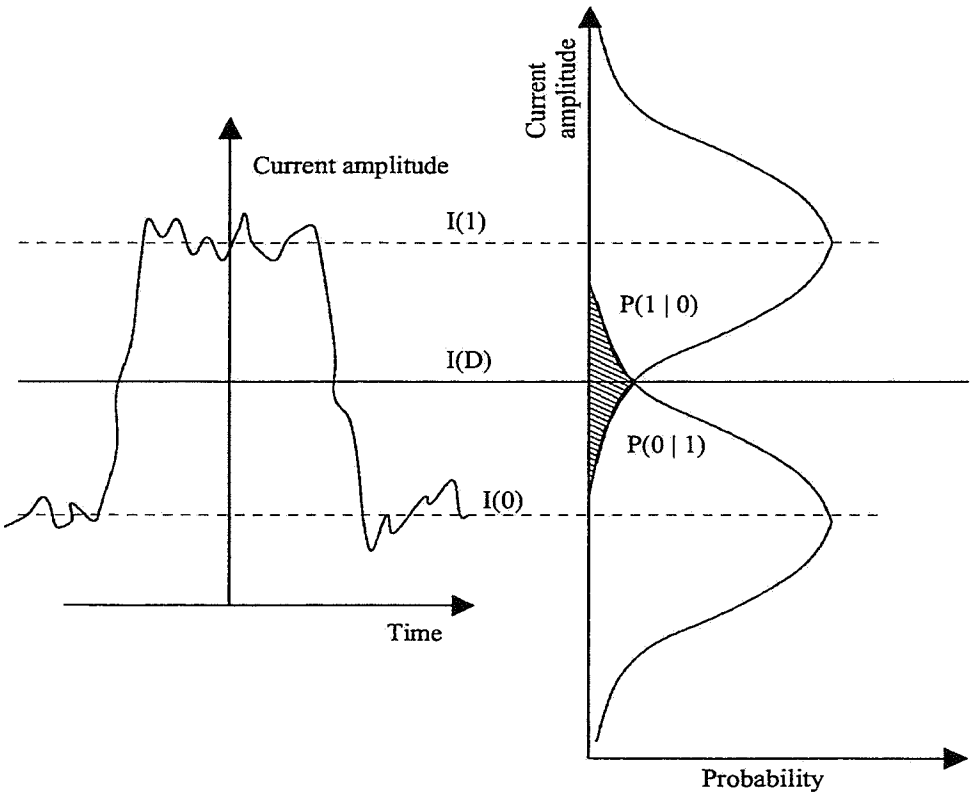


Figure 1.4 Received signal in presence of additive white Gaussian noise.

The functional form of $p(I)$, where I is sampled value, depends on the statistics of noise sources. The major noise sources in the receiver are thermal and shot noise. Both noise sources can be regarded as independent Gaussian random processes. Thermal noise has zero mean and a variance of σ_T^2. Shot noise, however, exhibits different variances for a '0' and a '1'. This is because the shot noise variance σ_s^2 is given by

$$\sigma_s^2 = 2q(I_p + I_d)\Delta f, \tag{1.2}$$

where q is electron charge, I_p data dependent output current, and I_d is photo detector dark current. As I_p is greater when a '1' is transmitted than when a '0' is transmitted, $\sigma_{s,1} >$

$\sigma_{s,0}$, where $\sigma_{s,1}^2$ and $\sigma_{s,0}^2$ are the shot noise variances when a '1' or a '0' is transmitted, respectively. Since the sum of two Gaussian random variables is also a Gaussian random variable, the sampled value I has a Gaussian probability density function with variance $\sigma^2 = \sigma_T^2 + \sigma_s^2$. However, the noise variance for a transmitted '1' and '0' will be different as shown in (1.2). If σ_1^2 and σ_0^2 are corresponding noise variances for data '1' and '0', respectively, the conditional probabilities are given by

$$p(0 \mid 1) = \frac{1}{\sigma_1\sqrt{2\pi}} \int_{-\infty}^{I(D)} exp(-\frac{(I - I(1))^2}{2\sigma_1^2})dI \tag{1.3}$$

$$p(1 \mid 0) = \frac{1}{\sigma_0\sqrt{2\pi}} \int_{I(D)}^{\infty} exp(-\frac{(I - I(0))^2}{2\sigma_0^2})dI. \tag{1.4}$$

The BER is given by

$$\frac{1}{4}\{erfc(\frac{I(1) - I(D)}{\sigma_1\sqrt{2}}) + erfc(\frac{I(D) - I(0)}{\sigma_0\sqrt{2}})\}, \tag{1.5}$$

where the error function $erfc(x)$ is defined as

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^{\infty} exp(-y^2)dy. \tag{1.6}$$

It is clear that the BER is dependent on the threshold $I(D)$. The minimum BER occurs when the threshold $I(D)$ is chosen such that:

$$\frac{I(1) - I(D)}{\sigma_1} = \frac{I(D) - I(0)}{\sigma_0} = Q, \tag{1.7}$$

where Q is sometimes referred to as the "eye opening." The explicit expression for $I(D)$ can be derived from (1.7) as

$$I(D) = \frac{\sigma_0 I(1) + \sigma_1 I(0)}{\sigma_0 + \sigma_1}. \tag{1.8}$$

Substituting (1.7) into (1.5) results in

$$BER = \frac{1}{2} erfc(\frac{Q}{\sqrt{2}}), \tag{1.9}$$

where

$$Q = \frac{I(1) - I(0)}{\sigma_1 + \sigma_0}. \tag{1.10}$$

For a BER of 10^{-9}, Q $\approx$ 6. Usually, thermal noise dominates the noise response and the threshold $I(D) = \frac{I(0)+I(1)}{2}$. In this case, $\sigma_0 = \sigma_1$ and $Q = \frac{I(1)}{2\sigma_1}$. By noting that

$$SNR = \frac{I(1)^2}{\sigma_1^1}, \tag{1.11}$$

$SNR = 4Q^2$. For a BER of 10^{-9}, the SNR should be at least 21.6 dB.

The sensitivity analysis shown above is applicable in a noise-dominated scenario. In presence of other nonidealities such as dispersion, the minimum average optical power required by the receiver to achieve the same BER increases. This increase in the average received power necessary to achieve the same BER is referred to as the *power penalty.* An EDC-based optical receiver reduces power penalty. Therefore, the sensitivity of ideal EDC-based optical receiver is higher than that of conventional CDR in presence of dispersion.

1.3 Dispersion

At high data rates, several impairments degrade the quality of the signal as it traverses the link. These impairments lead to erroneous decision by the CDR and hence an increase in the BER of the link. The sources of impairments in an optical link other than noise are attenuation, reflection, dispersion, timing jitter in CDR, and PIN diode extinction ratio. The extinction ratio in PIN diode is the ratio between on-state power and off-state power. Two main sources of dispersion in the optical link are polarization mode dispersion (PMD) and chromatic dispersion (CD). Other possible sources of dispersion include laser chirp, finite bandwidth of the optical filters, PIN diode and the TIA. In next-generation (10-GHz) optical communication systems, CD and PMD are two major sources of sensitivity degradation.

1.3.1 Chromatic dispersion

Chromatic dispersion (CD) occurs in both single-mode and multimode optical fibers. Chromatic dispersion occurs because different wavelengths of light travel through the fiber at different speeds. The transfer function $H(f)$ due to CD [6] is given by

$$H(f) = exp(\frac{-j\pi DL\lambda^2 f^2}{c}), \tag{1.12}$$

where λ is the center wavelength, c is the speed of light, L is the length of the fiber and D is the chromatic dispersion index specified in ps/nm/km. Typical values of these variables are: $\lambda = 1550\,\text{nm}$, $c = 3 \times 10^3\,\text{m/s}$, $L = 200\,\text{km}$, and $D = 17\,\text{ps/nm/km}$.

Chromatic dispersion is sometimes referred to as group delay dispersion or intramodal dispersion.

1.3.2 Polarization mode dispersion

Polarization mode dispersion (PMD) occurs due to the asymmetry of the fiber-optic strand. Fiber asymmetry may be induced by the manufacturing process, or may be a result of mechanical stress on the deployed fiber. The inherent asymmetries of the fiber are fairly constant over time, while the mechanical stress due to movement of the fiber can vary, resulting in PMD having a time-varying component.

The mechanical stress on optical fibers can originate from a variety of sources. One source that is very difficult to control is the diurnal (day/night) and seasonal heating and cooling of the optical fiber. Although much fiber is deployed in the ground and often within conduits, it is subject to temperature variations and corresponding mechanical stress.

Another source of mechanical stress can originate from nearby sources of vibration. For example, much fiber is deployed alongside railroad tracks because of the ease of right-of-way and construction. However, vibrations from passing trains can contribute to stress on the optical fiber. Fiber that is not buried next to railways and highways may be deployed aerially; in this scenario, wind can cause swaying of the fiber cable and can contribute to PMD.

Because of the combination of these effects, and the random manner in which these effects add up over a section of fiber, PMD does not have a single value for a given section of fiber. Rather, it is described in terms of an average differential group delay (DGD).

DGD refers to the difference in arrival time of two light pulses launched into a fiber with PMD along orthogonal polarization modes. Furthermore, a fiber has a distribution of DGD values over time. DGD is usually measured in picoseconds. The probability of the DGD of a fiber section being a certain value at any particular time follows a Maxwellian distribution. As an approximation, the maximum instantaneous DGD is about 3.2 times the average DGD of a fiber. Note that both CD and PMD result in intersymbol interference.

1.4 Organization of the Thesis

This thesis begins with a presentation of linear CMOS transimpedance amplifier design in Chapter 2. Chapter 3 presents a CMOS variable gain amplifier design with emphasis on linearity and bandwidth along with results from testing a prototype chip in 0.25-μm CMOS process that incorporates both the proposed TIA and VGA design. Chapter 4 presents a silicon germanium (SiGe) BiCMOS variable gain amplifier design with threshold voltage insensitive gain control scheme, wide variable gain range, and linearity. The last chapter summarizes the conclusions drawn from each section and points to future work.

CHAPTER 2

CMOS TRANSIMPEDANCE AMPLIFIER DESIGN

In this chapter, we propose a wideband linear transimpedance amplifier (TIA) design technique. The proposed technique enhances the gain-bandwidth product of the TIA by a factor of 3 over the commonly employed common-source shunt feedback structure without impacting the input-referred current noise and voltage headroom. A linear variable gain amplifier, which is presented in Chapter 3, is designed and integrated with the proposed TIA, so that it can be employed as a front-end in electronic dispersion compensation (EDC) based receiver in optical fiber links.

Conventional optical front-end requirements are high bandwidth (usually 0.7 times the date rate) and low noise ($SNR > 21\,\text{dB}$ for $BER < 10^{-9}$). However, a front-end with sufficient linearity and low noise is essential for proper analog-to-digital conversion or analog domain equalization. The signal-to-noise plus distortion ratio ($SNDR$) needs to be at least 18 dB if the receiver employs maximum likelihood detection [1].

The proposed TIA circuit technique is implemented in a standard 2.5-V, 0.25-μm CMOS process. The TIA is designed to have sufficient voltage headroom so that the design can be scaled in future nanometer CMOS processes. Figure 2.1 shows the block diagram of the proposed variable gain linear transimpedance front-end. The TIA and VGA are DC coupled. As the TIA is sensitive to noise, we place an offset cancellation

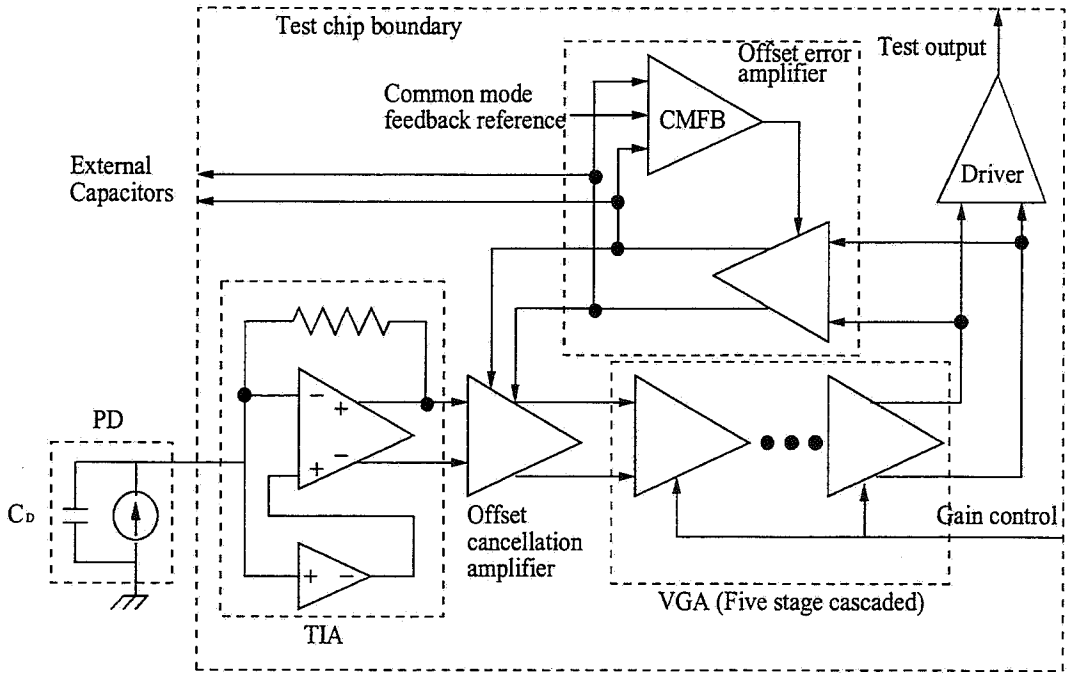


Figure 2.1 The block diagram of the linear variable gain transimpedance front-end.

block between the TIA and the VGA in order to prevent noise from coupling into the TIA. A fully differential-to-single ended 50-Ω driver is employed at the output stage for testing purposes. The gain of the 50-Ω driver is set to 0.7 in order to have sufficient bandwidth. Note that the output capacitance C_D of the pin diode is 0.25 pF-1 pF. It is this capacitance that eventually limits the bandwidth of the TIA.

In this chapter, we first explore the existing TIA designs. Second, we present the proposed TIA. Third, we analyze the noise response of TIA and conclude with simulation results for the proposed TIA.

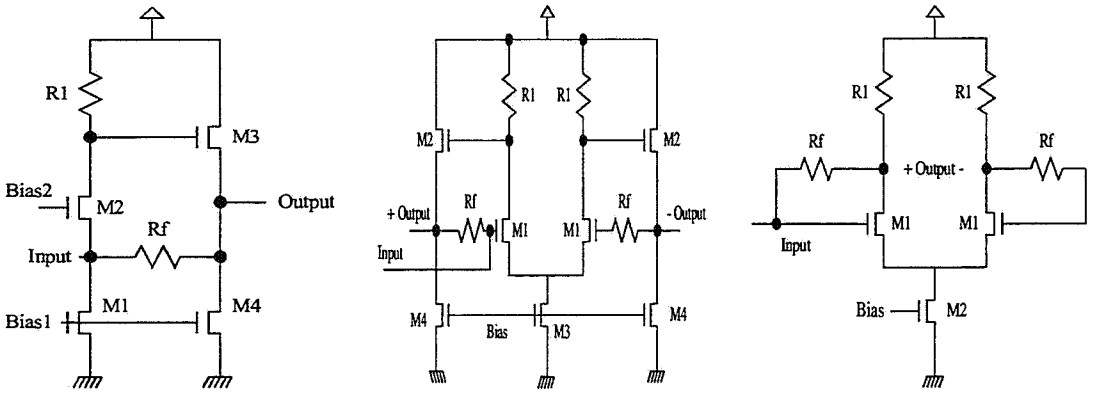


Figure 2.2 Existing transimpedance amplifier structures: (a) common gate, (b) two-stage common-source, and (c) single-stage common-source.

2.1 Existing TIAs

Figure 2.2 shows existing TIA structures. The common gate TIA (see Fig. 2.2(a)) [7,8] has relatively low open-loop input impedance, which results in a high closed-loop bandwidth. However, noise currents of R1 and M2 are directly reflected into the input deteriorating the noise performance. Stability and headroom constraints limit the size of R1, resulting in a noise-gain trade-off. The two-stage common-source feedback TIA [9–11] (see Fig. 2.2(b)) is the most commonly employed TIA structure. Low open-loop output impedance provides a high closed-loop bandwidth; however, reduced voltage headroom limits noise and bandwidth. From 2.2(b), we recognize that the gate-to-source potential of transistors M1 and M2 significantly constrains the DC drop across R1, thereby limiting the open-loop gain and raising the noise contributed by R1 and M2. Furthermore, the poles at the input node, the drain of M1, and the output node make it hard to achieve desirable phase margin. Capacitor peaking [12] is usually employed to enhance

the bandwidth at the expense of the phase margin. A disadvantage of the capacitor peaking technique is that phase margin can become very small in the presence of process variations. Single-stage common-source TIA [13–17] (see Fig. 2.2(c)) has relaxed headroom constraints, making it suitable for deep submicron CMOS processes. However, its relatively high open-loop output impedance limits the closed-loop bandwidth. Extra cascaded open loop gain stages have been proposed to overcome bandwidth limitations in this structure [13,14]. However, the absence of feedback in the additional stages degrades linearity.

Thus, the challenge in TIA design is to achieve high gain-bandwidth product while maintaining a common-source single-stage feedback structure to avoid headroom problems without sacrificing the linearity and noise performance.

2.2 Proposed TIA

We propose the idea of *transconductance peaking* to compensate for the dominant pole created by the large input capacitance C_D. Figure 2.3 shows the transistor-level schematic of the proposed TIA. Amplifier A_0 is a single-stage common-source feedback TIA and A_1 creates a parallel signal path with a left half-plane (LHP) zero. The LHP zero is implemented using a simple common-source amplifier with an active inductor load [18]. As the maximum output swing of TIA is 500-mV peak-to-peak differential, the feedback resistor is implemented using an n-well instead of a transistor due to the linearity and bandwidth requirement.

The small-signal model of the proposed TIA without the source follower (M_C, M_2) is shown in Fig. 2.4.

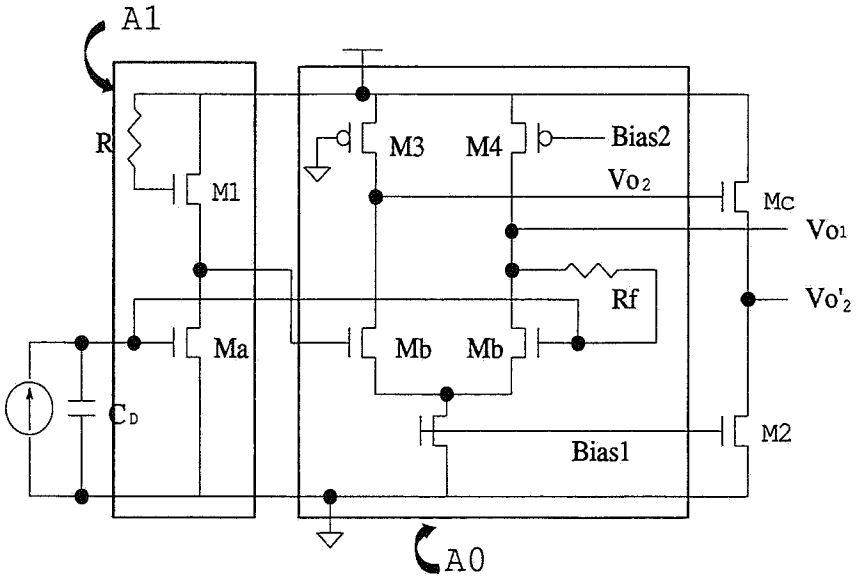


Figure 2.3 Schematic of the proposed TIA.

Applying KCL at the input node, we get

$$i_{in} = sC_{tot}V_{in} + \frac{V_{in} - V_{o1}}{R_f}, \tag{2.1}$$

where C_{tot} is the total input capacitance, R_f is the feedback resistance, V_{in} is the input voltage, V_{o1} is output voltage, and i_{in} is the input current. Similarly, at the output nodes V_{o1} and V_{o2}, we get

$$g_{m,p}V_{in} + \frac{V_{o1}}{Z_1} + \frac{V_{o1} - V_{in}}{R_f} = 0, \tag{2.2}$$

$$V_{o2} = g_{m,p}V_{in}Z_2, \tag{2.3}$$

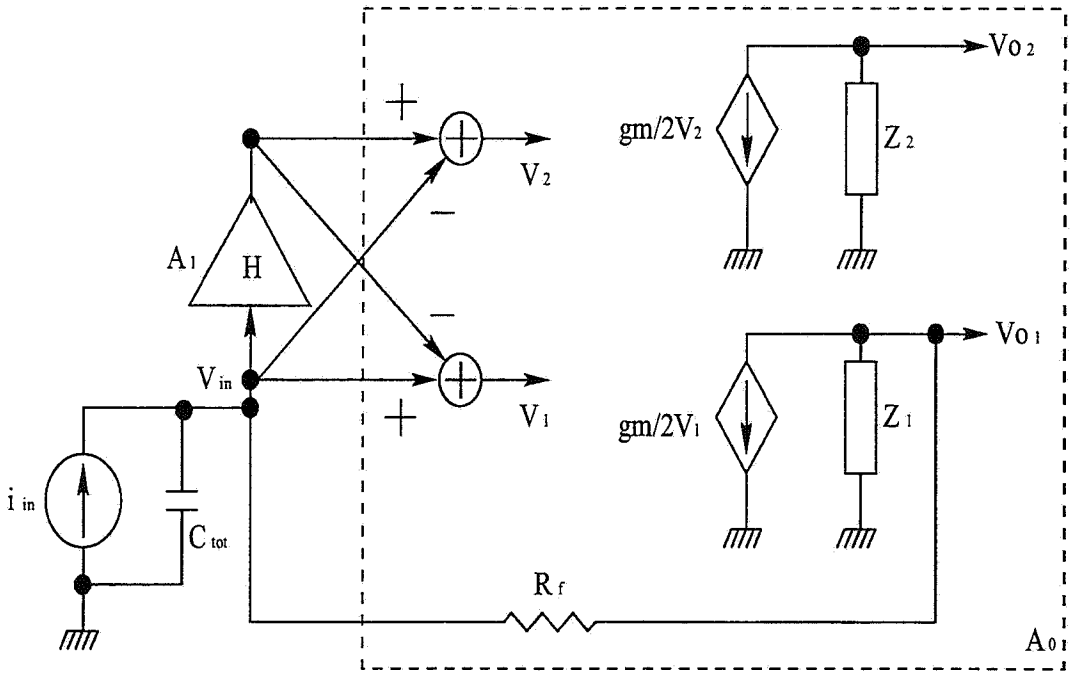


Figure 2.4 Small-signal block diagram of the proposed TIA without the source follower output stage.

where

$$g_{m,p} = \frac{g_m}{2}(1 - H). \tag{2.4}$$

Here, g_m is the transconductance, H is the transfer function of amplifier A_1, and Z_1 and Z_2 are the output loads. The transfer function $T_1 = \frac{V_{o1}}{i_{in}}$ can be derived from (2.1) and (2.2) by eliminating V_{in}. The transfer function T_1 is given by

$$T_1 = \frac{-R_f(g_{m,p}R_f - 1)}{g_{m,p}R_f - 1 + (\frac{R_f}{Z_1} + 1)(sC_{tot}R_f + 1)}. \tag{2.5}$$

If $H = -1$, (2.5) represents the transfer function of a conventional single-stage common-source transimpedance amplifier.

In order to compare the closed loop behavior of the conventional single-stage common-source TIA and the proposed TIA, we decompose (2.5) into separate forward a and feedback b gain [19] as follows:

$$\begin{aligned} T_1 &\approx \frac{a}{1+af}, \\ a &= -\frac{g_{m,p}}{((sC_{tot}+\frac{1}{R_f})(\frac{1}{Z_1}+\frac{1}{R_f}))}, \\ f &= -\frac{1}{R_f}, \end{aligned} \tag{2.6}$$

where we make the assumption $g_{m,p}R_f >> 1$.

Figure 2.5 shows the root locus for conventional single-stage TIA and proposed TIA, where the transfer function of H is assumed to have one pole and one zero:

$$H = B\frac{1+\frac{s}{Z_H}}{1+\frac{s}{P_H}}, \tag{2.7}$$

where $B < 0$, $|Z_H| < |P_H|$. The closed-loop zero $Z1'$ can be obtained by substituting (2.7) into (2.6) as

$$Z1' \approx P_H\frac{(1-B)Z_H}{Z_H - BP_H}. \tag{2.8}$$

A left half-plane zero is inserted between dominant poles by selecting B and Z_H properly. The left half-plane zero $Z1'$ inserted by A_1 attracts dominant pole at the input node. Further, the high-frequency pole of A_1 interacts with the nondominant pole of A_0 to generate closed loop complex poles. As a result, the bandwidth is increased.

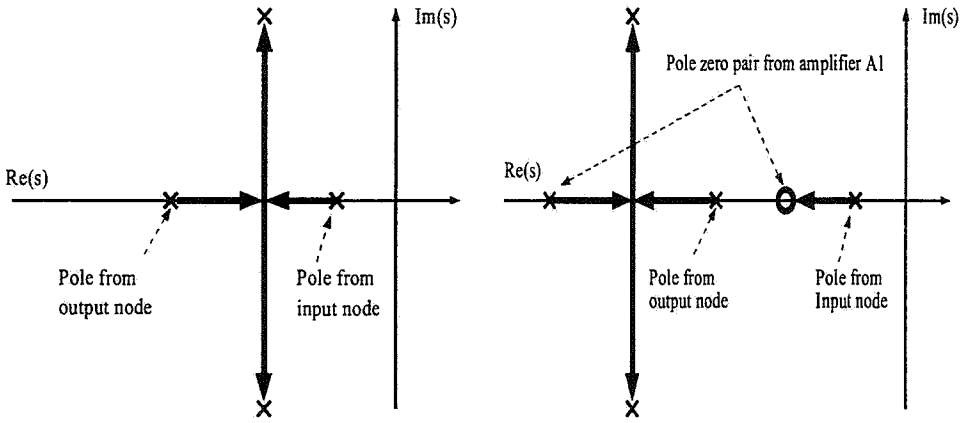


Figure 2.5 Root locus of (a) single stage common-source feedback TIA, and (b) that of the proposed TIA.

The transfer function $T_2 = \frac{V_{o2}}{i_{in}}$ is given by

$$T_2 = \frac{R_f(g_{m,p}(\frac{R_f}{Z_1}+1)Z_2)}{g_{m,p}R_f - 1 + (\frac{R_f}{Z_1}+1)(sC_{tot}R_f+1)}. \tag{2.9}$$

Additional output V_{o2} serves two purposes: one is to provide a pseudo-differential output and the other is to enhance the bandwidth and gain of $T_{diff} = T_1 - T_2$. The resistive component of Z_2 is set smaller than that of Z_1 to place an additional LHP zero in T_{diff} properly. However, the small output resistance reduces the low-frequency transimpedance gain of T_2. The low-frequency transimpedance of T_{diff} is

$$T_{diff} \approx -(1+\frac{Z_2}{Z_1})R_f + Z_2. \tag{2.10}$$

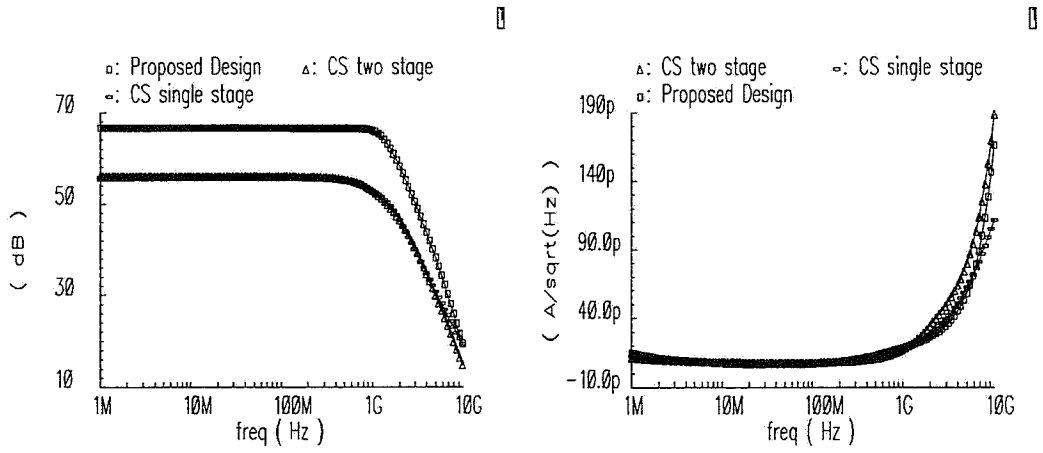
Compared to conventional designs, which have the transimpedance of $-R_f$, (2.10) is a significant increase without sacrificing bandwidth and stability.

The total input node noise current per unit bandwidth for any shunt-series feedback TIA including the proposed TIA is given by

$$i_{n,total} \approx i_n + v_n(\frac{1}{R_f} + j\omega C_D) + i_f, \tag{2.11}$$

where i_n and v_n are input-referred noise current and input-referred noise voltage of open loop amplifier, respectively; i_f is noise current of the feedback resistor; and C_D is the parasitic capacitance of the photodetector. The large feedback resistance R_f reduces the second and third terms in (2.11). In a conventional TIA with shunt feedback, R_f cannot be chosen to be arbitrarily large because R_f directly affects the closed loop pole locations and hence the bandwidth. In the proposed design, however, a properly selected left half-plane zero enables us to incorporate a relatively high feedback resistance without limiting the bandwidth.

Figure 2.6(a) and (b) show the transimpedance gain and noise performance of proposed TIA and conventional TIAs, respectively. The process technology employed in simulations is a standard 0.25-μm CMOS process with 2.5-V supply voltage. Each circuit is optimized to produce maximum gain-bandwidth product while maintaining similar noise performance. Increased feedback resistance enhances transimpedance gain and scales down additional noise generated by amplifier A_1 in Fig. 2.3. As can be seen in Figure 2.6(a), the proposed TIA has a gain-bandwidth product that is 3X better than either of the two common-source structures. Table 2.1 shows the phase margin of the proposed TIA at different process corners and with different photodetector capacitances. The worst case phase margin of 67.4° implies stability even in extreme process-temperature corner.



(a) (b)

Figure 2.6 TIA performance with 1-pF input capacitance and 200-fF output capacitance: (a) transimpedance gain, and (b) input referred current noise.

Table 2.1 Phase margin of proposed TIA in different process corners and photodetector capacitances.

Process corners	Photodetector capacitance	Phase margin
Slow, 125°	0.4 pF	67.4°
	1 pF	69.17°
Typical, 80°	0.4 pF	70.01°
	1 pF	71.87°
Fast, 25°	0.4 pF	72.61°
	1 pF	75.07°

We employ one single-ended source-follower output stage in order to reduce mismatches such as phase delay and DC voltage for the pseudo differential output signal because such mismatches have significant effect on the linearity of the VGA. The source-follower in the TIA is sized such that the phase delay is matched to within 1 % from DC to 1-GHz frequency range and the output offset voltage is less than 50 mV.

2.3 Summary

We proposed a wideband linear transimpedance amplifier (TIA) design technique. The proposed TIA design technique enhances the gain-bandwidth product by a factor of 3X over the commonly employed common-source shunt feedback structure without impacting the input referred current noise and voltage headroom.

CHAPTER 3

CMOS VARIABLE GAIN AMPLIFIER

In this chapter, we describe the design of a CMOS variable gain amplifier including the offset cancellation circuitry. Then, we present the simulation and test results of the entire linear variable gain transimpedance front-end comprised of the TIA described in Chapter 2 and the VGA described in this chapter.

3.1 Existing Designs

A nonlinear limiting amplifier is usually employed for additional amplification in a conventional clock-data recovery (CDR) system [18,20,21]. A few advanced CDRs employ a variable gain amplifier for threshold adjustment purposes [5, 13, 22, 23]. The threshold adjustment feature partially overcomes nonlinear noise characteristics of the EDFA and nonlinearity of the photo detector. In this case, the linearity of the variable gain amplifier is not important as long as the input-output characteristic is monotonic and the output signal is not clipped. However, signal processing-based optical communication systems require the variable gain amplifier to be linear over the entire input signal power range for equalization. The reasons listed above preclude conventional designs from being employed in a signal processing enhanced optical receiver.

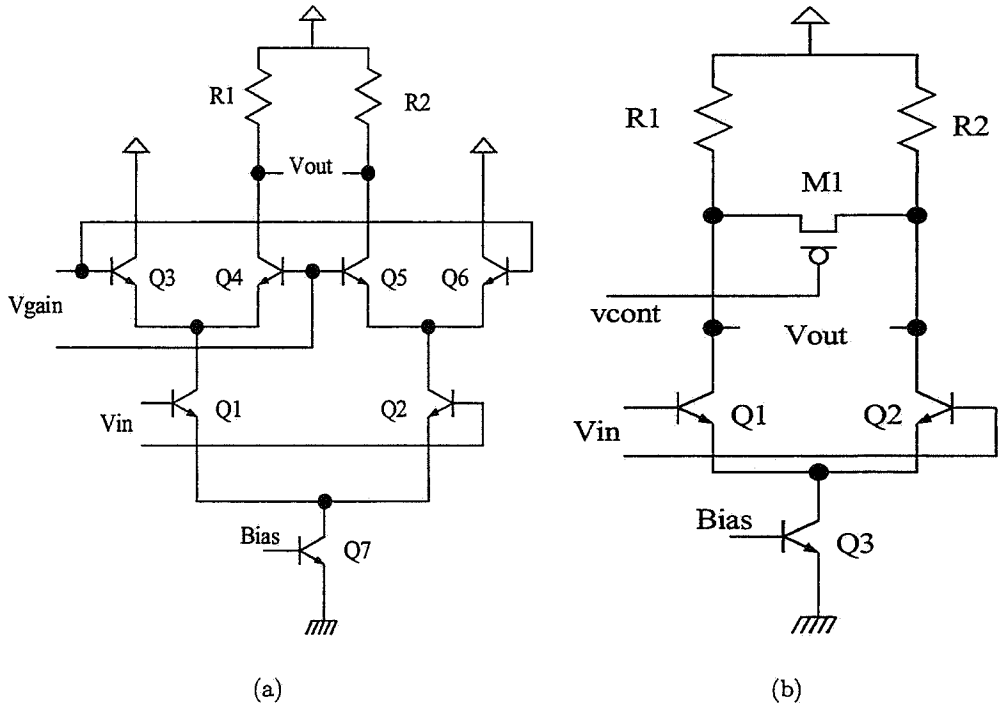


Figure 3.1 Conventional variable gain amplifiers with (a) variable conductance, and (b) variable load resistance.

Conventional VGAs (see Fig. 3.1) are of two types: variable conductance [5] (Fig. 3.1(a)) or variable load resistance [13] (Fig. 3.1(b)). Variable transconductance structure controls the gain by varying the transconductance g_m of cascode stage $Q3$-$Q6$ with V_{gain}. Small signal expression for gain A_v of this structure is given by

$$A_v = -g_{m1,2}\frac{g_{m4,5}}{g_{m4,5} + g_{m3,6}}R1,2, \tag{3.1}$$

where $g_{m4,5}$ is varied to change the gain. In the variable resistance structure, gain is tuned by varying gate voltage of M1 biased in the linear region. The small signal expression

for the gain A_v is given by

$$A_v = -g_{m1,2}(R1 \parallel \frac{R_{M1}}{2}), \tag{3.2}$$

where R_{M1} is varied to achieve gain adjustment. Both these structures have limited linearity without degeneration resistance. Incorporation of emitter degeneration to improve linearity results in a severe reduction in bandwidth because the load resistance needs to be made much larger than the degeneration resistance in order to achieve reasonable gain. The Cherry-Hooper structure [24] can be employed to reduce load resistance and hence improve the bandwidth. However, the increased transistor stack limits the voltage headroom, and thus the application of this technique is difficult in modern low-voltage processes.

3.2 Linear Variable Gain Amplifier

Five series connected identical amplifiers stages are employed as the VGA to provide a variable gain from 0 dB to 30 dB. The number of stages is determined by considering the dynamic range, bandwidth, and linearity requirements. The linearity of the entire front end is determined by that of the VGA because the signal level that the VGA handles is larger than that of the TIA. As the VGA is fully differential, it does not generate even harmonics provided that the transistors and input signals are matched in terms of the common mode, amplitude, and phase.

The basic structure of the proposed VGA is a variable g_m differential amplifier with an NMOS load (see Fig. 3.2). The gain of amplifier is tuned by controlling the bias current of the amplifier. The minimum current I_{bias} is set to 400 μA via device M5,

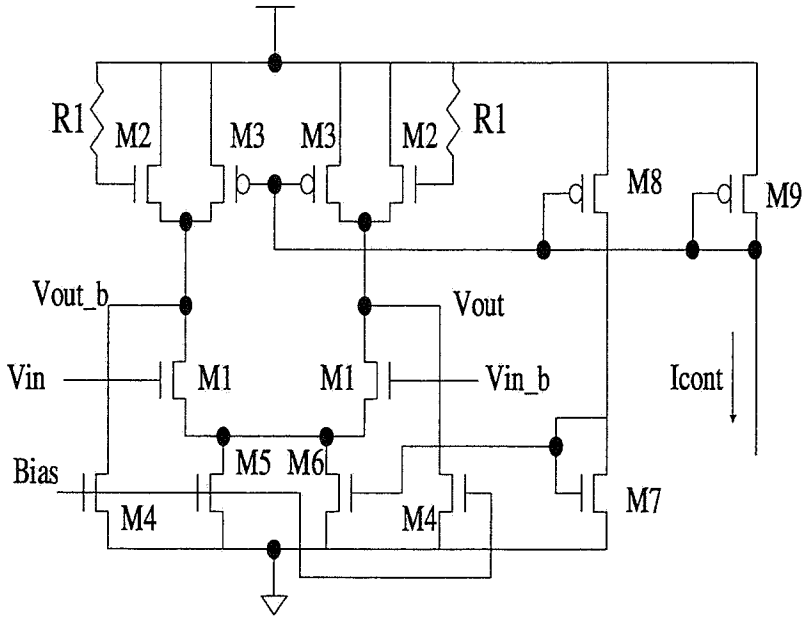


Figure 3.2 Single stage of the proposed variable gain amplifier.

which provides a 0-dB gain. Transistors M3 and M6 provide a variable current through M1 as a function of the control current I_{cont}. The size of transistors M8 and M9 are identical and the size of transistors M3 is half the size of transistor M8 while M6 and M7 are identical. Therefore, the current flowing through M2 does not change when I_{cont} changes. As the current flowing through M2 is fixed, the output common mode voltage is constant regardless of the current flowing through M1, and constant full scale output is maintained under all gain conditions. The gain of the VGA is given by

$$A_v = \frac{g_{m1}}{g_{m2}} = \frac{\sqrt{2k_{driver}(I_{bias} + I_{cont})}}{\sqrt{2k_{load}I_{bias}}}, \tag{3.3}$$

where k_{driver} and k_{load} are device transconductances of the driver M1 and load M2 transistors, respectively. As the two device transconductances g_{m1} and g_{m2} track each other, the absolute gain and variable gain range of the proposed VGA are independent of pro-

cess and temperature variations. The variable gain range is from 0 dB to 30 dB with the control current I_{cont} ranging from 0 mA to 1.6 mA and the control voltage V_{cont} between 1.3 V and 1.9 V.

As the nonlinearity of the driver M1 is compensated by that of M2, sufficient linearity can be achieved without using degeneration resistors as long as M1 operates in saturation region. The resistance R1 increases the bandwidth of the amplifier by adding a zero to the signal path. Transistor M2 with gate resistance R1 is also referred to as an active inductor [18].

Transistors M4 are used to create another design variable to satisfy linearity, bandwidth, common mode voltage, and gain simultaneously.

3.3 Linearity Requirement

Linearity of differential amplifiers is measured in terms of third harmonic distortion, which is defined as the ratio of the fundamental frequency at f_0 to the third harmonic at $3f_0$. The third harmonic distortion generated by the VGA is the dominant factor contributing to the overall spurious free dynamic range (SFDR). For a cascade of n identical amplifiers, the third harmonic distortion $HD_{3,n}$ is given by [25]

$$HD_{3,n} = HD_{3,single}\frac{G^{2(n-1)} - 1}{G^2 - 1}, \tag{3.4}$$

where $HD_{3,single}$ is the third harmonic distortion and G is the gain of each amplifier, respectively. The worst case SFDR occurs with $G \approx 1$, in other words, when the input

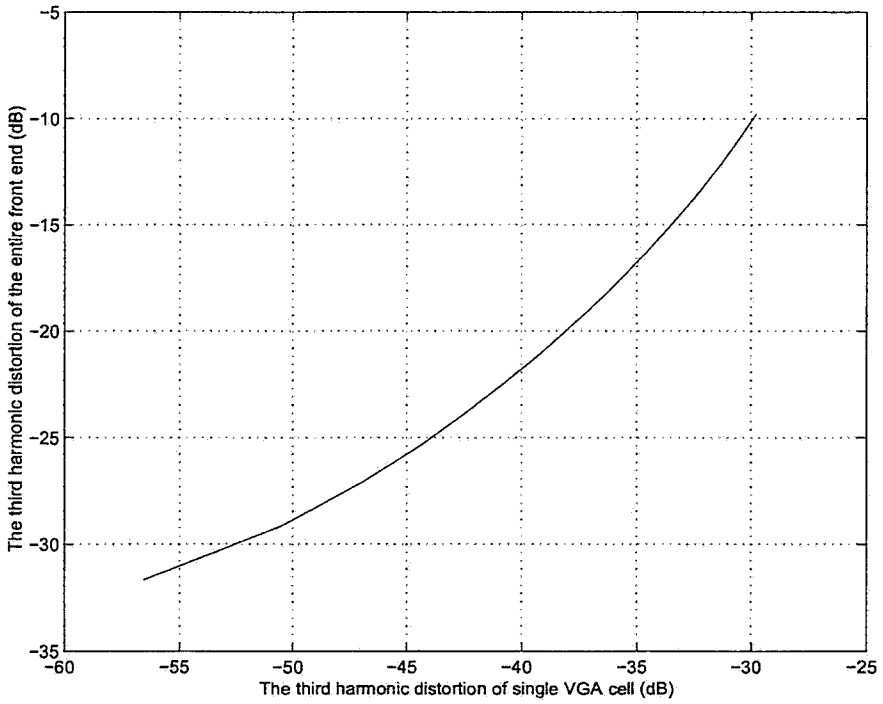


Figure 3.3 Relationship between the linearity of a single VGA cell and the entire front-end including TIA and VGA.

signal amplitude is close to full scale amplitude. In such cases,

$$HD_{3,n} \approx nHD_{3,single}. \tag{3.5}$$

Equation (3.5) determines the linearity requirements for each stage. Figure 3.3 shows the relationship between the linearity of the single VGA cell and the entire front-end obtained by plotting (3.5) with TIA nonlinearity included.

The sources of nonlinearity in the VGA are channel-length modulation and body effect. The linearity of the VGA is inversely proportional to gain and output DC bias point, which is controlled by the current flowing through M2 and the device size ratio of M1 and M2. Similarly, the size of transistor M2 trades off with bandwidth and gain.

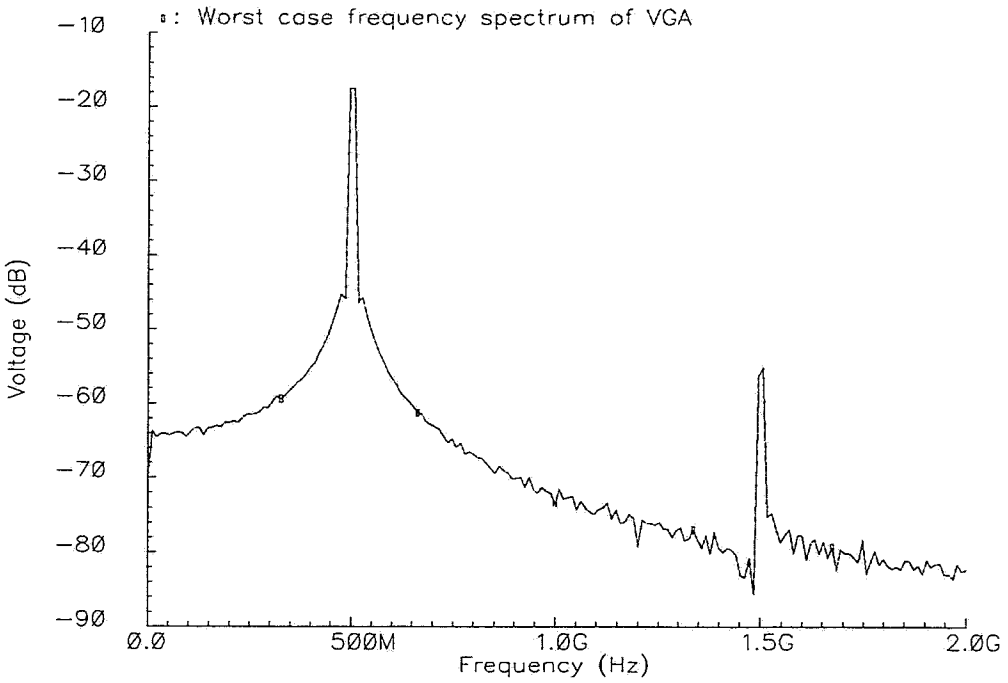


Figure 3.4 The worst case frequency spectrum of VGA with a 500-MHz input signal.

Therefore, transistors M4 are used to create another design variable. As a result, the linearity of VGA is improved while maintaining sufficient bandwidth, gain, and common mode voltage. Simulation results reveal that the worst case total harmonic distortion of the VGA is improved by more than 25 % by incorporating M4. With the worst case third harmonic distortion of the TIA being -39 dB, the third harmonic distortion of a single VGA cell needs to be about -37 dB in order to keep the third harmonic distortion of the entire front-end to be under -18 dB.

Figure 3.4 shows the results of the simulation of a single VGA cell with a 500-MHz signal tone at the input. The simulation results show that the worst case third harmonic distortion is -37.5 dB.

3.4 Offset Cancellation

The sources of front-end offset are the photo detector dark current, single-ended to fully-differential conversion, and the TIA and VGA offsets. However, it is important to maintain identical common mode levels for the two differential output signals in order not to lose effective number of bits (ENOB) in the receiver ADC. The offset control utilizes fully differential circuits in order to minimize the noise injection into the sensitive front stages. Figure 3.5 shows the fully differential offset cancellation amplifier (OCA) placed between the TIA and VGA (see Fig. 2.1). The output common mode voltage of the offset cancellation amplifier is insensitive to output common mode voltage of offset error amplifier (see Fig. 3.6) because the injected current from M3 is subtracted by M5. As

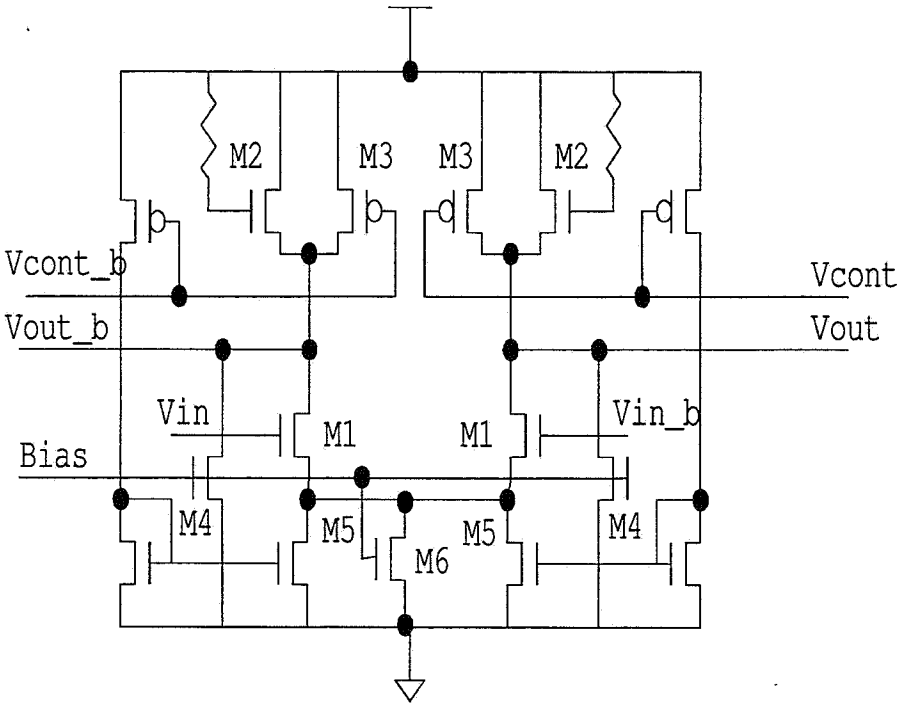


Figure 3.5 Offset cancellation amplifier schematic.

a result, offset cancellation block provides the same common mode voltage as VGA and hence maintains voltage headroom.

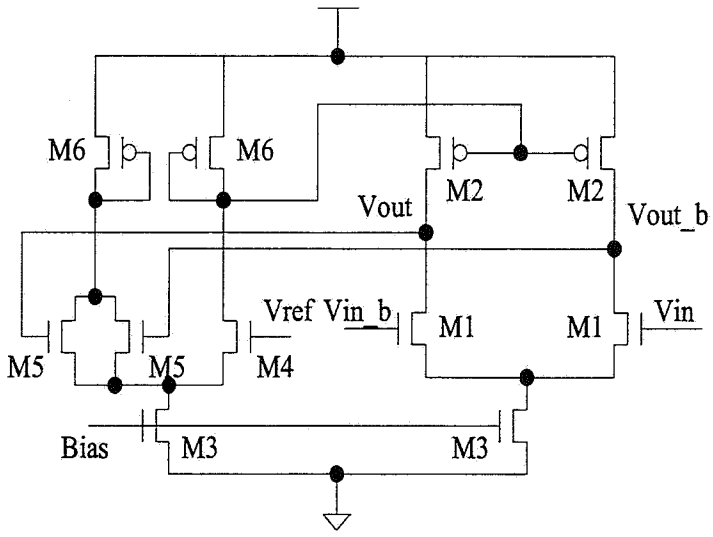


Figure 3.6 Offset error amplifier schematic.

The output offset voltage of the entire front-end becomes

$$V_{o,off} = \frac{A_v V_{off,1} + A_v A_e V_{off,2}}{1 + A_v A_e}, \tag{3.6}$$

where A_v is the VGA gain, A_e is the gain of error amplifier, $V_{off,1}$ is the sum of the input referred offset voltage of VGA and the output offset voltage of TIA, and $V_{off,2}$ is the input referred offset voltage of the offset error amplifier. In case the DC feedback is directly connected between the output of VGA and the input of TIA, the performance of TIA can be degraded due to the injected noise from the VGA output. In (3.6), passive DC feedback is not effective in cancelling the offsets because $V_{off,1}$ appears directly at the output.

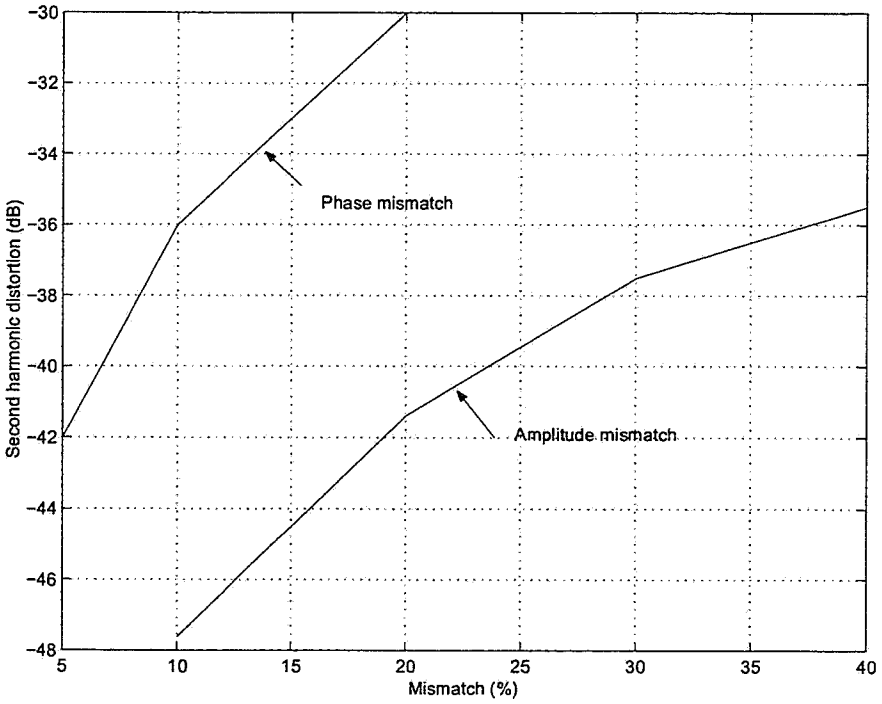


Figure 3.7 Second harmonic generation due to mismatches.

The outputs of the error amplifier are connected via external pins to large capacitors in order to reduce the lower -3-dB frequency, which is given by $\frac{(A_v A_c+1)}{2\pi r_o C_{ext}}$, where r_o is the output impedance of the error amplifier and C_{ext} is external capacitance. The output signal nonlinearity of OCA caused by the TIA output signal mismatch must be taken care of as the offset cancellation amplifier is placed between the TIA and VGA. The second harmonic generated by the mismatch appears at the output of VGA with a unity factor because the VGA does not contribute to the second harmonic distortion. The TIA output signal is not a perfectly matched differential signal and has common mode, amplitude, and phase delay mismatches. The common mode mismatch does not affect the output linearity very much once the offset is adjusted via DC feedback. The amplitude and phase delay mismatches have significant effect on the linearity. Figure 3.7 shows the second

harmonic distortions caused by these mismatches, and it is clear that the phase mismatch has a major effect. This is the reason for incorporating a source follower at one of the TIA outputs. The source follower is sized such that the phase delay is matched to within 1 % from DC to 1-GHz frequency range and the output swing mismatch is about 20 %. The nonlinearity caused by signal mismatch is apparent only at the interface between the TIA and VGA because the mismatch becomes negligible at the output of the OCA.

3.5 Simulation and Measured Results

In this section, we first present the simulation results of the entire variable-gain transimpedance front-end in 2.5-V 0.25-μm, 1-poly, 5-metal digital CMOS process. In addition, we have implemented the variable gain transimpedance front-end in a test chip. The test chip was wafer tested using a probe station. The transimpedance gain is measured using a network analyzer and linearity is measured using spectrum analyzer. Test results from this chip are also presented and compared with existing designs.

3.5.1 Simulation results

At the minimum gain, the harmonics generated by the TIA and the VGA are the dominant limiting factor in determining the $SNDR$ because input signal amplitude is large. Usually, the third harmonic distortion HD_3 increases in proportional to the square of input signal amplitude. However, the noise becomes the limiting factor at high gain. Figure 3.8 shows the $SNDR$, SNR, and $SFDR$ of the entire transimpedance front-end. The simulated result dictates that a minimum $SNDR$ of $18 - 19\,\mathrm{dB}$ is achieved at the gain extremes.

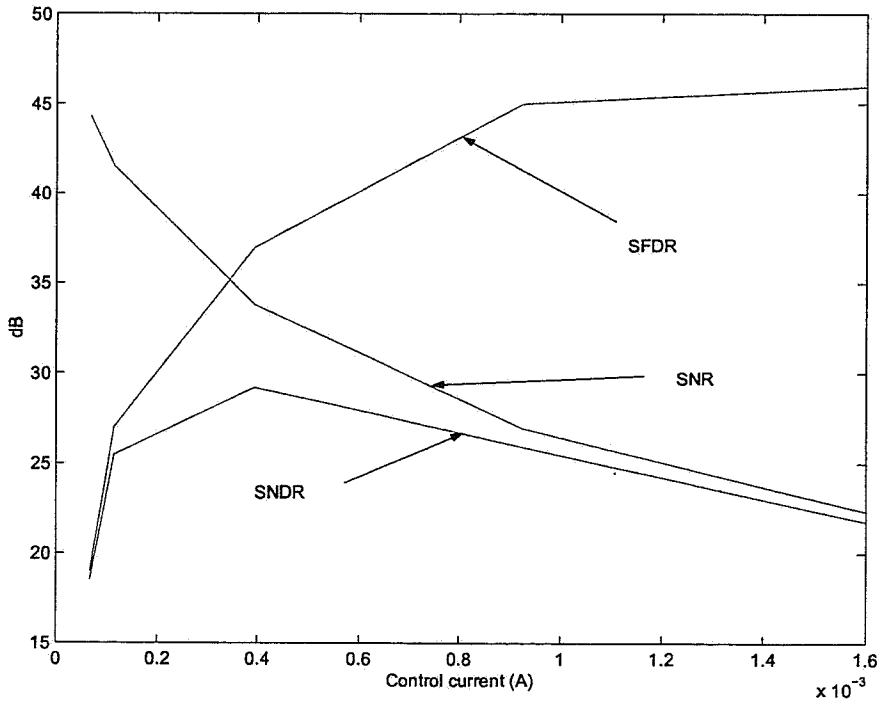


Figure 3.8 Simulated SNR, SFDR, and SNDR of the transimpedance front-end.

Figure 3.9 shows the temperature dependence of VGA gain. The gain variation is about 1.5 dB and 0.6 dB at high-end and low-end, respectively.

3.5.2 Measured results

Figure 3.10 shows the measured transimpedance of the complete front-end. The overall transimpedance can be tuned from 57 dBΩ to 87 dBΩ with a control voltage ranging from 1.3 V to 2.1 V, which is directly applied to control current input. The measured bandwidth of the overall system is 1.4 ± 0.1 GHz (with an input capacitance of 0.4 pF) implying that a data rate of 2 Gb/s can be achieved. The high-frequency glitches are caused by low SNR at those frequencies.

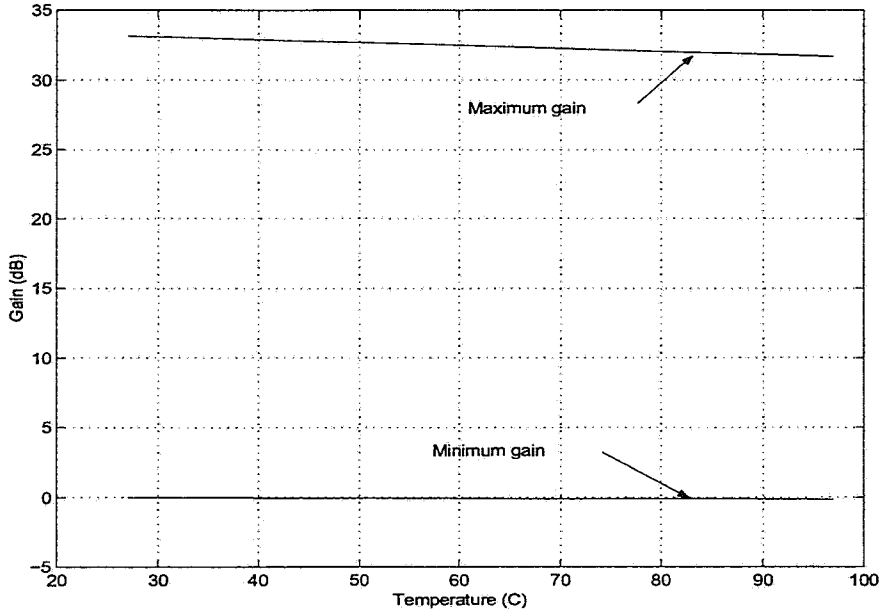


Figure 3.9 Simulated temperature dependence of VGA gain.

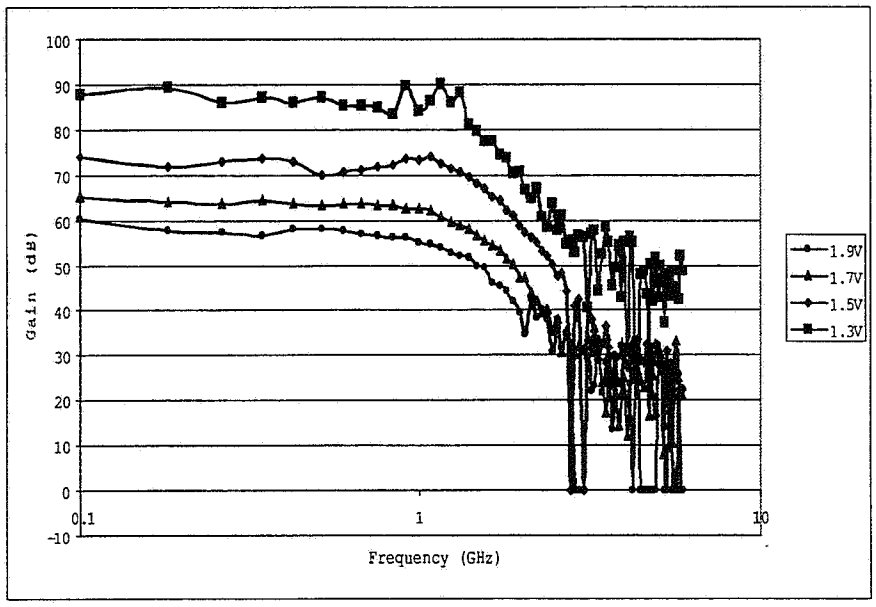


Figure 3.10 Measured transimpedance of the complete front-end.

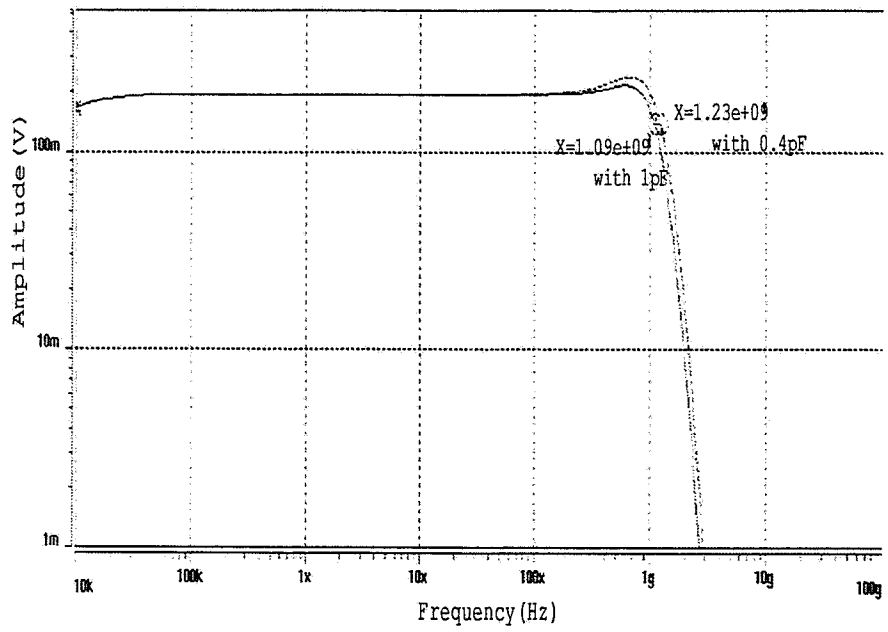


Figure 3.11 Simulated transimpedance of the complete front-end with a 0.4-pF and 1-pF input capacitor.

Nominal parasitic capacitances of the photo detector are 1 pF and 0.25 pF for OC-48 and OC-192 applications, respectively. Simulation results in Fig. 3.11 with a 0.4-pF and a 1-pF input capacitance indicate that the bandwidth degrades from 1.23 GHz to 1.1 GHz when the gain is 87 dB. It implies that effective pole-zero cancellation makes the bandwidth insensitive to the dominant pole location. Figure 3.12 shows the measured phase response of the system for the minimum and maximum gain conditions. The slope in phase response is the group delay and any fluctuation in group delay results in data-dependent jitter. It can be seen that the phase response is linear from 0.1 GHz to 1.9 GHz.

The spectrum analyzer measurements in Fig. 3.13 show a worst case SFDR of 19 dB when the gain of the VGA is set to minimum and the input power is set to maximum, just meeting the 18-dB requirements. Test equipment constraints forced the design of a single-

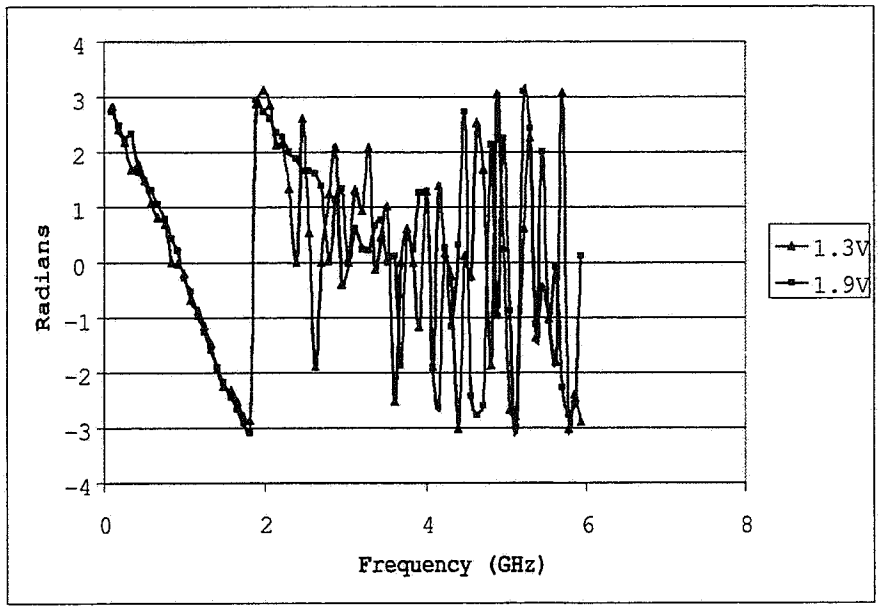


Figure 3.12 Measured phase response of complete front-end with 87-dB and 57-dB transimpedance gain.

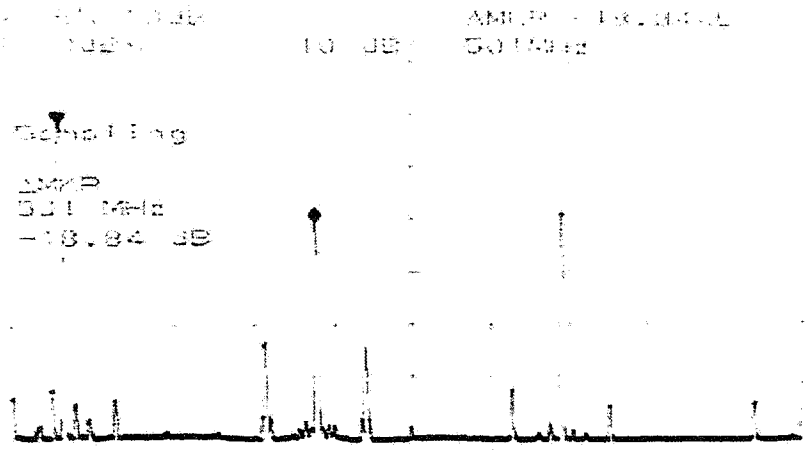


Figure 3.13 Measured frequency spectrum of the complete front-end with a 500-MHz input signal.

ended 50-Ω output driver, which is the dominant contributor to the second harmonic. The major source of the second harmonic component is the 50-Ω driver, which can be eliminated in a fully integrated system. The spurs around the harmonics are due to the intermodulation caused by a high-powered FM radio station near the laboratory.

Figure 3.14 shows the microphotograph of the test chip fabricated in standard 2.5-V, 0.25-μm, 1-poly, 5-metal digital CMOS process. The total area of the chip is $0.8 \times 0.9\,\text{mm}^2$ and the active area is $0.066\,\text{mm}^2$. The chip consumes 150 mW from a single 2.5-V supply, of which simulations show that the 50-Ω driver consumes 70 mW.

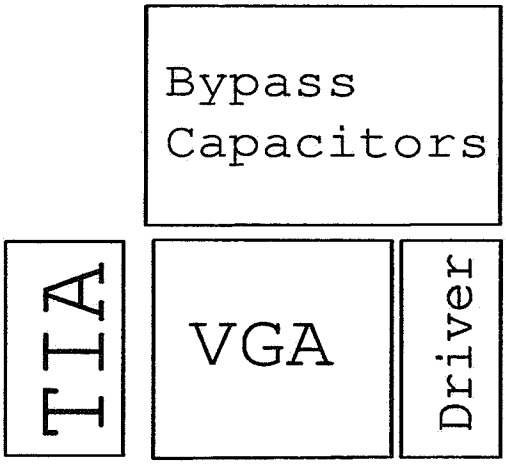


Figure 3.14 Microphotograph of test chip.

The proposed design and recently published designs are compared in Table 3.1. Existing designs have lower input referred current noise than proposed design because non-

linear designs can be implemented with fewer transistors. The proposed VGA is linear and achieves process-independent variable gain with wide bandwidth.

Table 3.1 Comparison with existing front-ends.

	This work	J. Lee [14]	A. Tanabe [13]	W-Z. Chen [26]
Process	0.25 μm CMOS	0.25 μm CMOS	0.15 μm CMOS	0.35 μm CMOS
Gain	57 dB-87 dB	Fixed 68 dB	Fixed > 69.9 dB	Fixed 97 dB
Bandwidth	1.4 GHz	0.65 GHz	1.9 GHz	< 2.3 GHz
Power dissipation	80 mW	23 mW	104 mW	100 mW
SFDR	19 dB	N/A	N/A	N/A
Noise	0.7 μA	0.28 μA	0.35 μA	0.5 μA

The measured performance of the optical front end system is summarized in Table 3.2.

Table 3.2 Test chip summary.

Process	0.25 μm, 1-poly 5-metal CMOS
Transimpedance gain	57 dB-87 dB
Bandwidth	1.4 ± 0.1 GHz
Power dissipation	150 mW (70 mW is from 50 Ω driver)
Chip area	0.72 mm^2
Active area	0.066 mm^2
Power supply	2.5 V
SFDR	19 dB (dominated by 50 Ω driver)
Group delay	0.56 ns
Full scale output	0.5 V peak-to-peak
Maximum input current	1.25 mA peak-to-peak

3.6 Summary

A linear process-insensitive CMOS variable gain amplifier design technique was proposed. Prototype implementation of the TIA-VGA circuit demonstrates a tunable tran-

simpedance in the range 57 dBΩ to 87 dBΩ, a −3-dB bandwidth of 1.4 ± 0.1 GHz, $SFDR$ > 19 dB while maintaining an output swing of $500\,\mathrm{mV_{pp}}$ in standard 2.5-V, 0.25-μm CMOS process.

CHAPTER 4

A SiGe BiCMOS VARIABLE GAIN AMPLIFIER (VGA)

This chapter describes the design and measured performance of a linear VGA for EDC-based OC-192 (10 Gb/s) optical receivers. The proposed VGA has been implemented in a 3.3-V, $f_T = 75\,\text{GHz}$, 0.25-μm SiGe BiCMOS process. The target application is OC-192 long-haul (LH) and ultra long-haul (ULH) fiber links. In this application, a variable gain range of $> 40\,\text{dB}$, SNDR of $> 18\,\text{dB}$, and a 3-dB bandwidth of $> 4\,\text{GHz}$ is required. The proposed VGA has been implemented in a 3.3-V, 0.25-μm SiGe BiCMOS process.

4.1 The VGA Architecture

The proposed VGA (see Fig. 4.1) consists of the a gain block, an analog multiplexer (MUX), a gain control block, an offset cancellation block, a replica bias generator and output drivers.

The gain block consists of three identical cascaded differential amplifiers A_0, A_1, and A_2. Each amplifier stage provides a gain range of $5 - 15\,\text{dB}$. The output of each stage is connected to an analog MUX. The gain of the VGA is controlled by a current injected into the gain control block and the analog MUX control input. The replica bias generator

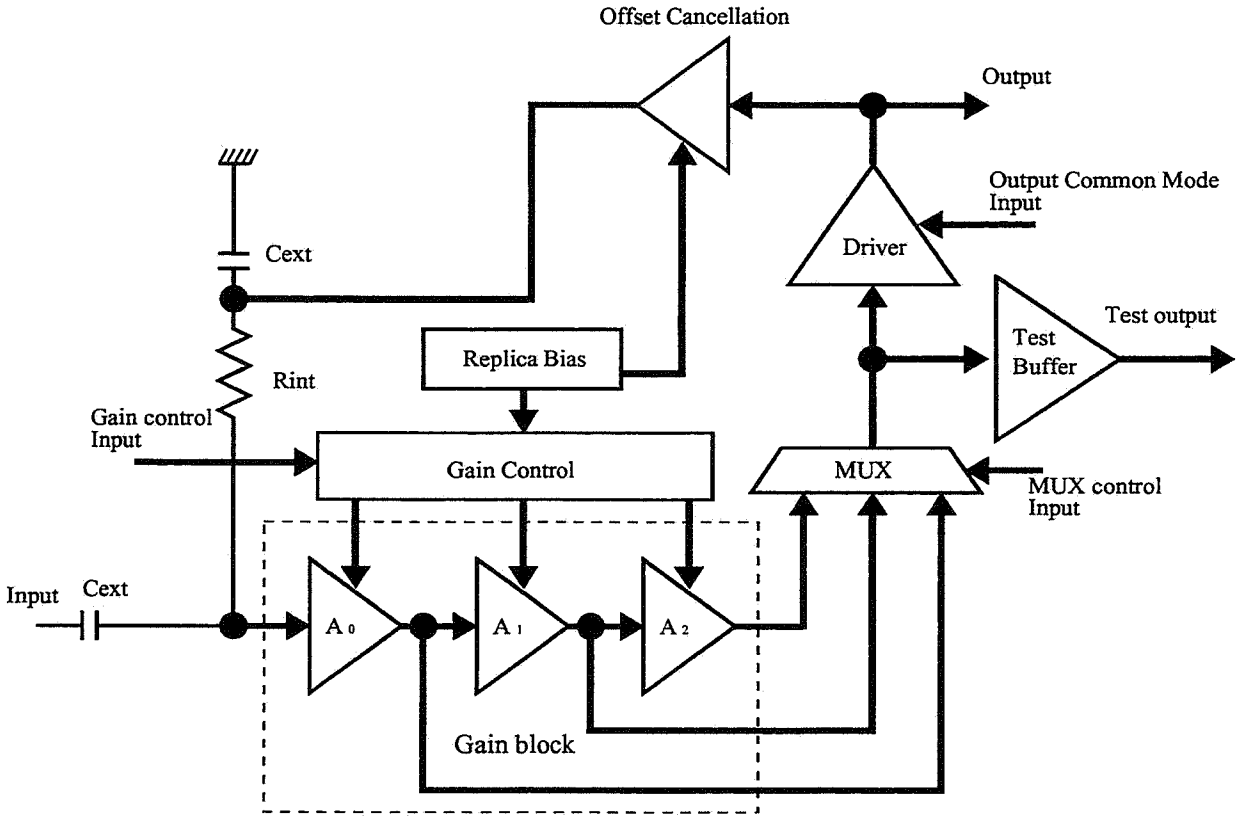


Figure 4.1 Block diagram of the proposed SiGe VGA.

generates a replica of the DC bias points of the gain block and provides them to the gain control block and offset cancellation block in order to achieve process insensitivity. The analog MUX feeds into an output driver that includes a common mode feedback (CMFB) loop to track the common mode voltage information provided by the next stage. The outputs of the driver provide offset information to the offset cancellation block, which then removes the output DC offset voltage. Another important functionality of the offset cancellation block is to provide proper input bias voltage to the first gain stage such that the gain of overall VGA is insensitive to process variations.

4.2 The Gain Block

The gain block consists of three identical differential amplifiers each having tunable emitter degeneration. The emitter degeneration resistor is made tunable by employing an NMOS transistor in parallel with a fixed resistor as shown in Figure 4.2. The gain is controlled by tuning the gate voltage of the NMOS transistor M_1 biased in the linear region.

One benefit of the proposed architecture is that the linearity of the gain stage is consistent with the input amplitude; i.e., when the input signal is large, the VGA gain is reduced and linearity increased by increasing the degeneration resistance.

4.2.1 Linearity analysis

For a differential amplifier without degeneration, the input-output relation is given by [19]

$$V_{od} = \alpha_F I_{TAIL} R_C tanh(-\frac{V_{id}}{2V_T}), \tag{4.1}$$

where $\alpha_F = \frac{\beta_F}{1+\beta_F}$, I_{TAIL} is the tail current source, and R_C is the load resistance. For input swing $|v_{id}| << 2V_T$, we can expand (4.1) using power series given by

$$V_{od} = \alpha_F I_{TAIL} R_C(-\frac{V_{id}}{2V_T} + \frac{V_{id}^3}{24V_T^3} + \cdots). \tag{4.2}$$

Emitter resistance in transistor amplifier results in local feedback. The loop gain T is given by

$$T = g_{m,Q_1}\frac{R_{total}}{2}, \tag{4.3}$$

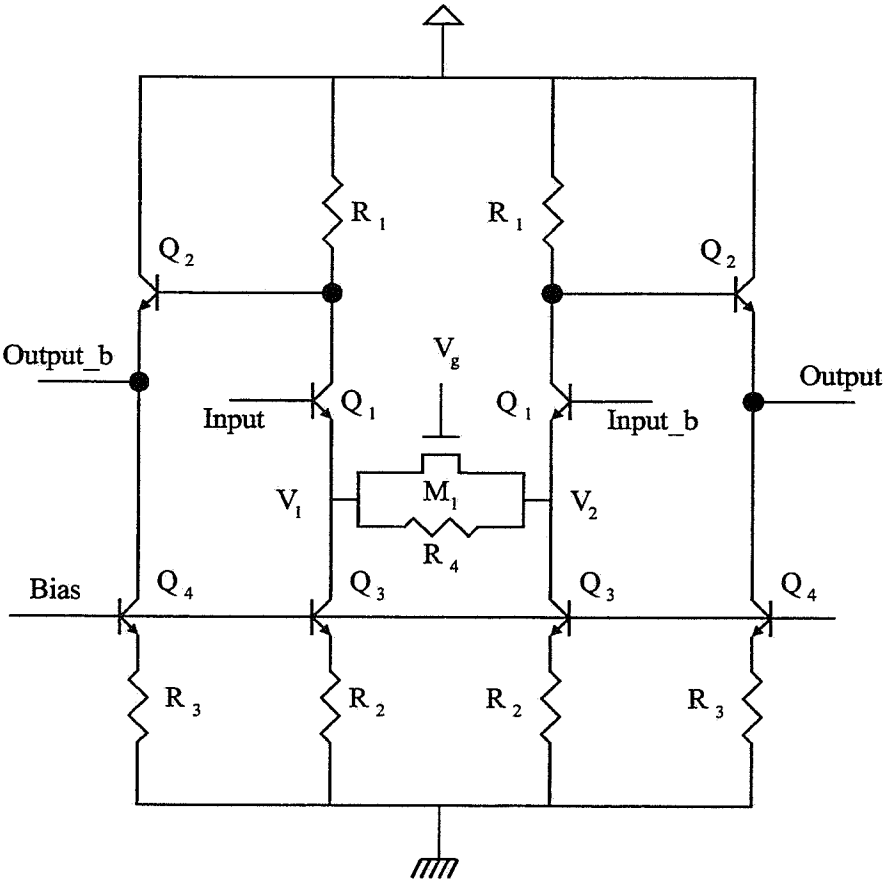


Figure 4.2 The circuit schematic of a gain stage.

where g_{m,Q_1} is the transconductance of transistor Q_1, and R_{total} is the resistance of the parallel combination of M_1 and R_4. In general, the third harmonic distortion $HD_{3,fb}$ in differential structure with local feedback is given by [27]

$$HD_{3,fb} = \frac{HD_3}{(1+T)^3}. \tag{4.4}$$

where HD_3 is the third harmonic distortion of a differential amplifier without degeneration and is given by [19]

$$HD_3 \approx \frac{V_{id}^2}{48V_T^2}, \tag{4.5}$$

where V_{id} is input amplitude and V_T is thermal voltage.

From (4.3)-(4.5), the third harmonic distortion of the gain stage is given by

$$HD_{3,fb} = \frac{V_{id}^2}{48V_T^2(1 + g_{m,Q_1}\frac{R_{total}}{2})^3}. \tag{4.6}$$

By noting that $\frac{V_{id}}{R_{total}} \approx \frac{V_o}{2R_1}$ and that V_o and R_1 are constant, it is clear that the VGA maintains linearity for all input levels according to (4.6).

4.2.2 Frequency response

The dominant pole p of a single gain stage is located at

$$p = \frac{1}{R_1(C_{\pi,Q_2} + C_{cs,Q_1})}, \tag{4.7}$$

where C_{π,Q_2} is the base-emitter capacitance of Q_2 and C_{cs,Q_1} is the collector-substrate capacitance of Q_1. One zero z is created by the capacitance in the degeneration path and is located at

$$z = \frac{2}{R_{total}(\frac{1}{2}C_{ox}LW + C_{cs,Q_3})}, \tag{4.8}$$

where L and W are the length and width of M_1, and C_{cs,Q_3} is the collector-substrate capacitance of Q_3. In order to prevent emitter peaking, we want to set the zero at or

above the dominant pole frequency. Thus, from (4.7) and (4.8) we get

$$\frac{2R_1}{R_{total}} \geq \frac{\frac{1}{2}C_{ox}LW + C_{cs,Q_3}}{C_{\pi,Q_2} + C_{cs,Q_1}}. \tag{4.9}$$

By noting that $C_{cs,Q_1} \approx C_{cs,Q_3}$ and $\frac{1}{2}C_{ox}LW \geq C_{\pi,Q_2}$, we conclude that $2R_1$ should be greater than R_{total}. Considering the fact that the minimum gain of an emitter degenerated differential amplifier is approximately $\frac{2R_1}{R_4}$, it is clear that it is hard to achieve low gain as well as a flat frequency response. Each gain stage provides a variable gain range of 10 dB, while maintaining 5 dB of minimum gain in order to prevent emitter peaking.

4.2.3 Emitter follower design

The emitter follower Q_2, Q_4 drives the differential amplifier in the next amplifier stage in the VGA, which causes frequency and amplitude dependent nonlinearity if the emitter follower is not biased properly. Figure 4.3 shows a simplified single-ended circuit diagram where an emitter follower is driving an inverting amplifier (representing the next stage) which has parasitic feed-forward capacitors. The parasitic feed-forward capacitance C is contributed by base-collector capacitance C_μ. The bias current I_{bias}, emitter current I_e, and output current I_{out} satisfy

$$I_{bias} = I_e - I_{out}, \tag{4.10}$$

$$I_{out} = C\frac{d(V_o - V_o')}{dt}, \tag{4.11}$$

$$V_o' = -AV_o, \tag{4.12}$$

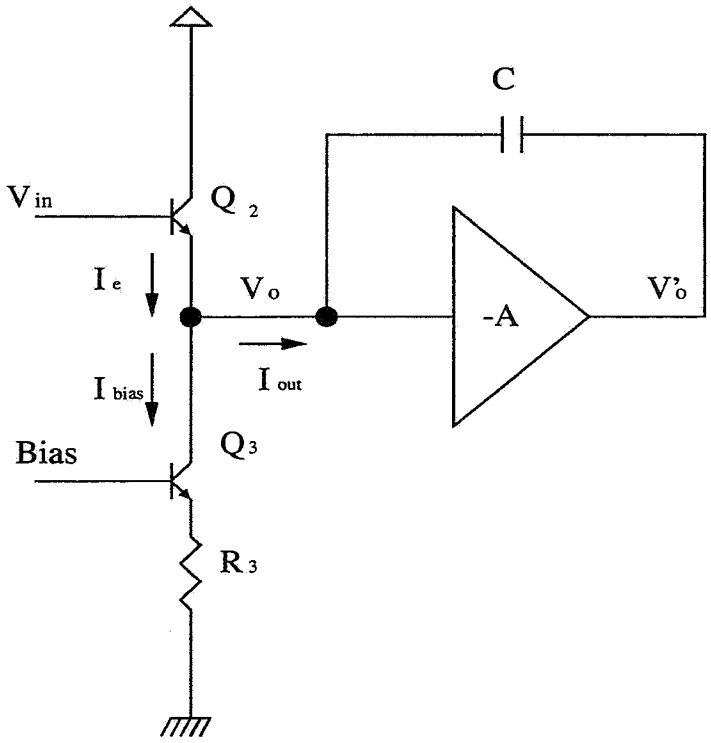


Figure 4.3 Simplified circuit schematic where an emitter follower is driving an inverting amplifier.

where V_o and V_o' are the output voltages of emitter follower and the inverting amplifier, respectively, and $-A$ is the gain of the inverting amplifier. By noting that $V_o = V_{in} - V_{be,Q_2}$ in proper operating condition, where V_{in} is the input voltage, we get

$$I_{bias} = I_e + C(A+1)\frac{\partial}{\partial t}V_{be,Q_2} - C(A+1)\frac{\partial}{\partial t}V_{in}. \tag{4.13}$$

For proper operation, I_e should be greater than zero. If V_{in} is sinusoid, i.e., $V_{in} = \alpha \sin \omega t$ and $\frac{\partial}{\partial t}V_{be,Q_2} \approx 0$, we get

$$I_{bias} > -C(A+1)\alpha\omega \cos \omega t. \tag{4.14}$$

The maximum current flows into emitter follower from the inverting amplifier if $\cos \omega t = -1$. The condition $V_o = V_{in} - V_{be,Q_2}$ is valid when

$$I_{bias} > C(A+1)\alpha\omega. \tag{4.15}$$

The bias current should increase with frequency and amplitude. We set I_{bias} such that minimum I_e is 10 % of I_{bias} to ensure linearity. In the proposed design, $A \times \alpha = 0.35$, $\omega = 2\pi \times 5 \times 10^9$, and $C \approx 50\,\text{fF}$.

The gain block has two significant issues that must be addressed. The first issue is the nonlinearity of the NMOS degeneration resistor. The second issue is the minimum gain achievable while maintaining a flat frequency response. The maximum value of the degeneration resistor R_{total} needs to be small enough to prevent emitter peaking. Thus, it is difficult to achieve small gain with a conventional cascaded VGA structure. The analog MUX solves both of these problems in an elegant manner as described next.

4.3 Analog Multiplexer

The analog MUX, shown in Fig. 4.4, consists of two cascaded stages. The first stage of the MUX is an isolation buffer that isolates the first and second gain stages from the second stage of the MUX. The third gain stage does not require an isolation buffer because the third gain stage acts as an isolation stage. The gain of MUX is unity except for the one connected to the third gain stage output, which has a gain of 6 dB. The second stage of the MUX sums the three inputs from the gain stages using an open collector scheme where inputs are selected by enabling the corresponding bias current.

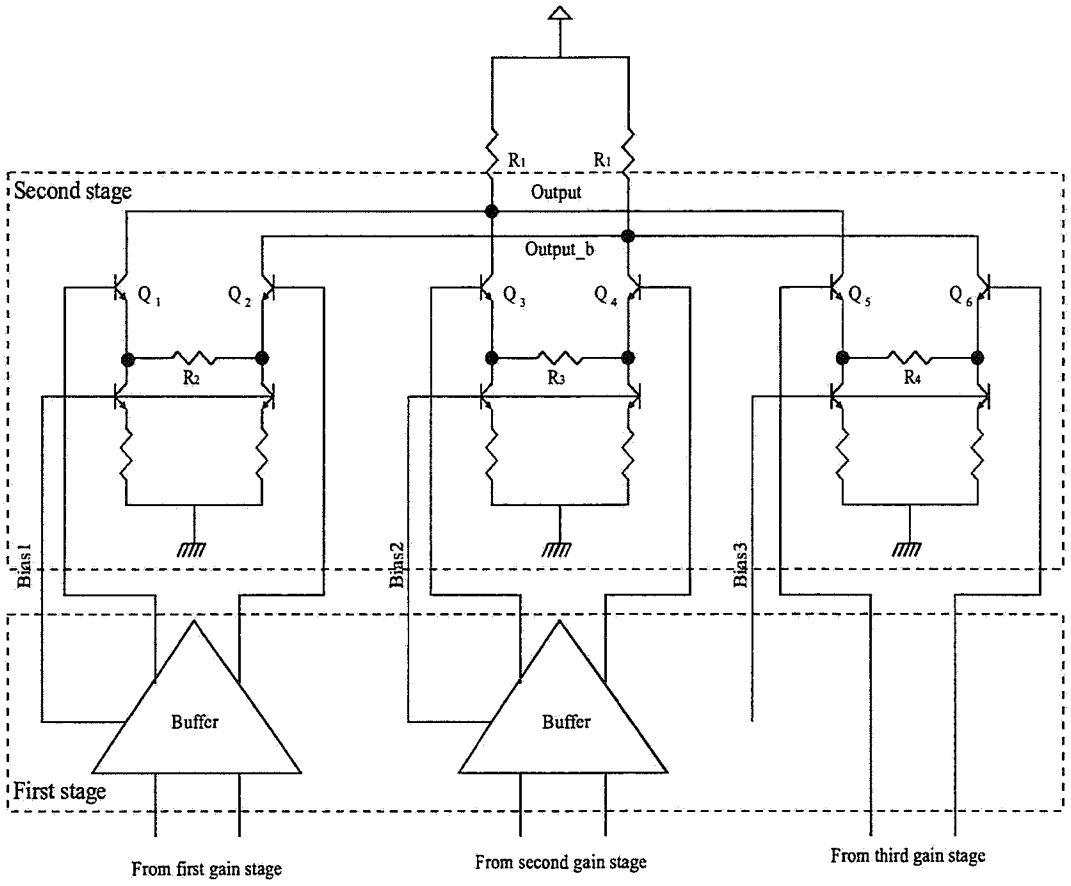


Figure 4.4 The circuit schematic of analog multiplexer.

A key advantage of the analog MUX is that it improves the VGA linearity both in the low and high gain mode. Consider the case when the input signal is large. In that case, the second and third gain stages are bypassed and only the first stage is selected by the analog MUX. Given that the linearity of the analog MUX is better than that of the gain stages because the former employs larger passive fixed degeneration resistors for unity gain, the overall VGA linearity is improved over a static three cascaded stage architecture. In case the input swing is small, the final amplification is done in MUX and the output of final gain stage is 6 dB smaller than full scale output. Simulation results

reveal that the proposed analog MUX design improves the linearity of VGA by 10 dB compared to the conventional cascaded structure.

Another advantage of the analog MUX is the improved gain range. Each gain stage provides a variable gain of $5 - 15$ dB. For the conventional three cascaded stage VGA, the total gain range will be $15 - 45$ dB. On the other hand, the proposed design provides a gain range of $5 - 51$ dB. Thus, the proposed design provides an additional 16-dB gain adjustment.

One drawback of the analog MUX is its bandwidth limitation. However, this limitation was not found to be severe when proper layout guidelines were employed. Having a process technology with an f_T of 75 GHz also helped.

4.4 Process Insensitive Gain Control

The performance of the gain block is highly dependent on the MOS process variables such as the threshold voltage V_{th} and the device transconductance K of M_1 (see Fig. 4.2). By noting that the gain of each gain stage A_v is given by

$$A_v \approx (1 + KR_4(V_{gs} - V_{th}))\frac{2R_1}{R_4}, \tag{4.16}$$

where V_{gs} is the gate-to-source voltage of M_1, it is necessary to control the gate-to-source voltage V_{gs} carefully in order to achieve process independence. Process insensitive gain controller schematic is shown in Fig. 4.5. The replica bias cell generates the DC bias point V_1 (see Fig. 4.2) for the gain control block. By incorporating a diode connected NMOS which is identical to the NMOS M_1 used in the gain stages (see Fig. 4.2), the

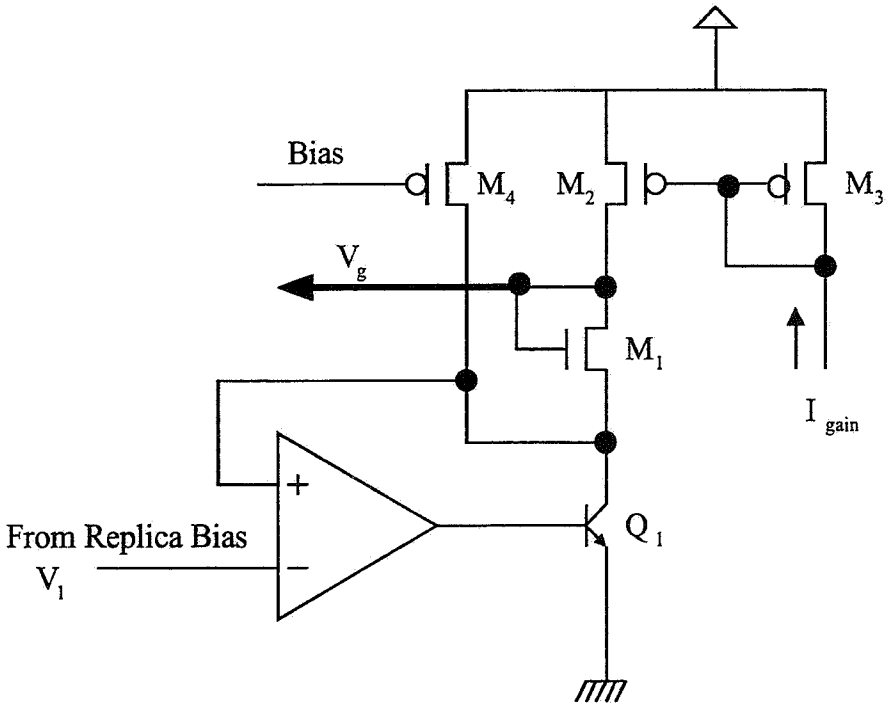


Figure 4.5 The simplified circuit schematic of threshold voltage insensitive gain controller.

gain control voltage V_g is given by

$$V_g = V_1 + V_{th} + \sqrt{\frac{2I_{gain}}{K}}, \tag{4.17}$$

where I_{gain} is external current input which determines the gain. Substituting (4.17) into (4.16), we obtain

$$A_v \approx (1 + R_4\sqrt{2KI_{gain}})\frac{2R_1}{R_4}. \tag{4.18}$$

From (4.18), it is clear that the gain is independent of the threshold voltage, and sensitivity to device transconductance K is also decreased.

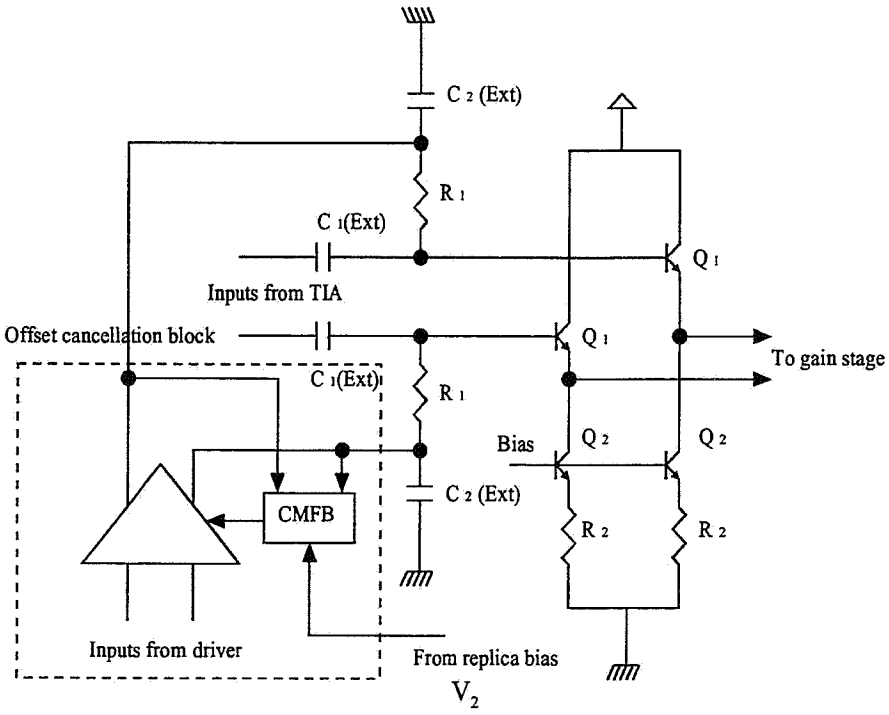


Figure 4.6 The simplified circuit schematic including offset cancellation scheme and input termination.

Transistor M_4 enhances the stability of the gain controller by reducing the output impedance variation at the source of M_1 as a function of the gain control current, which varies in the range $0.01 - 2\,\text{mA}$. Thus, appropriate pole separation is achieved while using small compensation capacitor.

4.5 Input Termination and Offset Cancellation

Figure 4.6 shows the simplified input termination scheme for the VGA. Capacitance C_1 is an AC coupling capacitor and R_1 is a 50-Ω input termination resistor. Capacitance C_2 contributes to offset feedback compensation. Both C_2 and C_1 are off-chip. Thus, by choosing $C_2 = C_1$ and using bond wires of equal lengths, the gain from the tran-

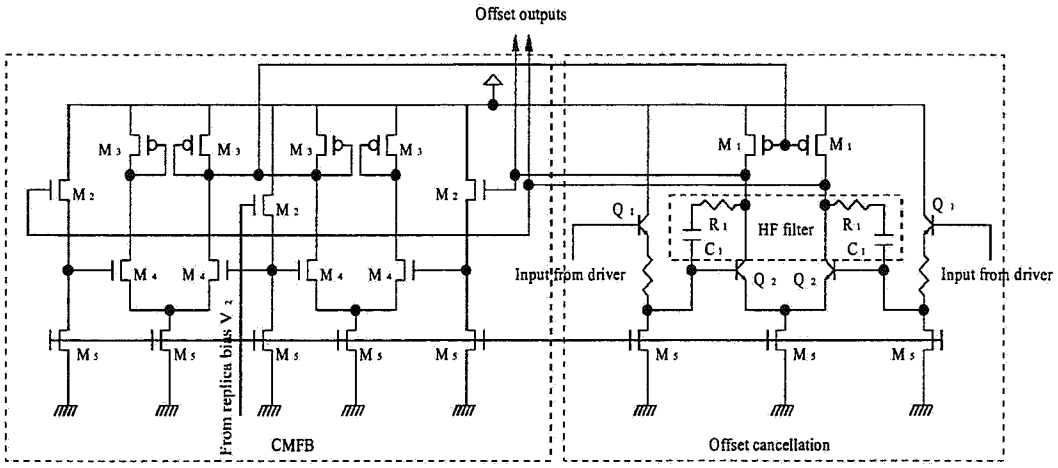


Figure 4.7 Schematic of offset cancellation and common mode feedback (CMFB).

simpedance amplifier output to the emitter follower input remains flat at $-6\,\mathrm{dB}$ over all frequencies thereby approaching the characteristics of an ideal 50-Ω termination.

The emitter follower stage isolates the input termination from the gain stage, thereby providing a constant input impedance over the entire gain range. The correct input common mode voltage ($V_{in} = V_{cc} - I_{bias}R_1 - V_{be}$ in Fig. 4.2) is generated by the replica bias and used for common mode voltage reference. As a result, the first stage also benefits from the process insensitive gain control scheme described earlier.

The offset cancellation circuitry suppresses the VGA output offsets. Offset cancellation circuitry must be simulated with the package model in order to ensure the stability of the entire VGA. Offset cancellation circuitry suppresses high-frequency loop gain caused by packaging inductance below $-90\,\mathrm{dB}$ with high-frequency poles (R_1 and C_1 in Fig. 4.7) while achieving 31 dB low-frequency gain. As a result, the overall VGA has a flat frequency response in entire gain range. Figure 4.8 shows the open loop gain of entire VGA in maximum gain condition. Additional high frequency pole added into offset

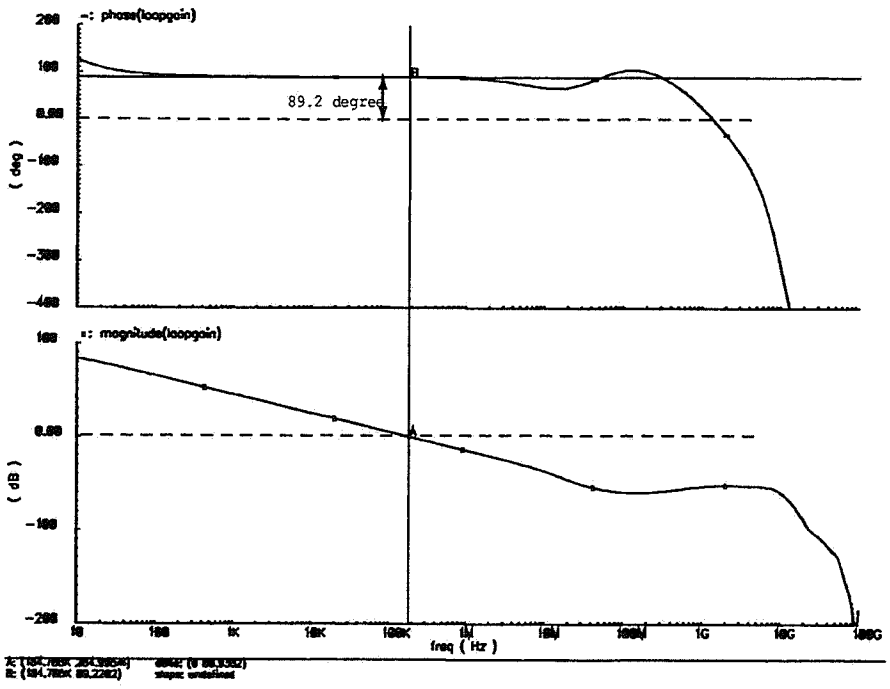


Figure 4.8 VGA loop-gain in maximum gain condition.

cancellation block suppresses the inductive peaking caused by packaging inductance and maintains worst case phase margin of 89°.

4.6 Replica Biasing

Replica bias generates bias voltages that track with process variations. The replica bias replicates two cascaded single-ended gain stages. Replica bias generates two bias voltages, one for gain control block (V_1) and the other for offset cancellation (V_2).

The transistor Q_1 in dotted line in Fig. 4.9 is used to enhance the accuracy of bias voltage generated by replica bias by replicating the base current. The ideal voltage for

V_2 is

$$V_2 = V_{cc} - IR_1(\frac{\alpha_F}{\beta_F}(\frac{2\alpha_F}{\beta_F} + 1) + 2\alpha_F), \tag{4.19}$$

where $\alpha_F = \frac{\beta_F}{1+\beta_F}$ and β_F is forward current gain. Table 4.1 compares the accuracy of bias voltage with and without Q_1.

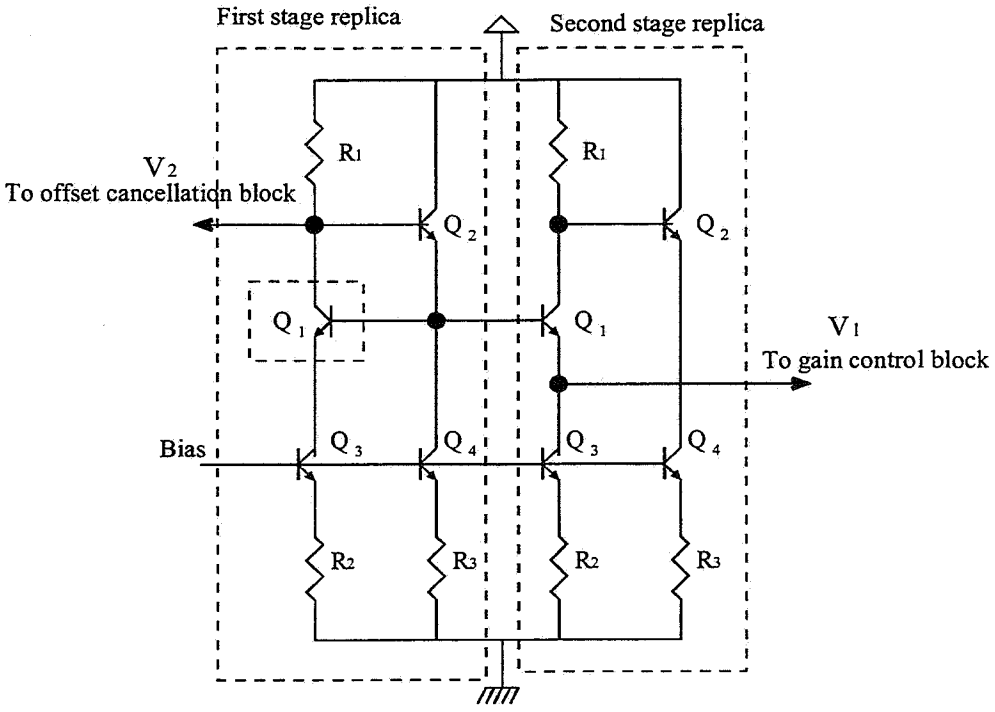


Figure 4.9 The circuit schematic of a replica bias generator.

Table 4.1 The accuracy comparison of replica bias voltage generator.

	Without Q_1	With Q_1
V_2	$V_{cc} - IR_1(\frac{\alpha_F}{\beta_F}(\frac{2\alpha_F}{\beta_F} + 1) + 2)$	$V_{cc} - IR_1(\frac{\alpha_F}{\beta_F}(\frac{4\alpha_F}{\beta_F} + 1) + 2\alpha_F)$
Error	$2IR_1\frac{1}{\beta_F+1}$	$2IR_1\frac{1}{(\beta_F+1)^2}$

4.7 Simulated Results

Figure 4.10 shows the gain of VGA with various temperature, supply, and process corners. In this simulation, three stages are cascaded and the control current is varying from 0.01 mA to 2 mA with 1-GHz input signal. The total gain variations are 1.3 dB and 2.5 dB at low and high gain modes, respectively.

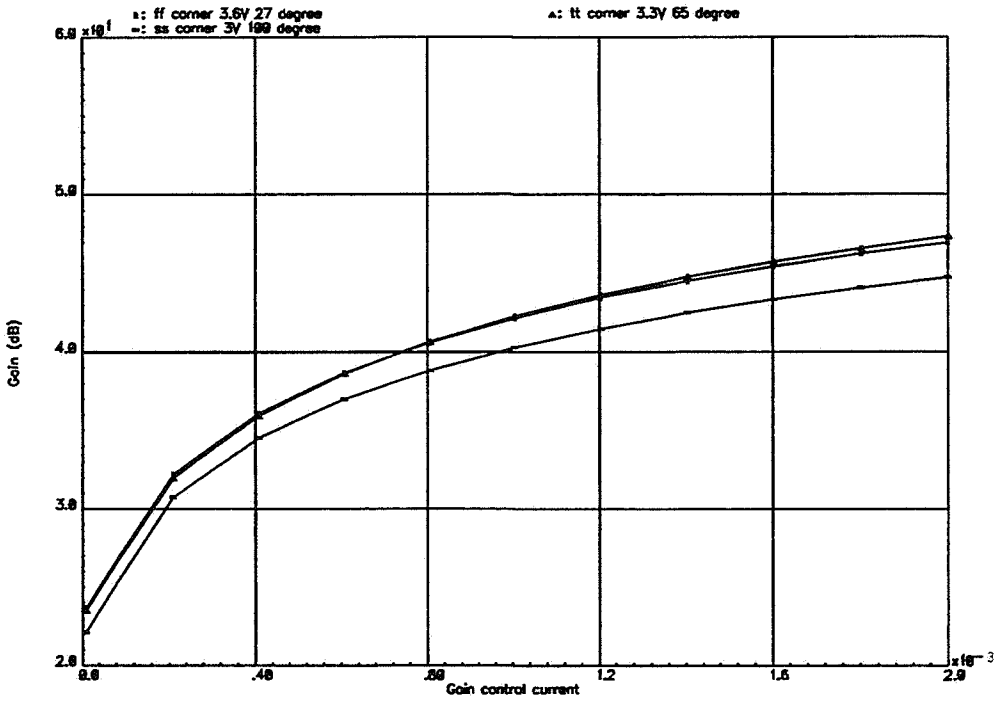


Figure 4.10 The VGA gain at various conditions.

4.8 Measured Results

Figure 4.11 shows the measured frequency response of VGA. For a given gain setting, the input power is adjusted such that the single-ended output power at the test buffer

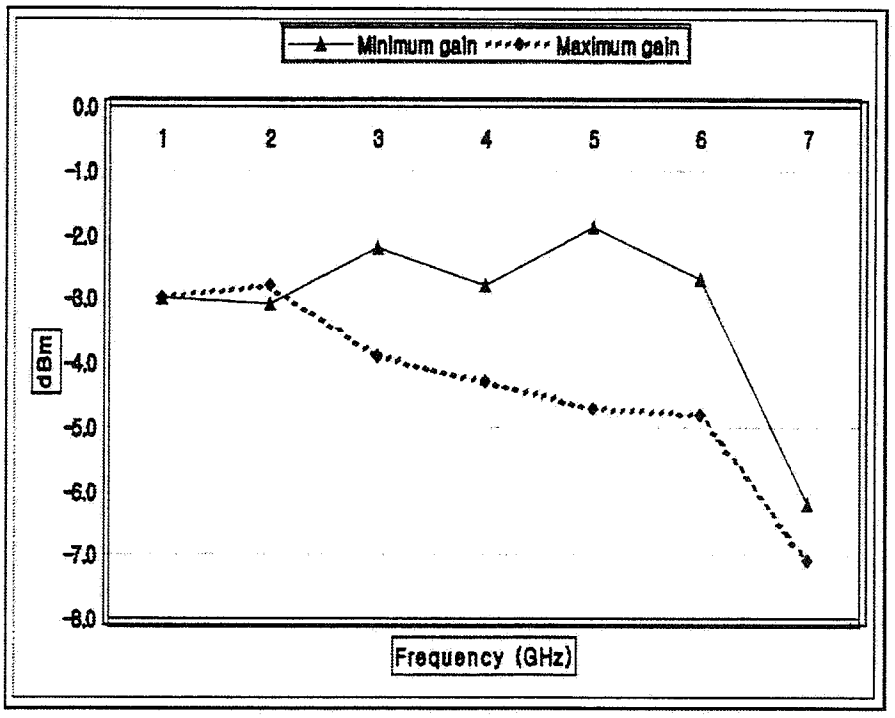


Figure 4.11 Measured frequency response of VGA at minimum and maximum gain.

output is −3 dBm. This is done because the gain of the test buffer is −4.4 dB and the nominal VGA output swing is set to 1.4-V peak-to-peak differential. The maximum measured gain of the VGA is 44.73 dB and the minimum gain is 2.43 dB. The measured 3-dB cutoff frequency is around 6.5 GHz and 7 GHz in the maximum and minimum gain conditions, respectively.

Figures 4.12 and 4.13 show the frequency spectra of the entire VGA in the minimum and maximum gain mode, respectively. The single-ended output signal power is set at −3 dBm with 700-MHz sinusoidal input signal in both cases. A sufficiently low-frequency (700 MHz) input signal is chosen to prevent the attenuation of harmonics. The measured spurious free dynamic range ($SFDR$) is 32.38 dB in minimum gain mode and 26.46 dB in maximum gain mode. The $SFDR$ is lower for maximum gain because all three gain

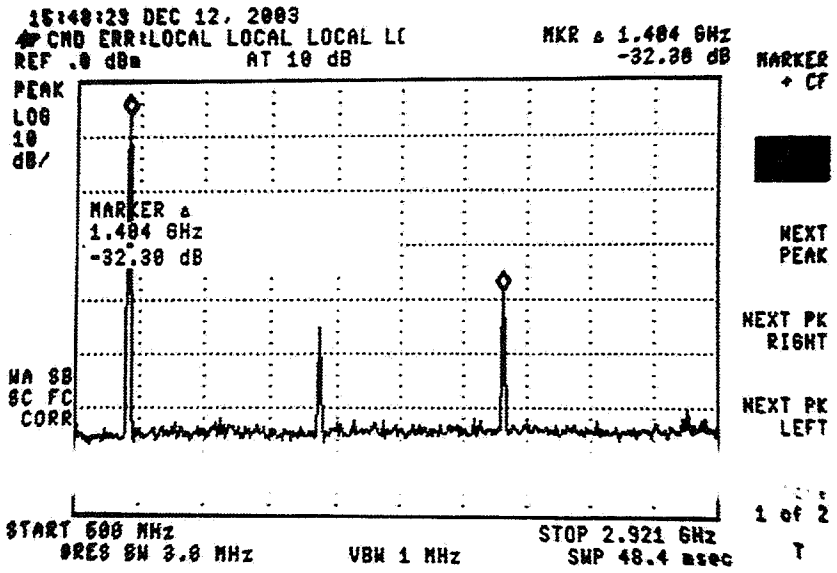


Figure 4.12 Frequency spectrum of the VGA at minimum gain with 700-MHz tone.

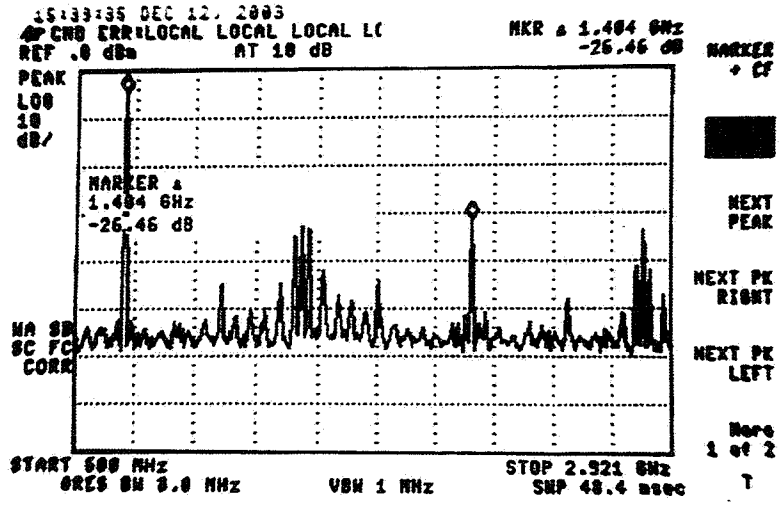


Figure 4.13 Frequency spectrum of the VGA at maximum gain with 700-MHz tone.

blocks are cascaded. The even order harmonic is caused by the single-ended measurement. The peaks around second harmonic shown in Fig. 4.13 are caused by substrate coupling from other blocks on the chip.

Simulations have shown that the worst case total integrated output noise is $43.9\,\mathrm{mV_{rms}}$ and the SNR is 21.3 dB.

Figure 4.14 shows the microphotograph of the VGA.

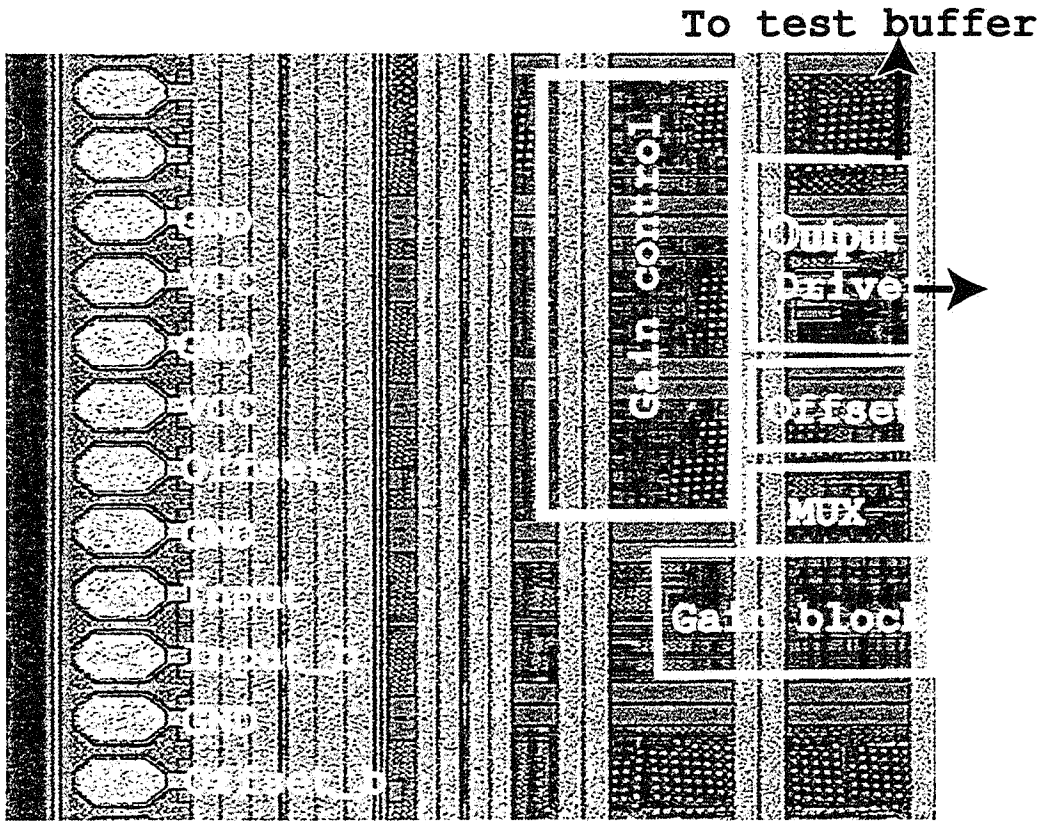


Figure 4.14 The microphotograph of VGA.

The measured performance of VGA is summarized in Table 4.2, where the power number includes the measured power consumption of all the blocks in the VGA shown in Fig. 4.1 minus the simulated power consumption of the output buffer.

Table 4.2 Measured results.

Process	0.25 μm, SiGe BiCMOS
Gain range	2.43 dB $\sim$ 44.73 dB (total 42.3 dB)
Bandwidth	6.5 GHz maximum gain 7 GHz minimum gain
Output common mode voltage	power supply - 0.45 V
Output offset voltage	$< 15\,mV$
Power dissipation	$102\,mW$
Area	0.66 mm^2
packaging	169 pins, 13mm $\times$ 13mm FBGA
Power supply	3.3 ± 0.3 V
$SFDR$	26.46 dB maximum gain 32.38 dB minimum gain
Full scale output	1.4 V_{pp} differential fixed (ADC) 0.84 V_{pp} differential fixed (test buffer)

Table 4.3 Comparison with existing designs.

	This work	[MM94] [5]	[HK00] [4]
Process	75 GHz f_T SiGe BiCMOS	22 GHz f_T Si-Bipolar	30 GHz f_T SiGe Modular BiCMOS
Gain	2.43 dB-44.73 dB	-10 dB-37 dB	Fixed 30 dB
Bandwidth	> 6.5 GHz	10 GHz	12 GHz
Power dissipation	$102\,mW$	$850\,mW$	$115\,mW$
Power supply	3.3 ± 0.3 V	-6.5 V	3.6 V
SFDR	> 26.46 dB	N/A	N/A

Comparison with existing optical front-ends is shown in Table 4.3. Existing designs have wider bandwidth but require higher supply voltages and are nonlinear. The proposed VGA is linear, and achieves process-independent variable gain with a bandwidth that is sufficient for EDC-based OC-192 applications.

4.9 Summary

The SiGe BiCMOS variable gain amplifier achieves wide dynamic range and linearity with low supply voltage of 3.3 V by incorporating variable degeneration and analog mul-

tiplexer. The SiGe BiCMOS VGA provides process-independent 42-dB dynamic range while achieving worst case SFDR of 26 dB with 1.4-V peak-to-peak output swing. Also, it achieves a minimum 3-dB bandwidth of 6.5 GHz, consumes 102 mW of power in 0.25-μm SiGe BiCMOS process.

CHAPTER 5

CONTRIBUTIONS AND FUTURE WORK

In this dissertation, we demonstrated front-end circuits suitable for EDC based fiber-optic communication systems.

5.1 Contributions

The proposed work contributed the following:

(1) A wide-band CMOS TIA design technique referred to as transconductance peaking improves gain-bandwidth product without impacting noise and headroom.

(2) A linear process-insensitive CMOS variable gain amplifier design technique was proposed. The CMOS VGA achieves 30-dB dynamic range, and sufficient linearity and bandwidth without impacting headroom.

(3) Prototype implementation of the TIA-VGA circuit demonstrates a tunable transimpedance in the range 57 dBΩ to 87 dBΩ, a −3-dB bandwidth of 1.4 ± 0.1 GHz, SFDR > 19 dB while maintaining an output swing of 500 mV_{pp} in standard 2.5-V, 0.25-μm CMOS process.

(4) SiGe BiCMOS variable gain amplifier achieves wide dynamic range and linearity with low supply voltage of 3.3 V by incorporating variable degeneration and analog multiplexor.

(5) Prototype implementation of SiGe BiCMOS VGA suitable for EDC at 10 Gb/s was presented. The SiGe BiCMOS VGA provides process-independent 42-dB dynamic range while achieving worst case SFDR of 26 dB with 1.4-V peak-to-peak output swing. Also, it achieves a minimum 3-dB bandwidth of 6.5 GHz, and consumes 102 mW of power in 0.25-μm SiGe BiCMOS process.

5.2 Future Work

Large scale integration in the gigahertz frequency range results in considerable substrate coupling even in highly resistive substrates. In this case, random noise including thermal and shot noise, and substrate coupling with respect to voltage swing at individual building block must be taken into account carefully for desired operation. The following design challenges need to be addressed:

(1) The substrate coupling mechanism resulting in frequency domain mixing must be understood and reflected in the design procedure. Investigation of optimum swing in low swing digital circuits considering noise and substrate coupling will provide a lower bound on power consumption.

(2) Digital signal processing techniques can be employed to control critical analog parameters such as the bias current as well as bandwidth for error correction.

REFERENCES

[1] K. Azadet, E. Haratsch, H. Kim, F. Saibi, J. Saunders, M. Shaffer, L. Song, and M.-L. Yu, "DSP techniques for optical transceivers," in *IEEE Conference on Custom Integrated Circuits*, 2001, pp. 281–288.

[2] H. Bulow and G. Theilecke, "Electronic PMD mitigation - from linear equalization to maximum-likelihood detection," in *Proc. Optical Fiber Communication Conference and Exposition*, 2001, p. WAA3.

[3] H. F. Haunstein and K. Sticht, "Design of near optimum electrical equalizers for optical tranmission in the presence of PMD," in *Proc. Optical Fiber Communication Conference and Exposition*, 2001, p. WAA4.

[4] H. Kim and J. Bauman, "A 12 GHz, 30 dB modular BiCMOS limiting amplifier for CMOS limiting amplifier for 10 Gb SONET receiver," in *ISSCC Digest of Technical Papers*, 2000, pp. 160–161.

[5] M. Moller, H. M. Rein, and H. Wernz, "13 Gb/s Si-bipolar AGC amplifier IC with high gain and wide dynamic range for optical-fiber receivers," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 815–822, July 1994.

[6] M. Sieben, J. Conradi, and D. E. Dodds, "Optical single sideband transmission at 10 Gb/s using only electrical despersion compensation," *IEEE Journal of Light Wave Technology*, vol. 17, pp. 1742–1749, Oct. 1999.

[7] T. Vanisri and C. Toumazou, "Integrated high-frequency low-noise current-mode optical tranimpedance amplifiers: Theory and practice," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 677–685, June 1995.

[8] J. Martinez-Castillo and J. Silva-Martinez, "Transimpedance amplifiers for optical fiber systems based on common-base transistors," in *Proc. International Symposium on Circuits and Systems*, 1999, pp. 85–88.

[9] H. H. Kim, S. Chandrasekhar, C. A. Burrus, and J. Bauman, "A Si BiCMOS transimpedance amplifier for 10 Gb/s SONET receiver," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 769–776, May 2001.

[10] H. Ikeda, T. Ohshima, M. Tsunotani, T. Ichioka, and T. Kimura, "An auto-gain control transimpedance amplifier with low noise input dynamic range for 10 Gb/s optical communication system," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1303–1308, June 2001.

[11] R. G. Meyer and R. Blauschild, "A wide-band low-noise monolithic transimpedance amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-21, pp. 530–533, Aug. 1986.

[12] C. Kuo, C. Hsiao, S. Yang, and Y. Chan, "2 Gbit/s transimpedance amplifier fabricated by 0.35 μm CMOS technologies," *Electronic Letters*, vol. 37, pp. 1158–1160, Sept. 2001.

[13] A. Tanabe, M. Soda, Y. Nakahara, T. Tamura, K. Yoshida, and A. Furukawa, "A single-chip 2.4 Gb/s CMOS optical receiver IC with low substrate cross-talk preamplifier," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 2148–2153, Dec. 1998.

[14] J. Lee, S. Song, S. Park, C. Nam, Y. Kwon, and H. Yoo, "A multichip on oxide of 1 Gb/s 80 dB fully-differential CMOS transimpedence amplifier for optical interconnect applications," in *ISSCC Digest of Technical Papers*, 2002, pp. 80–81.

[15] M. Neuhauser, H.-M. Rein, and H. Wirnz, "Low-noise high-gain si-bipolar preamplifiers for 10 Gb/s optical-fiber links-design and realization," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 24–29, Jan. 1996.

[16] J. Mullrich, H. Thurner, E. Mullner, J. F. Jensen, W. E. Stanchina, M. Kardos, and H.-M. Rein, "High-gain transimpedance amplifier in InP-based HBT technology for the receiver in 40 Gb/s optical-fiber TDM links," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1260–1265, Sept. 2000.

[17] A. Schild, H.-M. Rein, J. Mullich, L. Altenhain, J. Blank, and K. Schrodinger, "High-gain SiGe transimpedance amplifier array for a 12 $\times$ 10 Gb/s parallel optical-fiber link," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 4–12, Jan. 2003.

[18] E. Sackinger and W. C. Fischer, "A 3 GHz, 32 dB CMOS limiting amplifier for SONET OC-48 receivers," in *ISSCC Digest of Technical Papers*, 2000, pp. 158–159.

[19] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Robert, *Analysis and Design of Analog Integrated Circuits*, 4^{th} ed., New York: John Wiley & Sons Inc., 2001.

[20] M. Nakamura, N. Ishihara, Y. Akazawa, , and H. Kimura, "An instantaneous response CMOS optical receiver IC with wide dynamic range and extremely high sensitivity using feed-forward auto-bias adjustment," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 991–997, Sept. 2001.

[21] R. Reimann and H. M. Rein, "Bipolar high gain limiting amplifier IC for optical fiber receivers operating up to 4 Gbits/s," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 504–510, Aug. 1987.

[22] T. Ruotsalainen, P. Palojarvi, and J. Kostamovaara, "A current-mode gain-control scheme with constant bandwidth and propagation delay for a transimpedance preamplifier," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 253–258, Feb. 1999.

[23] R. Reimann and H. M. Rein, "A single-chip bipolar AGC amplifier with large dynamic range for optical-fiber receivers operating up to 3 Gbit/s," *IEEE Journal of Solid-State Circuits*, vol. 324, pp. 1744–1748, Dec. 1999.

[24] E. M. Cherry and D. E. Hooper, "The design of wide band tranistor feedback amplifier," in *Proc. Inst. Elec. Eng*, 1963, pp. 375–389.

[25] B. Razavi, *RF Microelectronics*. Upper Saddle River: Prentice Hall, 1998.

[26] W.-Z. Chen and C.-H. Lu, "A 2.5 Gbps CMOS optical receiver analog front-end," in *IEEE Conference on Custom Integrated Circuits*, 2002, pp. 359–362.

[27] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits and Systems*, vol. 46, pp. 315–325, Mar. 1999.

VITA

Hyeon-min Bae obtained the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1998 and the M.S. degree in electrical and computer engineering from University of Illinois at Urbana-Champaign, Urbana, IL, in 2001. His research interest is in the area of analog circuits design for fiber-optic communications, switch-mode power supplies, and audio amplifiers. He is currently employed at Intersymbol Communications in Champaign, Illinois since 2001.