NEAR-FIELD WIRELESS POWER TRANSFER TO AND COMMUNICATION WITH CHIP-SCALE DEVICES

BY

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THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2017

Urbana, Illinois

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Abstract

This thesis addresses the design challenges of achieving simultaneous near-field wireless power transfer to and communication with chip-scale devices that have a form factor on the order of 100s of microns and a thickness of 10s of microns. One application that requires this technology is the supply chain security for electronic components, in which a wireless chip-scale device is embedded within the package of a host electronic component in order to verify the provenance of the host as it passes through the supply chain. The need for wireless capabilities in such an application arises from the small form factor of the chip-scale device and its lack of space for a battery, while the authentication process for security assurance requires wireless data communication with the chip-scale device. Simultaneously achieving both capabilities involves the co-design of both the power and data transceivers with an optimized near-field coupling scheme.

The organization of the thesis is as follows. Chapter 2 covers electromagnetic coupling theory to achieve wireless power transfer. A tri-coil design approach is introduced to improve the wireless power transfer efficiency of the link compared to traditional two-coil designs. The design is verified using simulated and measured results. Additionally, a certain kind of circuit is required to enable a chip-scale device to support simultaneous power and communication. Chapter 3 presents a rectifier topology that achieves this purpose, and a prototype circuit is fabricated and measured to validate the design concepts. Finally, in order for a chip-scale device to be commercially viable, it needs to be compatible with standard CMOS fabrication processes. Chapter 4 discusses design strategies and procedures for multiple CMOS-compatible circuits for chip-scale simultaneous wireless power transfer and communication applications.

Acknowledgments

First and foremost, I would like to thank my adviser Professor Songbin Gong for giving me the opportunity to work in his lab and learn under his tutelage. Throughout my graduate studies, he has demonstrated extraordinary generosity with his students, both in terms of the time he invests in us and the resources he provides for our experiments. This thesis could not have been completed without his full support. I am personally grateful for his wisdom and advice that have shaped my education, research, and career as an engineer.

Second, I would like to express my deepest appreciation for all the graduate students in our research group: Ruochen Lu, Ali Kourani, Jack Krol, Yansong Yang, Michael Breen, Anming Gao, Sarah Shim, Liuqing Gao, and Arunita Kar. They have helped and supported me countless times in my research and classes. I would also like to give special thanks to the post-docs and scholars that I have interacted with during my studies at UIUC: Dr. Yong-Ha Song, Dr. Tomas Manzaneque-Garcia, Dr. Cheng Tu, and Dr. Daotong Li. I could not have asked for a friendlier group of individuals to work with.

Third, I want to thank all the professors who have had a tremendous impact on my academic development at UIUC: Professor Steven Franke, Professor Pavan Hanumolu, Professor Jose Schutt-Aine, Dr. Su Yan, and Professor Jennifer Bernhard. I am especially grateful to Professor Franke who has always warmly received my frequent visits to his office hours and allowed me to become a TA for one of my favorite ECE courses.

Fourth, I would like to thank my friends who have made Illinois feel like a home away from home: Sakshi Srivastava, Ashwarya Rajwardan, Shweta Patwa, and the many enthusiastic individuals of Illini-Life Christian Fellowship.

A special thank-you, for teaching me to love electromagnetics, goes to Professor Jeffrey Young, without whom I would not have reached graduate school.

Last but not least, I must give my most sincere thanks to my family, whose love and support help me find meaning in everything I do.

Table of Contents

Chapter 1: Introduction

For the majority of modern electrical apparatuses, power delivery is facilitated by transmission lines, cables, or wires. Although the idea of wirelessly delivering power seems attractive, this will always result in a poorer efficiency compared to a wired power transmission system [1]. Nevertheless, the practical advantages of a wireless power link have inspired several existing and emerging commercial applications.

The earliest work in wireless power transfer was pioneered by Nikola Tesla at the start of the 20th century [2]. Tesla's visionary use of resonant inductive coupling to facilitate wireless power transfer resulted in impressive demonstrations for his time, but his idea was not adopted for commercial applications until nearly a century later. However, the use of electromagnetic waves for wireless communication underwent rapid development in the decades that followed. The first practical wireless communication links were developed by Guglielmo Marconi, who demonstrated the first transatlantic wireless communications via Morse code in 1901 [3]. After the development of the vacuum tube triode in 1906, long-distance wireless voice transmissions were made possible and the first commercial radio stations began to broadcast in 1920 [3]. While the development of radio communications has a vast and rich history, systems that supported simultaneous wireless power transfer and communication were not introduced until the development of radio frequency identification (RFID). This work investigates near-field wireless power transfer to and communication with chip-scale devices.

1.1 Motivation

In the past few years, there has been an increase of interest in a variety of applications that use wireless power transfer, and as such, the technology has improved substantially. There are several advantages to using wireless power technology for certain applications. Biomedical implanted devices have batteries that need to be recharged somehow. Since it is unsuitable to use a wire to power the implanted device, the battery ought to be charged wirelessly [4]. Wireless sensor networks are another application that benefits from wireless power technology. Rather than replacing the batteries for each sensor node in the system, the devices can harvest ambient RF energy to recharge their batteries [5]. While widespread integration of this technology in existing

wireless platforms is still underway, we are already witnessing its impact in the form of massive deployment of RFIDs.

RFID

RFID is now a ubiquitous part of the commercial electronics market. Since this work has much relevance to RFID concepts, some terminology will be introduced that will be used throughout the rest of this thesis. The RFID system consists of a reader and a tag. The reader (also known as an interrogator) is a transceiver that is usually large and stationary, whereas the tag is a chip containing a unique identifier for the object it is attached to. The reader is used to identify the various tags within its vicinity. The communication link between the tag and the reader can be one of two types — near-field or far-field — based on the required operating distance (i.e. the distance between the reader and the tag) for the intended application.

A near-field link is one in which the physical dimensions of the tag are much smaller than a wavelength at the carrier frequency. Commercial RFID systems that use near-field links typically operate in the LF band (30 to 300 kHz) or the HF band (3 to 30 MHz) [6]. The tag and the reader are electromagnetically coupled. The tag is able to transmit information (e.g. the identifying code) to the reader by modulating its impedance, which induces a change in the reader antenna impedance. The stronger the coupling between the reader and tag antennas, the more the change induced in the reader antenna. This change in impedance is sensed by the reader transceiver, and it is able to uniquely identify a given tag. One advantage of using near-field links is that the propagation delay between the tag and the reader is small compared to the period of the carrier, making the communication between them effectively instantaneous [6]. One disadvantage of using this type of system is that the operating distance is limited because the nature of the link requires the reader and tag antennas to be within each other's near-field. Moreover, in the near-field, power densities decay at a rate of $1/r^3$ compared to a rate of decay of $1/r^2$ when the antennas are operating in the far-field, where r is the operating distance. This further limits the operating range of a near-field system, especially if the reader can only transmit a fixed output power.

In a far-field link, the tag size is comparable to a wavelength at the operating frequency. The tags in these systems typically operate in the UHF band (300 MHz to 3 GHz). At these frequencies, a tag antenna that is a few centimeters in length can have a high radiation efficiency and operates in

the far-field. The reader and tag in this system use electromagnetic radiation, rather than coupling, to facilitate communication. For the majority of far-field links, the tag relies on the power transmitted by the reader for a physical support to transmit information to the reader. The tag reflects a portion of this power back to the reader and communicates by modulating its load impedance, which modulates the reflected power that is delivered to the reader. This process of communication is known as backscattering. Since this modulation is unique for each tag, it makes identification of individual tags possible. Far-field links can offer an order-of-magnitude larger operating distance compared to that of near-field links, but they suffer from more complex propagation environments and sensitivity to nearby objects.

RFID tags themselves can be categorized into the following three groups:

- Passive tags: These tags have no battery, which makes them small and cheap. These tags rely on backscattering for transmitting information to the reader. They power their onboard electronics by rectifying the incoming RF waveform from the reader. Since they need the power from the interrogation signal, they are much more limited in terms of operating distances.

- Semi-passive tags: These are essentially battery-assisted passive tags. They use backscattering to communicate to the reader, but they have batteries to power their on-board electronics. Semi-passive tags have much larger operating distances than passive tags because they do not need to extract power from the incoming signal. The operating distance is limited by the communication link, i.e. by the distance at which a backscattered signal can no longer be reliably demodulated by the reader transceiver.

- Active tags: These tags comprise a complete, working radio system, with an antenna, battery, transceiver, and control circuits. These tags are generally bulky and expensive, but they can provide operating ranges of hundreds of meters. They do not use backscattering and instead have a local transmitter to boost the signals delivered to the reader. Active tags can be very useful in overcoming harsh communication environments and in situations where accurate tracking is necessary.

The focus of this work will be primarily concerned with the operation of passive RFID tags in a near-field communication link.

Supply Chain Security

An emerging application for wireless power technology is the security of the supply chain for electronic components. Electronic devices constitute a large portion of the $200 billion worth of counterfeit goods that are exchanged every year, and ensuring the supply chain integrity of these components is pivotal to reducing the financial loss due to counterfeiting [7]. One solution to this problem is to have an extremely small (0.01 mm^2) hardware root-of-trust embedded within the package of the host electronic component, as shown in Fig. 1.1. The root-of-trust can be used to authenticate the origin of the components as they pass through the supply chain. It needs to be extremely small not only so that its operation does not interfere with the host's IC, but also so that it can be manufactured for a fraction of a cent per chip [8]. The root-of-trust must be able to support simultaneous wireless power and communication so that it can demodulate the interrogation from the near-field reader and provide an appropriate response by modulating its impedance without the need for an external power source. The operation of the root-of-trust is very similar to that of a passive RFID tag, except that the envisioned device is much smaller than the existing commercial RFID tags and operates at a much larger coupling distance compared to the device size.

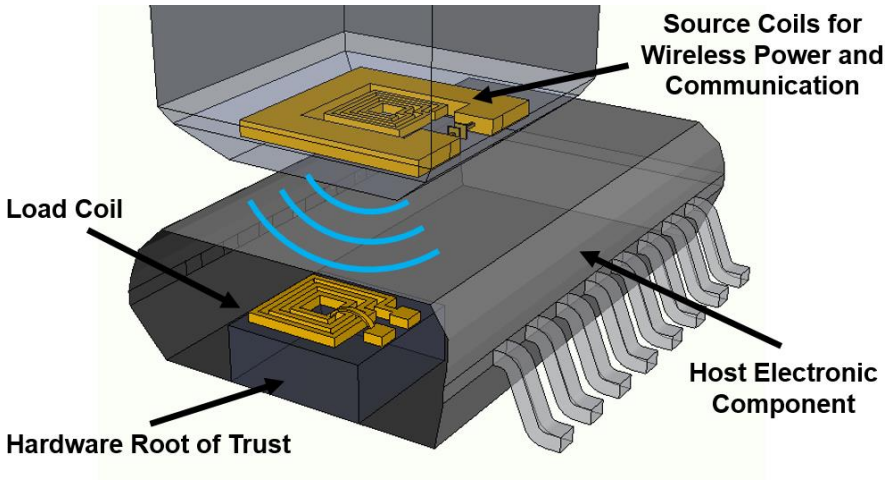

Figure 1.1 Mock-up of a hardware root-of-trust embedded in a packaged electronic component. Courtesy of Liuqing Gao.

There are a few challenges involved in achieving wireless power transfer when the device size is so small. If inductive coupling is used, the mutual coupling is limited by the smallest coil in the

system [9], [10]. Furthermore, a practical implementation of the system would require an operating distance that is at least five times the smallest coil diameter (> 0.5 mm) [9], [11], [12], which degrades the power transfer efficiency. The link is also susceptible to misalignment between the near-field reader and root-of-trust, especially if the reader is manually positioned. In spite of these challenges, recent efforts to shrink RFID tags have demonstrated the feasibility of a hardware root-of-trust for electronic supply chain security applications.

Review of Recent Work

Recent work in chip-scale wireless power technology has yielded devices of impressively small form-factors. In [11] a 1 mm by 0.5 mm on-chip antenna was designed and fabricated with a maximum physical operating distance of 5 mm. The reader antenna for this link was 15 mm by 12 mm in size. The link was designed at 2.45 GHz and operated in the near-field. The on-chip antenna was connected to an integrated circuit which relayed information back to the reader antenna by modulating its load impedance at a rate of 100 kb/s. While this work does not directly characterize the RF-RF power transfer efficiency of the magnetically coupled coils, it provides important details regarding the design of IC-based systems for wireless power transfer and communication.

The smallest commercial RFID tag to date is the Hitachi μ-chip [13], whose dimensions are 0.4 mm by 0.4 mm, including the on-chip antenna. It includes a 0.3 mm by 0.3 mm IC with 128 bit memory using 0.18 μm CMOS technology. The on-chip antenna can be replaced by an external 56 mm by 2 mm antenna for an improved read range, yielding a maximum operating distance of 300 mm using a reader output power of 300 mW. To achieve the maximum operating distance, a tunable slit on the antenna was varied to perform impedance matching between the antenna and IC. While the μ-chip is the smallest commercial RFID chip to date, no performance metrics are reported for the complete 0.4 mm by 0.4 mm tag.

One recent work has reported an experimental RFID tag that is 200 μm by 200 μm [12]. The system operates at 2 GHz with a coupling distance of 1.1 mm between the near-field reader and tag. The tag is able to deliver 100 μW of rectified DC power to an IC load when the near-field reader is transmitting 21 dBm of power, or roughly 125 mW. A varactor with an external bias is used to modulate the tag impedance in order to transmit information from the tag to the reader. The authors

use a single coil for both the reader and tag antennas and report a power transfer efficiency of -29 dB.

While these works demonstrate the feasibility of a sub-mm scale RFID tag that could be used for supply chain security applications, they have not explicitly discussed methods to improve the power transfer efficiency of the link, which is one of the primary challenges for this application space.

1.2 Scope of this Research

This thesis concerns the operation of chip-scale (100s of μm) devices that support simultaneous wireless power transfer and communication. The device size is much smaller than a wavelength at the intended frequency, so the devices are operating in the near-field. This work seeks to address the challenges associated with achieving wireless power transfer for small-scale devices that could be used for electronic supply chain security applications.

The rest of the thesis is organized as follows:

Chapter 2 focuses on the design for the wireless power link and introduces a design strategy to overcome some of the challenges associated with chip-scale wireless power transfer. Electric and magnetic coupling links are compared, and two-coil and three-coil systems are introduced. A customized experimental testbed is presented to validate the operation of the fabricated devices. The effects of misalignment are also explored.

Chapter 3 discusses the design considerations for a rectifier that can support simultaneous power and communication. A rectifier topology is selected and modified for the intended application. A PCB prototype is presented, and the measured results are compared to simulations.

In Chapter 4, the implementation of the hardware root of trust in an IC is presented. Slight modifications are performed on the designs to accommodate the IC environment. Detailed information regarding the design and validation process is presented, as well as post-layout simulations accounting for the parasitics on the chip.

Finally, Chapter 5 gives a summary of the material presented and discusses areas for future work.

Chapter 2: Wireless Power Transfer

There are a few approaches to analyzing near-field coupled systems. From a physical standpoint, the reader and tag contain antenna elements that operate in each other's near-field region. The field distributions can be calculated from Maxwell's equations, and the coupling strength of the link can be determined from the ratio of the coupled to stored electromagnetic energy. Another approach is to treat the antenna elements as coupled resonators, for which equivalent circuit models can be constructed. This approach is preferred since it produces a model that can be integrated in the larger transmit and receive system. Depending on the nature of the electromagnetic coupling, the equivalent model can be treated as a transformer or as a filter. The coupled-resonator filter approach will be used in the subsequent analysis. A comprehensive overview of this analysis can be found in [14].

2.1 Electromagnetic Coupling Schemes

The coupling between two resonators can be described as electric, magnetic, or a combination of both. Electrically coupled resonators use capacitors as their primary reactive elements whereas magnetically coupled resonators use inductors. A rudimentary analysis will be given for both types of coupling, followed by a brief discussion over which scheme is preferred for chip-scale applications.

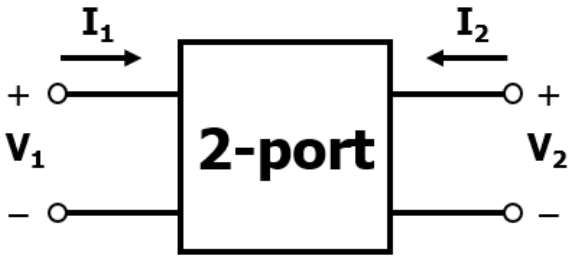

Figure 2.1 Voltage and current conventions

Electric Coupling

Electrically coupled resonators using capacitors are conventionally characterized by their short-circuit admittance parameters, or Y-parameters. The two-port Y-parameters are defined as follows, with the polarities of the port voltages and currents given in Fig. 2.1:

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \tag{2.1}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{2.2}$$

where

$$Y_{11} = \frac{I_1}{V_1}\Big|_{V_2=0} ; Input\ admittance, output\ shorted \tag{2.3}$$

$$Y_{12} = \frac{I_1}{V_2}\Big|_{V_1=0} ; Reverse\ transfer\ admittance, input\ shorted \tag{2.4}$$

$$Y_{21} = \frac{I_2}{V_1}\Big|_{V_2=0} ; Forward\ transfer\ admittance, output\ shorted \tag{2.5}$$

$$Y_{22} = \frac{I_2}{V_2}\Big|_{V_1=0} ; Output\ admittance, input\ shorted \tag{2.6}$$

Any reciprocal two-port network that can be characterized by Y-parameters has an equivalent pi circuit model shown in Fig. 2.2 (a).

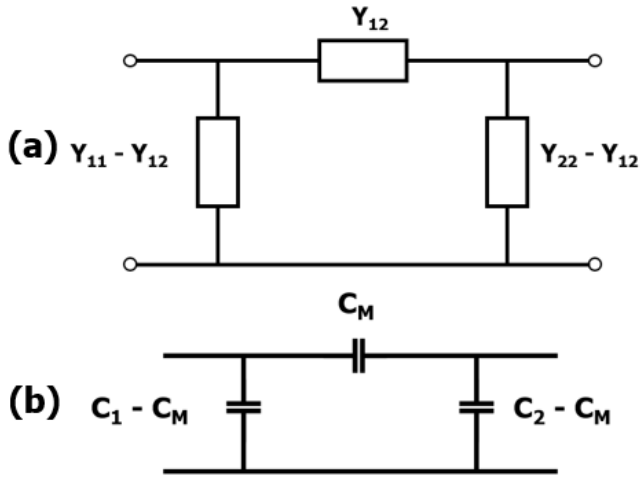

Figure 2.2 (a) Pi equivalent circuit model for a reciprocal two-port network and (b) equivalent circuit model for an electrically coupled resonator

For an electrically coupled system, this results in the equivalent circuit shown in Fig. 2.2 (b), where each port can be loaded with an inductor to form an electrically coupled resonator. C_1 and C_2 represent the self-capacitances of the reactive elements on the reader and tag (which are not the same in general), and C_M represents the mutual capacitance between them. The coupling coefficient for this system is defined as:

$$k_e = \frac{C_M}{\sqrt{C_1 C_2}} \tag{2.7}$$

which relates the coupled electric energy to the stored electric energy of the resonant system. A high coupling coefficient is desirable for wireless power transfer applications. If the Y-parameters of an electrically coupled resonator can be determined, an equivalent circuit model can be constructed to guide system-level design choices.

Magnetic Coupling

Magnetically coupled resonators using inductors are conventionally characterized by their open-circuit impedance parameters, or Z-parameters. The two-port Z-parameters are defined as follows, with the polarities of the port voltages and currents given in Fig. 2.1:

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \tag{2.8}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \tag{2.9}$$

where

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} ; Input\ impedance, output\ open\ circuited \tag{2.10}$$

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} ; Reverse\ transfer\ impedance, input\ open\ circuited \tag{2.11}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} ; Forward\ transfer\ impedance, output\ open\ circuited \tag{2.12}$$

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} ; Output\ impedance, input\ open\ circuited \tag{2.13}$$

Similar to how any reciprocal two-port Y-matrix has an equivalent pi circuit model, any reciprocal two-port network that can be characterized by Z-parameters has an equivalent T circuit model that is shown in Fig. 2.3 (a).

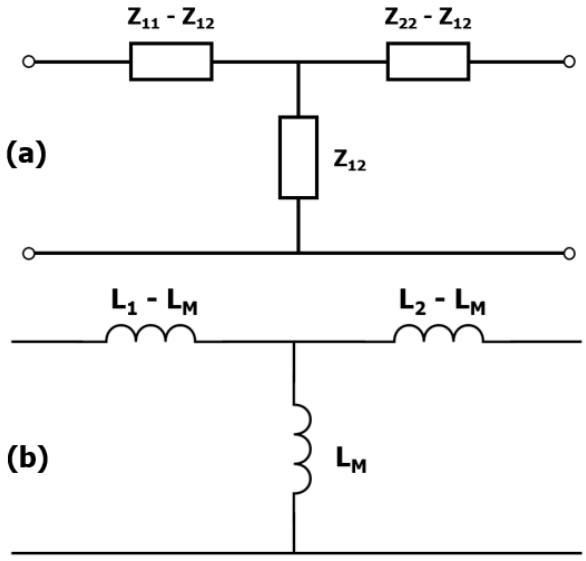

Figure 2.3 (a) T equivalent circuit model for a reciprocal two-port network and (b) equivalent circuit model for a magnetically coupled resonator

For a magnetically coupled system, this results in the equivalent circuit shown in Fig. 2.3 (b), where each port can be loaded with a capacitor to form a magnetically coupled resonator. L_1 and L_2 represent the self-inductances of the reactive elements on the reader and tag (which are not the same in general), and L_M represents the mutual inductance between them. The coupling coefficient for this system is defined as:

$$k_m = \frac{L_M}{\sqrt{L_1 L_2}} \tag{2.14}$$

which relates the coupled magnetic energy to the stored magnetic energy in the resonant system.

Whether it is more advantageous to use electric or magnetic coupling for the coupled resonator will largely depend on the application. In the ideal case, where there are no losses in the system and the reactance values can be made arbitrarily small or large, there is no difference between the two coupling mechanisms. From a mathematical perspective, Y-parameters can be converted into Z-parameters, pi circuit models can be transformed into T circuit models, and vice-versa without any change in performance. At high frequencies, inductors tend to be more lossy than capacitors, so for some applications, an electrically coupled resonator is preferred. However, the primary design constraint for chip-scale wireless power technology is space utilization, and since inductors have more flexibility with respect to the range of inductance values for a given area, magnetically coupled resonators are preferred for this application.

Review of Recent Work

Before discussing the design approaches taken for this thesis, it will be instructive to review some of the recent work that has been done on inductively coupled systems. Prior work on magnetically coupled resonators focused on multiple identically sized coils separated by a "mid-distance" (2~4 coil diameters) [15]–[18]. The coils were larger than typical UHF RFID tag antennas (more than 10s of centimeters) and had relatively low resonant frequencies in the MHz range. The analysis of these systems employed reflected load theory [18], coupled mode theory [19], and a combination of both [20]. However, these analyses neglect non-adjacent coil coupling [18] and assume automatic impedance matching [20]. Thus, they do not address the challenges of wirelessly delivering power to a chip-scale device from a millimeter-scale source, a scenario in which the coil diameters take on drastically different sizes and where there might not be enough room for an on-chip matching network. A couple of these works will be examined in detail.

In [15] a formalism is presented for an inductively coupled resonant system to wirelessly deliver power over a distance that is 4 times the coil diameter. The copper coils are identical, each with a diameter of 50 cm operating at a frequency of 9.9 MHz. The system was designed such that the coils would operate at their self-resonant frequency with a very high Q value of around 950 for each coil. The experimental setup included wirelessly delivering power to a 60 W lightbulb, and with a 15% overall efficiency, this meant driving the transmitter with 400 W of power. While the Q values of the coils were very high and the system was able to achieve wireless power transfer over a mid-distance, the coils had identical dimensions and are much larger than what could be used for a chip-scale application.

The system used in [18] employs multiple coils to facilitate the wireless power transfer. The wireless link is composed of four coils: a power, a sending, a receiving, and a load coil. Each coil has a diameter of 15 cm with a conductor thickness of 1 mm. The power and load coils had one turn, while the sending and receiving coils had eight turns. The system operated at 16 MHz with a relatively wide bandwidth due to the extra resonant frequency introduced by the additional coils. This wide bandwidth was present when the coils were closely spaced, but as the sending and receiving coils were moved farther apart (23 cm spacing), the direct coupling from the power and load coils became negligible and the wide bandwidth was lost. While the coil dimensions from

this experiment are still too large for chip-scale applications, the idea of using multiple coils can be used to overcome some of the challenges of using small inductors.

2.2 Design Approaches

In order to evaluate the performance of a wireless power transfer link, a quantitative figure of merit must be introduced. The power transfer efficiency of a link is a metric that relates the power delivered to the load to the power transmitted by the source. High power transfer efficiency is a critical design consideration for wireless power transfer applications. The power transfer efficiency of a link can be directly computed using the two-port scattering parameters, or S-parameters, which are defined as follows:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.15}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.16}$$

where

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \tag{2.17}$$

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} \tag{2.18}$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} \tag{2.19}$$

$$S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0} \tag{2.20}$$

The wave variables a_i and b_i are normalized parameters with units of $[\text{Watts}]^{1/2}$. Incident waves that are going into the network are designated by a_i, whereas reflected or scattered waves leaving the network are designated by b_i, where 'i' is an index that references a specific port. The advantages of using S-parameters for this application are that they can be easily and reliably measured at high frequencies, and that they can be directly used to determine the power transfer efficiency of a wireless link. A comprehensive overview of S-parameters can be found in [21].

From coupled-resonator filter theory, the power transfer efficiency of a link is determined in the same way that the insertion gain is calculated for a filter, namely by evaluating the $|S_{21}|^2$ of a two-

port network. This quantity is usually expressed in decibels (dB) and is the primary figure of merit for evaluating the quality of the following design approaches to wirelessly deliver power to a chip-scale component.

Two-Coil Link

The challenges of wirelessly delivering power to a chip-scale device will be illustrated using a simple two-coil system. The T circuit model shown earlier in Fig. 2.3 can be redrawn to include the effects of self-resistance of coils and tuning capacitors for resonant system. The modified circuit model is shown in Fig. 2.4, along with an illustration of the coupled coils.

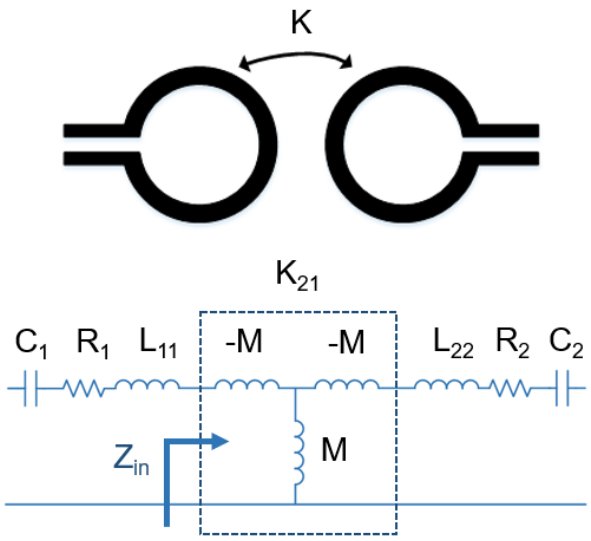

Figure 2.4 Modified circuit model for a two-coil system

The two-port Z-parameters of this circuit are given by

$$Z_{2-coil} = \begin{bmatrix} R_1 + j\omega L_{11} + \frac{1}{j\omega C_1} & j\omega M \\ j\omega M & R_2 + j\omega L_{22} + \frac{1}{j\omega C_2} \end{bmatrix} \tag{2.21}$$

The analysis of the system can be simplified by examining the operation of the sub-circuit enclosed by the dashed line box in Fig. 2.4 and labeled K_{21}. The sub-circuit acts as an impedance inverter and has two-port Z-parameters that are given by

$$Z_{inv} = \begin{bmatrix} 0 & j\omega M \\ j\omega M & 0 \end{bmatrix} \tag{2.22}$$

The impedance inversion can be seen clearly when calculating the input impedance of this simplified circuit:

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}+Z_L} = \frac{\omega^2 M^2}{Z_L} \tag{2.23}$$

where Z_L is the load impedance connected to the second coil. One of the primary disadvantages of this system for chip-scale applications is that the power transfer efficiency is limited by the impedance mismatch: the small coil size limits the amount of mutual inductance that can be achieved, and there is typically not enough space for an on-chip matching network. Hence, if this link were to be used in a 50 Ω system, much of the power would be reflected rather than transmitted to the load coil. A 3D model of a two-coil design was constructed in Ansys HFSS and is shown in Fig. 2.5. The design consists of a 1 mm by 1 mm transmitting coil and a 100 μm by 100 μm receiving coil.

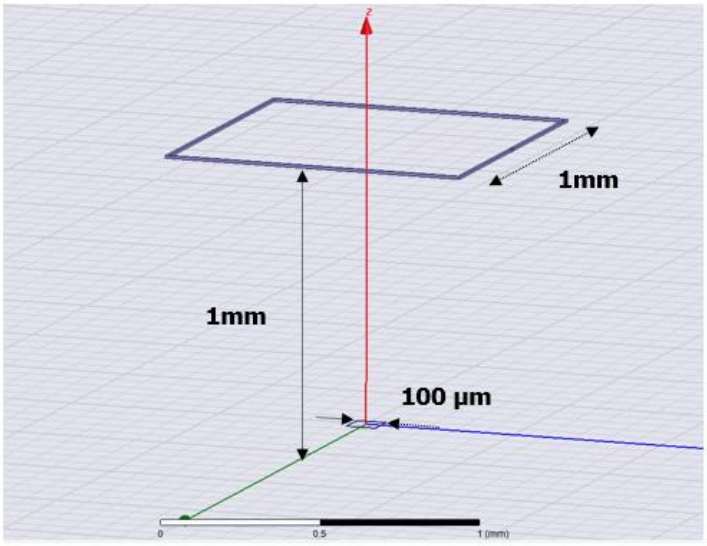

Figure 2.5 HFSS model for a two-coil system

Since the separation distance is 1 mm (which is 10 times the receiving coil diameter), an asymmetric design approach was used to increase the mutual inductance of the system. Series capacitors were added to cause the system to resonate at 2 GHz, and the simulation yielded a mutual inductance of 1.25 pH and a power transfer efficiency of -50 dB. This means that only 0.001% of power transmitted by the source coil was actually delivered to the load coil. In order to

avoid transmitting several watts of power to operate the link, a different topology with a higher power transfer efficiency should be explored.

Tri-Coil Link

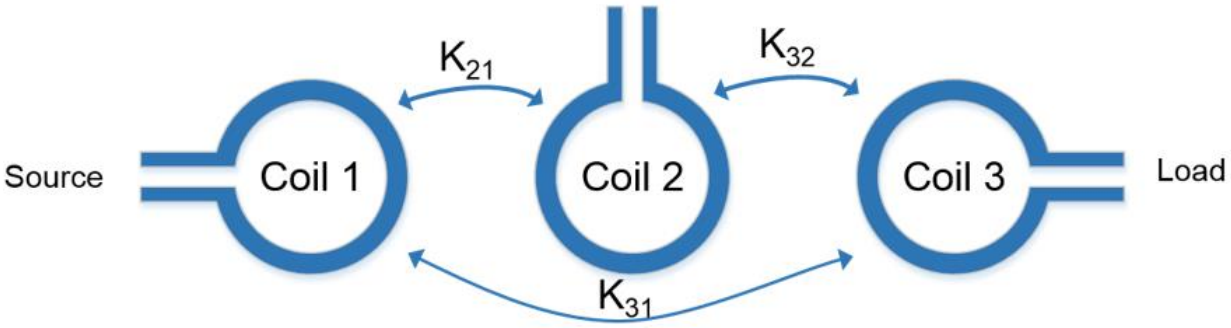

Figure 2.6 Illustration of a tri-coil system

One of the ways to mitigate the poor efficiency due to impedance mismatch is to introduce an intermediate coil, as shown in Fig. 2.6. This intermediate coil can be thought of as a matching network between the source and load coils, but this adds complexity to the equivalent circuit model, as shown in Fig. 2.7. The impedance inverter sub-circuit that was present in the two-coil system appears three times in the tri-coil link, where they are designated by the K_{21}, K_{32}, and K_{31} blocks in the equivalent circuit model.

One way to simplify the analysis is to design the coils such that the direct coupling between the source and load coils (coils 1 and 3) can be neglected at the design frequency. This can be done by making the source and intermediate coils coplanar and by using a large intermediate coil. The coplanar source and intermediate coils will ensure a large coupling between coils 1 and 2, and the large intermediate coil will result in a large coupling between coils 2 and 3. This design choice will also lead to a smaller coupling between coils 1 and 3 since they have similar form factors and are separated by a distance of 10 coil diameters. The simplified equivalent circuit model for the tri-coil link is shown in Fig. 2.8, which has two impedance inverters rather than three.

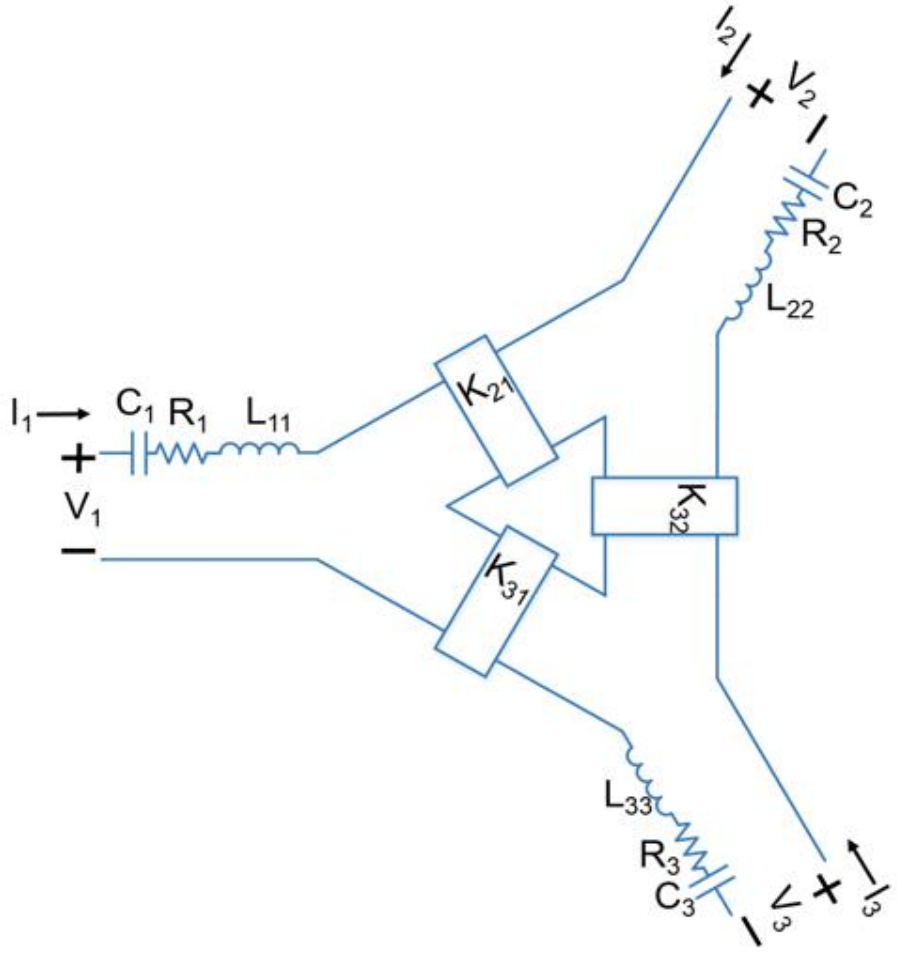

Figure 2.7 Equivalent circuit model of a tri-coil system. Courtesy of Justin Postma.

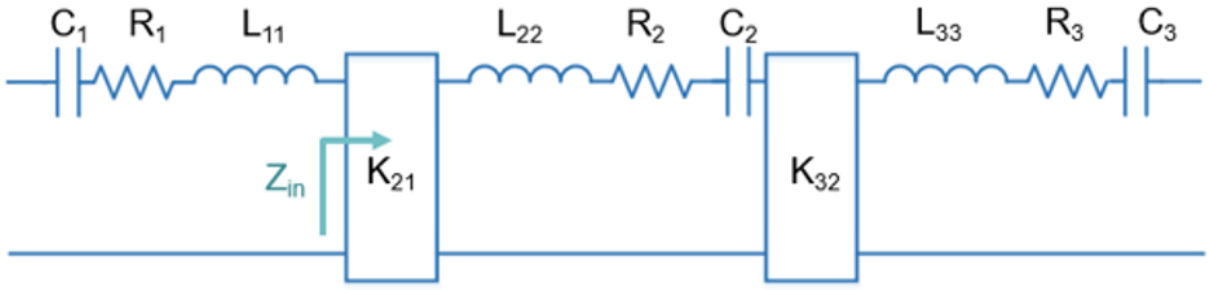

Figure 2.8 Simplified equivalent circuit model of a tri-coil system

If the intermediate coil is designed to have very low loss (i.e. $R_2 \sim 0$) and C_2 is selected to tune out its self-inductance at the desired frequency, the input impedance becomes

$$Z_{in} = \frac{M_{21}^2}{M_{32}^2} Z_L \tag{2.24}$$

where M_{21} and M_{32} are the mutual inductances between coils 1 and 2, and between coils 2 and 3 respectively. If this tri-coil link were to be used in a 50 Ω system (Z_S and Z_L = 50 Ω), a good impedance match can be achieved even if the mutual coupling is relatively weak as long as M_{21} is roughly equal to M_{32}. In practice, the load coil is not terminated with 50 Ω, but rather with a rectifier to convert the RF waveform to DC power. A detailed analysis for the theory of operation of the tri-coil link using coupling quality factors can be found in [9].

A 3D model of the tri-coil link was constructed in HFSS and is shown in Fig. 2.9. The properties of each coil are listed in Table 2.1. The intermediate coil has a large width in order to reduce its self-resistance and increase its Q, which is a critical component in increasing the power transfer efficiency of the link. The intermediate coil is loaded with a capacitor that can be used to set an arbitrary operating frequency, which makes the tri-coil link a frequency-scalable technology platform. In general, higher frequencies can produce better efficiencies since the mutual coupling (defined by ωM) is proportional to the operating frequency. However, the operating frequency cannot be made frivolously high, as it is limited by the lowest self-resonant frequency of the coils, beyond which it will operate in the capacitive region.

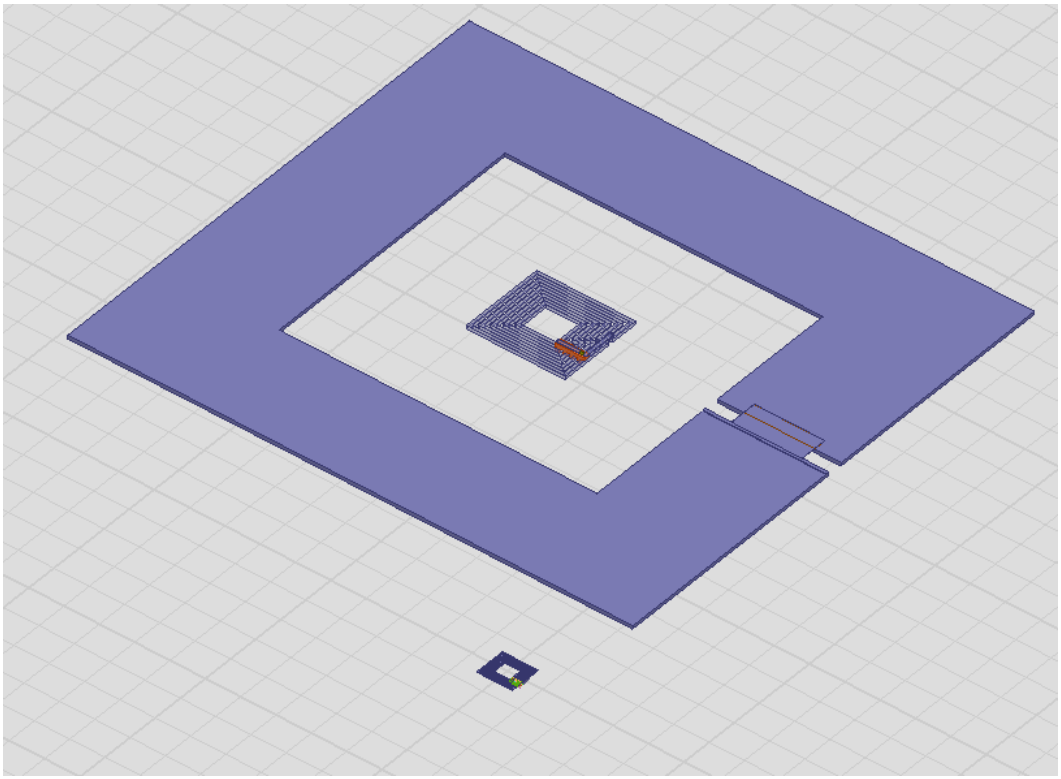

Figure 2.9 HFSS model of a tri-coil system

Table 2.1 Physical Properties of Tri-Coil System

Coil #	No. of Turns	Outer Diameter	Segment Width	Segment Spacing
1	5	300 µm	10 µm	10 µm
2	1	1.5 mm	350 µm	N/A
3	5	100 µm	3 µm	3 µm

The simulated result of the tri-coil link is shown in Fig. 2.10, which plots the S_{21} of the system in dB as a function of frequency. As can be seen from the graph, the tri-coil link has a simulated efficiency of -29 dB at 5.7 GHz at a separation distance of 1 mm, which is ten times the smallest coil diameter.

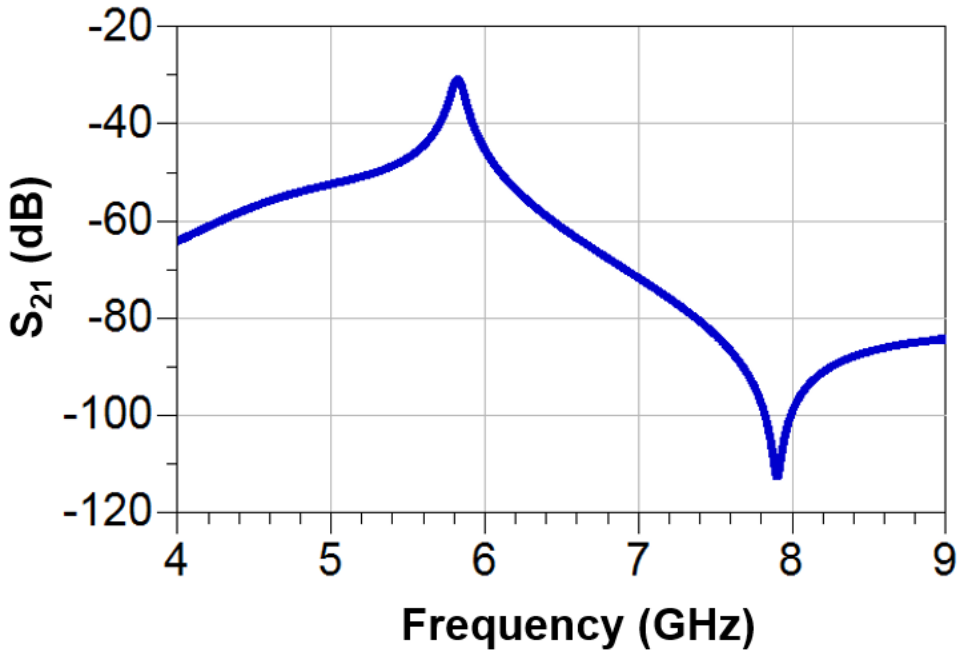

Figure 2.10 HFSS simulations results for the tri-coil link

2.3 Experimental Validation

In order to experimentally validate the tri-coil inductive link, a two-substrate approach was employed, which involves fabricating coils 1 and 2 (herein referred to as the source coils) on a separate substrate from coil 3 (the load coil). This method provides numerous advantages over fabricating the coils on a single substrate, including 1) flexibility and diversity of misalignment measurements and 2) reduced fabrication time and complexity by removing the need for thru-silicon-vias.

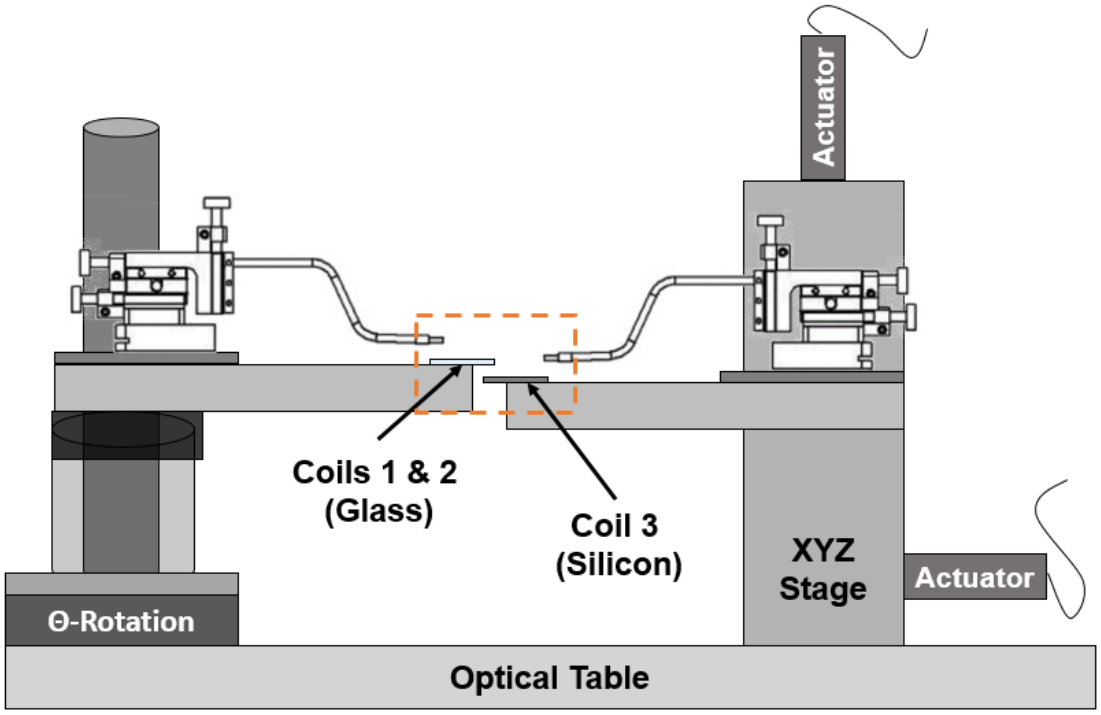

Figure 2.11 Side-view mock-up of the measurement setup

This approach requires a customized experimental testbed, which is shown in Fig. 2.11. The source coils are fabricated on a glass wafer, whereas the load coil is fabricated on a silicon wafer. The wafers are diced into singulated samples that are about 10 mm by 20 mm in size. Each sample is suspended over an aluminum plate and held in place by a set of vacuum holes, as can be seen in Fig. 2.12. The source coils are fabricated on glass so that the load coil is visible through the transparent substrate, which is useful for alignment purposes. The coils are fabricated using gold, where the bridges and capacitors are constructed using benzocyclobutene (BCB). An optical image of the fabricated coils can be seen in Fig. 2.13.

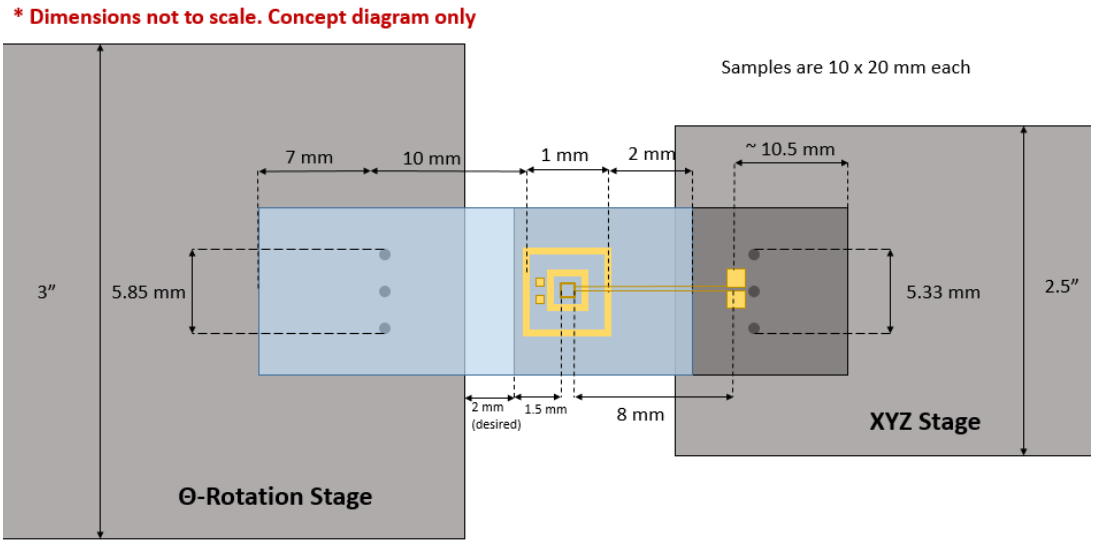

Figure 2.12 Top-view mock-up of the measurement setup

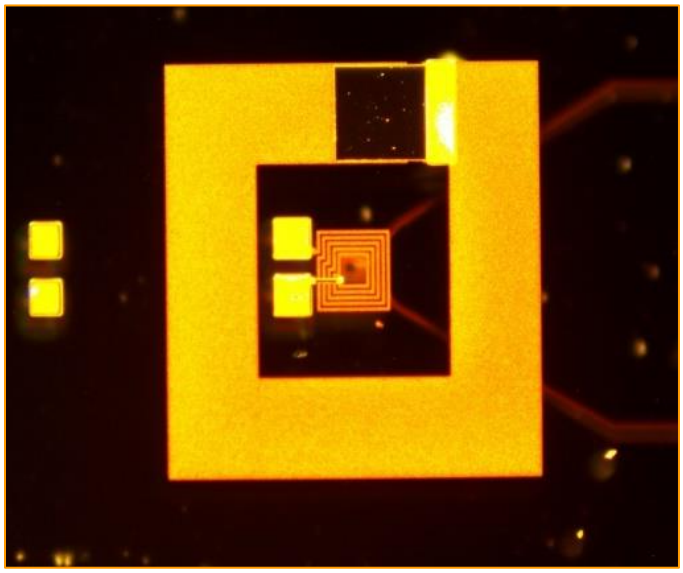

Figure 2.13 Optical image of fabricated coils. Fabrication courtesy of Yansong Yang.

The alignment of the system is controlled by a set of high-precision translational and rotational platforms (Thorlabs PT3-Z8 and PR01). The translational XYZ stage (which supports the load coil) has 25 mm of movement range in each direction with sub-micron resolution. This stage also supports software-defined movement for more precision. Angular alignment (in the XY plane) is controlled by a rotational platform (which supports the source coils) with resolution as low as 5 arcmin. The system can be precisely aligned using a set of alignment markers, shown in Fig. 2.14. Crosshairs with trace thicknesses on the order of 20 μm are fabricated on the bottom of the

glass substrate, and their corresponding target boxes are fabricated on the top of the silicon substrate. The crosshairs lie exactly within their corresponding target boxes when the system is in alignment.

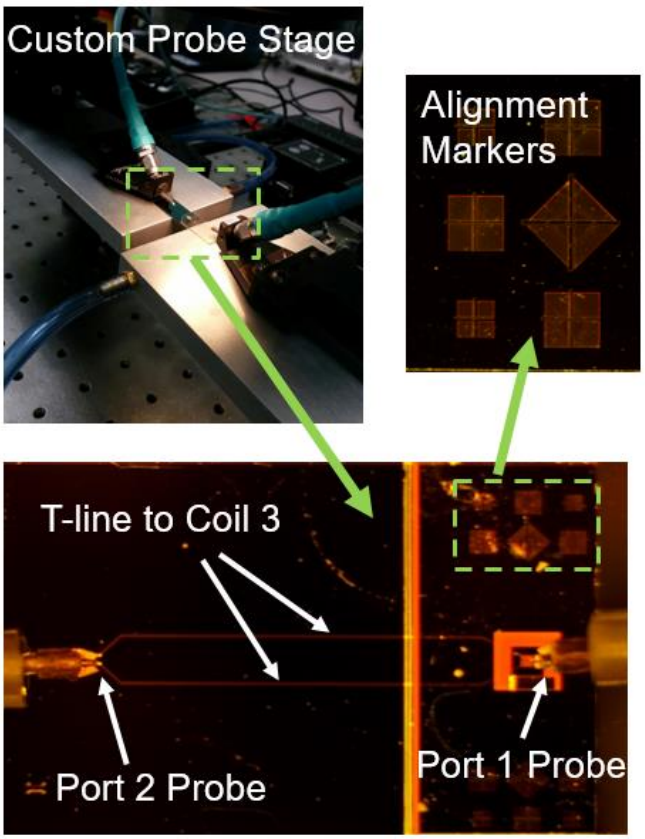

Figure 2.14 Measurement setup with alignment markers

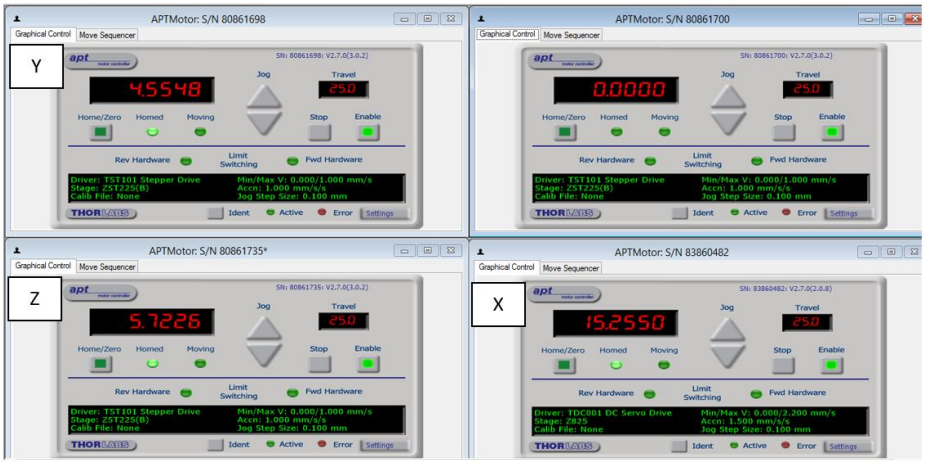

Figure 2.15 Software that controls the movement of the XYZ platform. The travel distances displayed are in units of millimeters.

The measurement procedure is as follows:

1. Use the translational actuators to bring the samples close to each other and achieve alignment using the alignment markers.
2. The samples should be in contact (500 µm of glass-silicon separation). Record the position of the XYZ platform (example shown in Fig. 2.15) and measure the system in perfect alignment.
3. Lower the silicon sample by 500 µm and move in the XY direction using the software to ensure exact misalignment values (e.g. 20 µm in the X-direction or 100 µm in the Y-direction).
4. Raise the silicon sample by 500 µm and measure the system in precisely defined misalignment.

The measured misalignment results for this system are shown in Fig. 2.16 and Fig. 2.17. Figure 2.16 shows the de-embedded measured results of the tri-coil link for various vertical separation distances, where the power transfer efficiency degrades by about 7 dB when going from 500 µm to 1.5 mm of vertical separation. The measured lateral misalignment results, with the effects of the transmission line to the load coil de-embedded, are shown in Fig. 2.17. As can be seen in the figure, the 5.7 GHz tri-coil design had a measured peak RF power transfer efficiency of -29 dB that degrades by about 6 dB over a lateral misalignment of 600 µm.

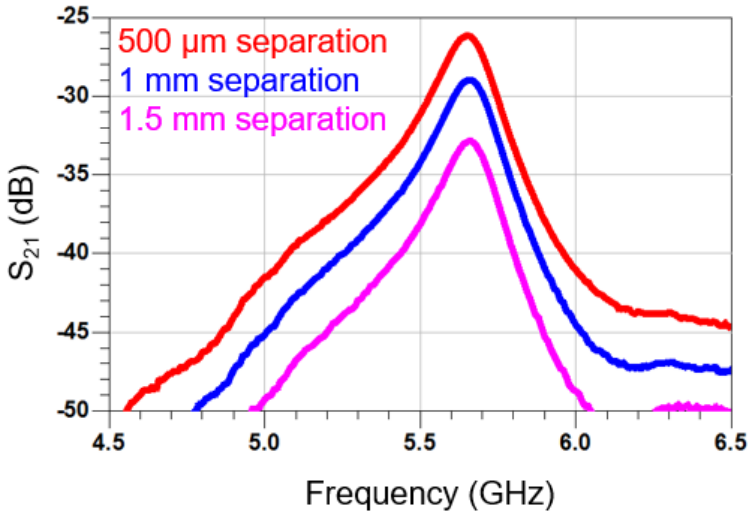

Figure 2.16 De-embedded measured results for the power transfer efficiency (S_{21}) of the 5.7 GHz tri-coil design with various vertical separation distances

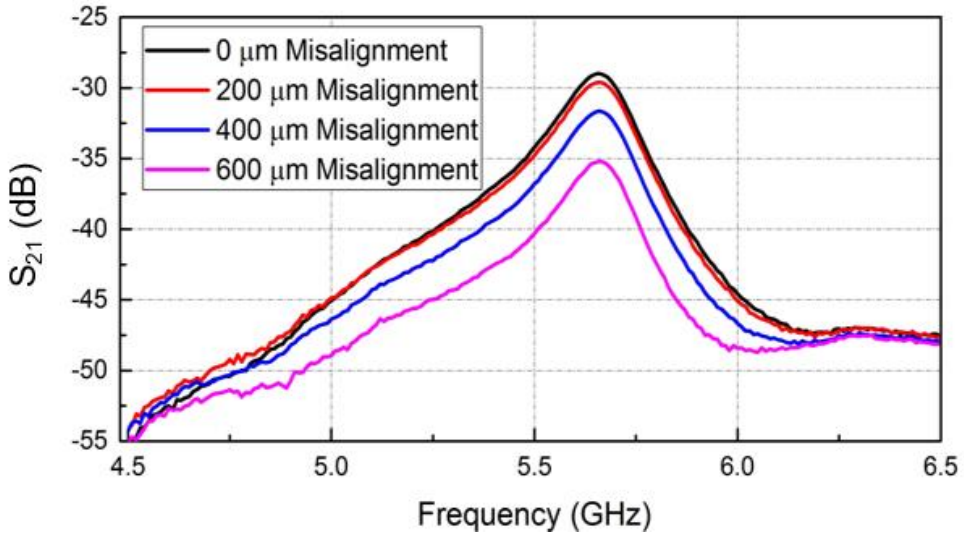

Figure 2.17 De-embedded measured results for the power transfer efficiency (S_{21}) of the 5.7 GHz tri-coil design with various lateral misalignment distances for a vertical separation distance of 1mm

Chapter 3: Simultaneous Power and Communication

Since the tri-coil link has been demonstrated to wirelessly deliver power successfully and has some resilience to misalignment, the next step is to integrate it into a system that can support simultaneous power and communication. A key aspect to achieving this is in the rectifier design. In order for the rectifier to perform simultaneous RF-DC conversion and amplitude-shift keying (ASK) demodulation, a power splitting technique is used [22]. Part of the incoming RF signal from the reader is sent along one branch of the circuit to be rectified while the other part is demodulated using an envelope detector. The rectifier topology will be discussed first.

3.1 Rectifier Design Considerations

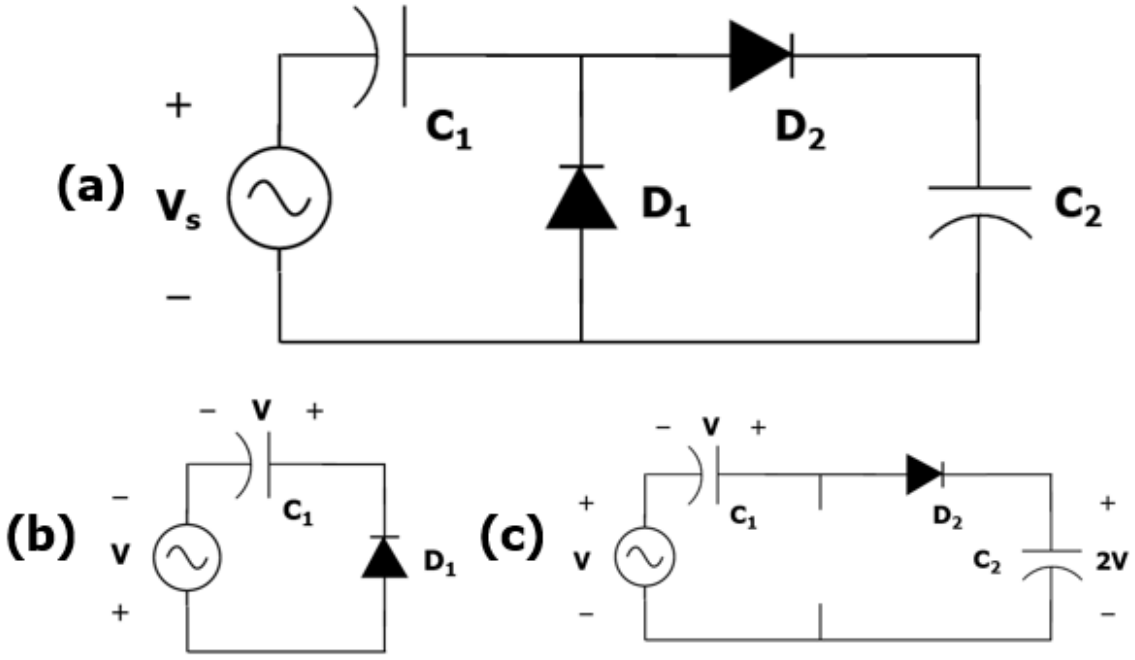

Figure 3.1 (a) Voltage doubler, (b) voltage clamp, and (c) half-wave rectifier schematics

One of most fundamental types of rectifying circuit is the voltage doubler, the schematic of which is shown in Fig. 3.1 (a). The circuit consists of a voltage clamp and a peak detector, also known as a half-wave rectifier. The operation of the doubler is illustrated in Fig. 3.1 (b) and 3.1 (c). During the negative half-cycle of the RF excitation, the shunt diode D1 turns on and charges the capacitor to a voltage equal to the amplitude of the RF signal (minus the voltage drop across the diode). During the positive half-cycle, the shunt diode is reverse biased and looks like an open, whereas

the series diode D2 conducts and charges the capacitor to twice the RF amplitude voltage due to the added voltage from the first capacitor. Since the output is charged only every half cycle, this particular circuit is also called a half-wave voltage doubler.

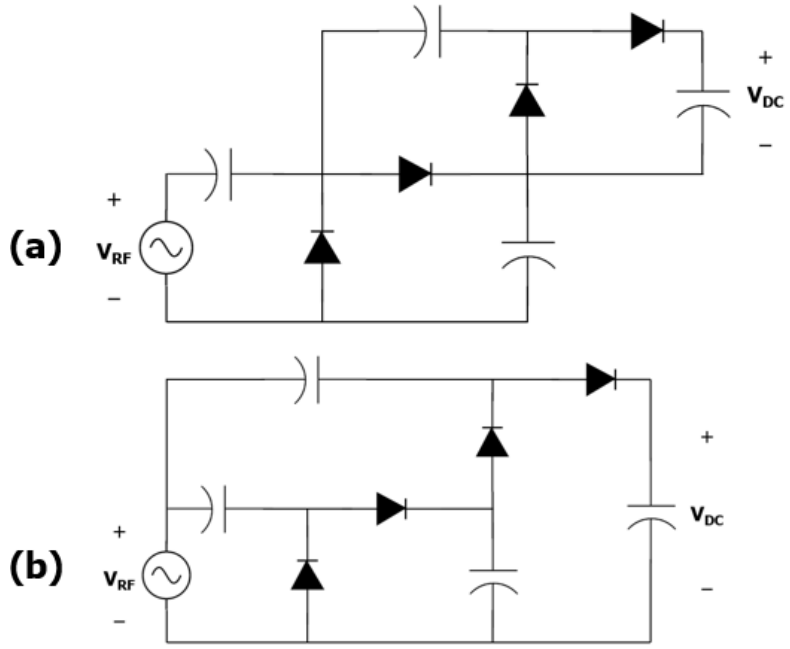

Figure 3.2 (a) Villard multiplier and (b) Dickson multiplier schematics

A voltage multiplier can be obtained by cascading multiple voltage doubler circuits. These can be used to increase the voltage at the load, but this does not necessarily come with increased power efficiency. It is preferable to use a voltage multiplier circuit for low-power applications since the incident RF voltage amplitude is typically very small. There are two basic types of multiplier topologies, as shown in Fig. 3.2. The first is the half-wave series multiplier, also known as a Villard multiplier, whereas the second is the half-wave parallel multiplier, also known as a Dickson multiplier. While there are no significant differences between them in terms of rectifying performance [5], there are design considerations that would lead to selecting one over the other for a particular application. In general, parallel multipliers require less capacitance per stage than their series counterparts, which is beneficial when circuit area is a concern [23]. Moreover, the parallel configuration of each stage results in a lower input impedance, which is useful for matching the impedance to the tag antenna. Series multipliers are useful for high-voltage applications since there is not as much voltage stress on the capacitors for each successive stage (which happens in the

case for parallel multipliers). Since high voltage is not a concern, the parallel topology will be used for this application.

It is apparent that any voltage drop across the diode in the voltage doubler circuits will reduce the rectification efficiency of the circuit. Therefore, diodes with the lowest turn-on voltages are preferred for wireless power transfer applications. This is especially important if the incident RF energy to the circuit is low because the diodes will not be able to conduct if the RF waveform cannot overcome the voltage threshold of the devices. Another consideration for the diode selection is the switching time, as the diodes need to turn on and off quickly in response to the high frequency carrier of the link. A diode that has both of these characteristics is the Schottky diode, which consists of a metal-semiconductor junction. Some other favorable characteristics are low equivalent resistance, low junction capacitance, and high saturation current, but it is difficult to have all three in the same device since high saturation current typically results in higher junction capacitance.

Since the topology and composition of the multipliers are known, the next step is to determine the number of stages that will result in the best performance for a given application. Keysight's Advanced Design System (ADS) is used to set up the simulation environment for this determination. The ADS schematic of a two-stage Dickson rectifier is shown in Fig. 3.3.

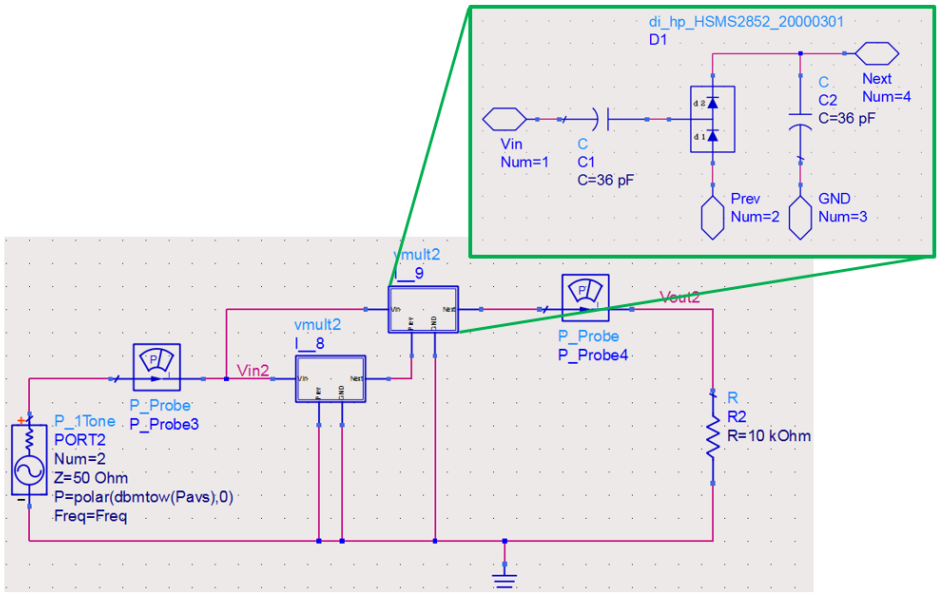

Figure 3.3 ADS schematic for a two-stage Dickson rectifier

Increasing the number of stages will increase the output voltage of the rectifying circuit, but it does not guarantee a higher rectification efficiency [5]. There are two different efficiencies that can quantify the performance of the rectifier. The first is called the conversion efficiency, which is defined as

$$\eta_c = \frac{DC\ Output\ Power}{Incident\ RF\ Power - Reflected\ RF\ Power} \tag{3.1}$$

The conversion efficiency takes the ratio of the DC output power to the input power of the circuit at the fundamental frequency. It describes how much RF power is converted to DC rather than being dissipated in the rectifier or converted to other harmonics. The second is called the overall efficiency, which is defined as

$$\eta_0 = \frac{DC\ Output\ Power}{Incident\ RF\ Power} \tag{3.2}$$

This takes the ratio of the DC output power to the power available from the source, i.e. the power available from the tag antenna. The overall efficiency is a more valuable metric for the performance of the device since it accounts for mismatch loss in the efficiency calculation. The overall efficiencies for the Dickson multipliers comprised of different numbers of stages are shown in Fig. 3.4.

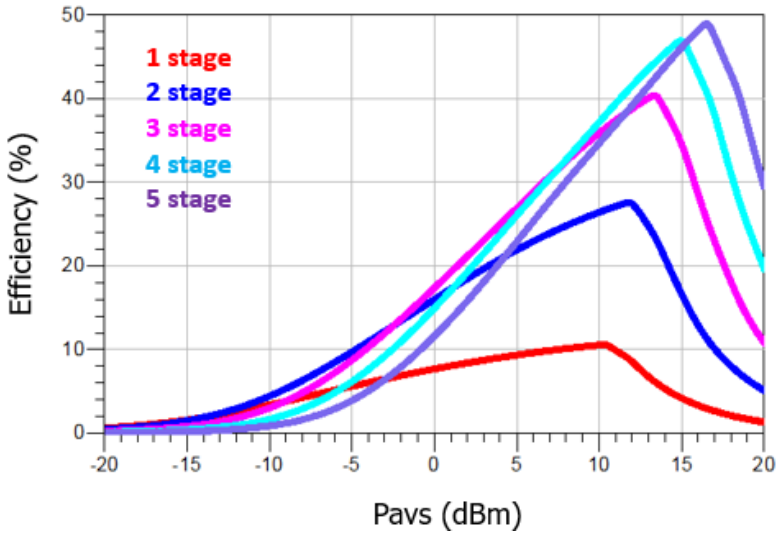

Figure 3.4 Effect of number of stages on the overall efficiency of the rectifier

The efficiency of a rectifier depends on a number of parameters. As can be seen from the previous figure, the rectifier efficiency depends on the number of stages that comprise the multiplier. One general observation is that the multipliers with more stages perform better at higher input powers (e.g. when the power available from the source is greater than 10 dBm). The efficiency also depends on the load connected to the rectifier, but since this is not always controllable, it will not be investigated here. It is worth recognizing that the efficiency for a particular design varies with input power, which suggests that the circuit can be optimized for better performance for a given input power.

The diodes that make up the rectifier are nonlinear, so the circuit itself also exhibits nonlinear characteristics. One of the most critical consequences of this nonlinearity is that the input impedance to the circuit is dependent on its input power. A matching network can be used to improve the overall efficiency of the rectifier, but when a matching network is implemented in the system, the power delivered to the rectifier changes, which in turn changes its input impedance. This results in an impedance mismatch in the system, even though a matching network is employed. It follows that a good matching network design for a rectifier must produce an impedance match both at the desired frequency and at the intended input power level.

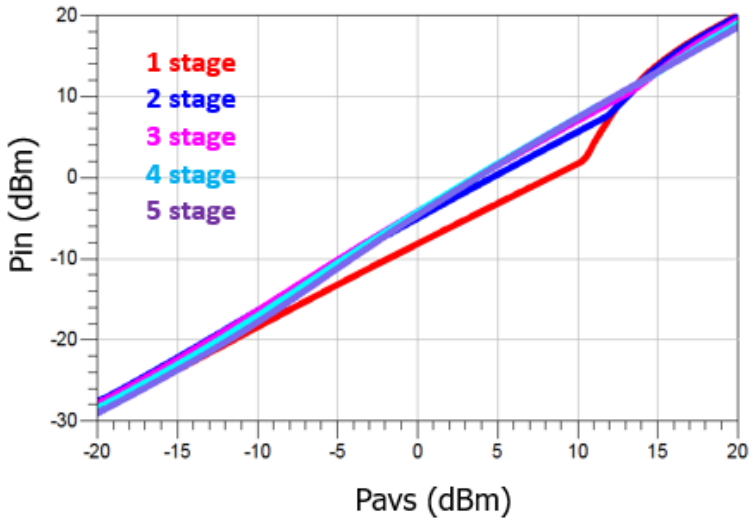

Figure 3.5 Effect of number of stages on mismatch loss as a function of power available from the source

One way to do this in ADS is to use a combination of large signal S-parameter (LSSP) and harmonic balance (HB) simulations. First, an HB simulation is performed to determine the relationship between the power available from the source (Pavs) and power delivered to the input

of the rectifier (Pin), as shown in Fig. 3.5. The difference between these two values is the input mismatch loss. The desired input power can be determined from the link budget of the system; e.g. if the power from the transmitter is 30 dBm and the RF-RF power transfer efficiency of the link is -30 dB, then 0 dBm of power is expected to be delivered to the rectifier. If the mismatch loss between the source and the rectifier is found to be 10 dB for the desired power level, then a Pavs value of 10 dBm should be used to extract the input impedance of the rectifier at the design frequency. This can be done using an LSSP simulation, which can extract the input impedance of the circuit for a given Pavs level. A matching network designed to match this impedance with the source impedance will result in optimal performance of the rectifier for the desired power level and frequency. The efficiencies of the voltage multipliers with matching networks designed for 0 dBm input power are shown in Fig. 3.6.

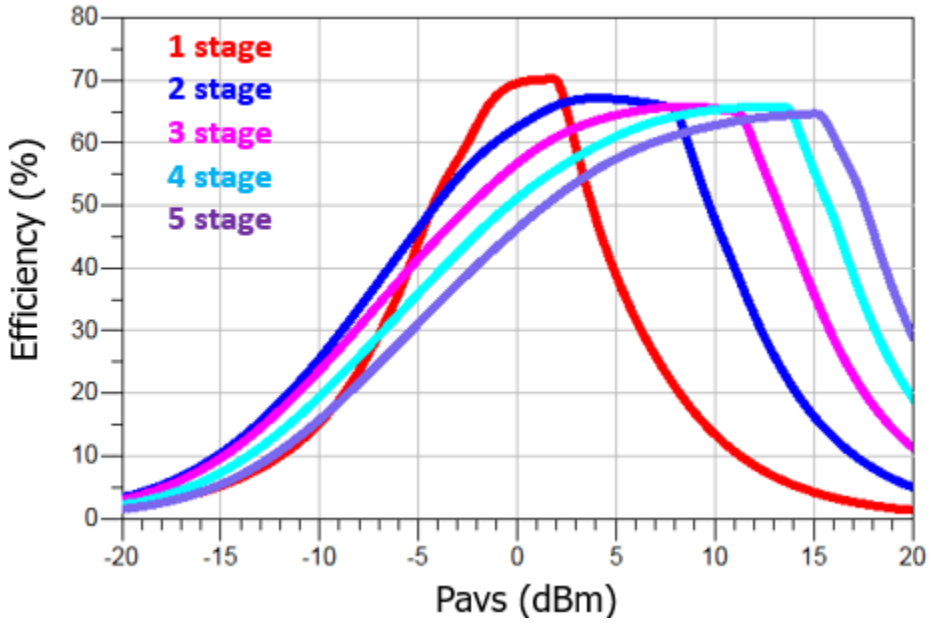

Figure 3.6 Overall efficiencies of multi-stage rectifiers with matching networks

3.2 Tag Demodulation

Now that the rectifier design considerations have been outlined in detail, the next step is to modify the design to accommodate simultaneous RF-DC conversion and ASK demodulation. The simplest way to achieve this is to employ a power splitting technique [22]. This technique can be implemented using a modified two-stage Dickson rectifier, as shown in Fig. 3.7. The first stage of the rectifier builds up charge that is pumped to the second stage of the circuit but also doubles as

an envelope detector for demodulation. The second stage of the rectifier performs the necessary RF-DC conversion that will be used to power the on-chip circuits in the eventual IC integration. The compact design is desirable since it does not require separate rectification and demodulation circuits. This will leave room for other circuitry on the eventual 0.1 mm by 0.1 mm chip. One major challenge associated with this technique is the resistive loading of the first stage, which degrades the overall RF-DC conversion efficiency of the rectifier. This consequence can be mitigated by the enhanced RF-RF power transfer efficiency provided by the tri-coil link. One alternative to this technique is to have a separate power management unit to regulate the output of the rectifier and supply DC power to the circuits, where the ripple on the rectifier output signal can be used as the logic input to the chip. While this can greatly improve the rectification efficiency of the circuit, it comes with cost of larger and more complex circuitry.

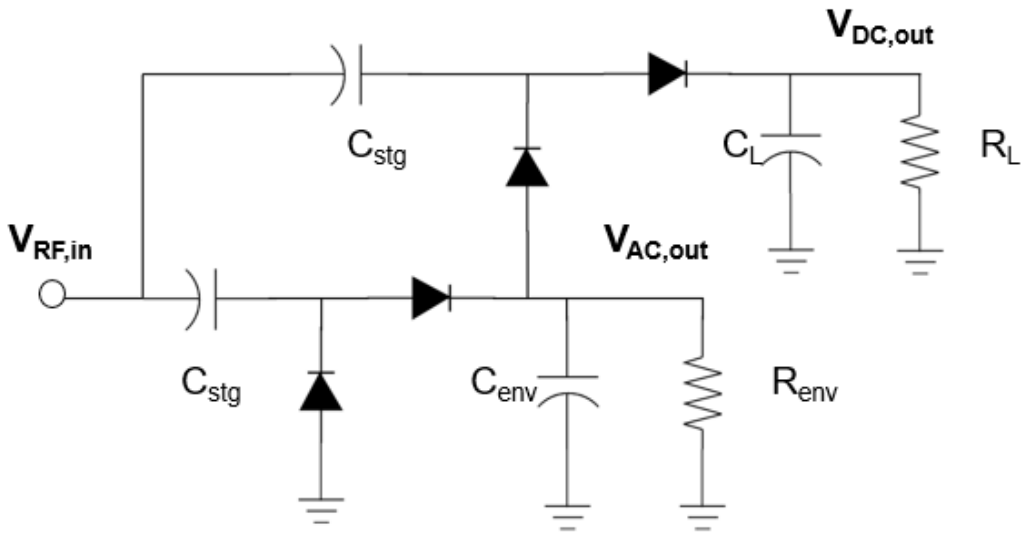

Figure 3.7 Rectifier and envelope detection circuit schematic

In order for the first stage to successfully demodulate the incoming ASK-modulated waveform, the envelope detector's component parameters must satisfy the following inequality:

$$\frac{1}{f_c} \ll R_{env}C_{env} \ll \frac{1}{f_m} \tag{3.3}$$

where f_c is the carrier frequency and f_m is the modulation frequency. For example, if the carrier frequency is 2.48 GHz and the modulation rate is 1 Mb/s, the RC time constant of the envelope detector needs to be between 400 ps and 1 μs. After several design iterations to obtain acceptable values for the output DC voltage and demodulated output for a carrier frequency of 2.48 GHz, the

component values in Table 3.1 were obtained. The Avago HSMS-2852 Schottky diodes were selected for their low turn-on voltage of 150 mV and convenient packaging for voltage multiplier applications. The design was verified using HB and transient simulations in ADS, and its schematic is shown in Fig. 3.8.

Table 3.1 Components Used in the Rectifier Circuit

Component	Value
C_{stg}	36 pF
C_{env}	120 pF
C_L	10 nF
R_{env}	1.5 kΩ
R_L	4.7 kΩ
Diodes	HSMS-2852

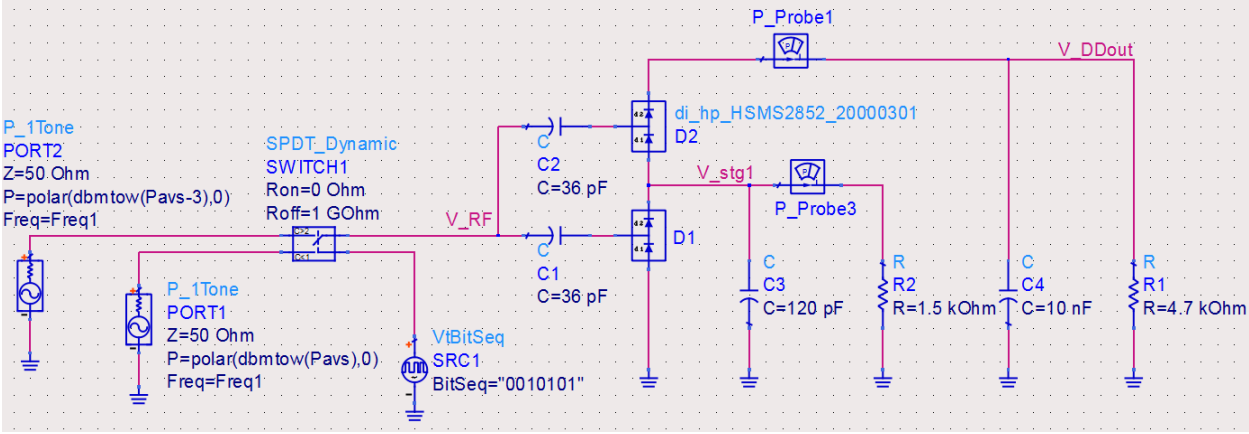

Figure 3.8 ADS schematic for the rectifier and envelope detection circuit

The incident RF signal was ASK modulated with a modulation depth of 50% and contained a bit sequence of 1101010 at a rate of 1 Mb/s. The average input power for this modulated signal can be calculated as

$$P_{avg} = \frac{N_H P_H + N_L P_L}{N_H + N_L} \tag{3.4}$$

where N_H and N_L are the number of high and low states in the bit sequence, respectively and P_H and P_L are the associated powers of the high and low states, respectively. For an average input power of 1.2 mW, the designed two-stage rectifier had a simulated conversion efficiency of 19.6%.

The moderate conversion efficiency is a consequence of the power splitting technique, but the output DC power is still sufficient for low power applications.

3.3 Experimental Validation

The PCB for the rectifier was designed in the EAGLE CAD software. The trace widths were 4.7 mm, which were designed to be 50 Ω transmission lines for the chosen substrate. The PCB was fabricated using an LPKF Protomat S103 milling machine on a Rogers duroid 5880 board. The fabricated board with the components is shown in Fig. 3.9.

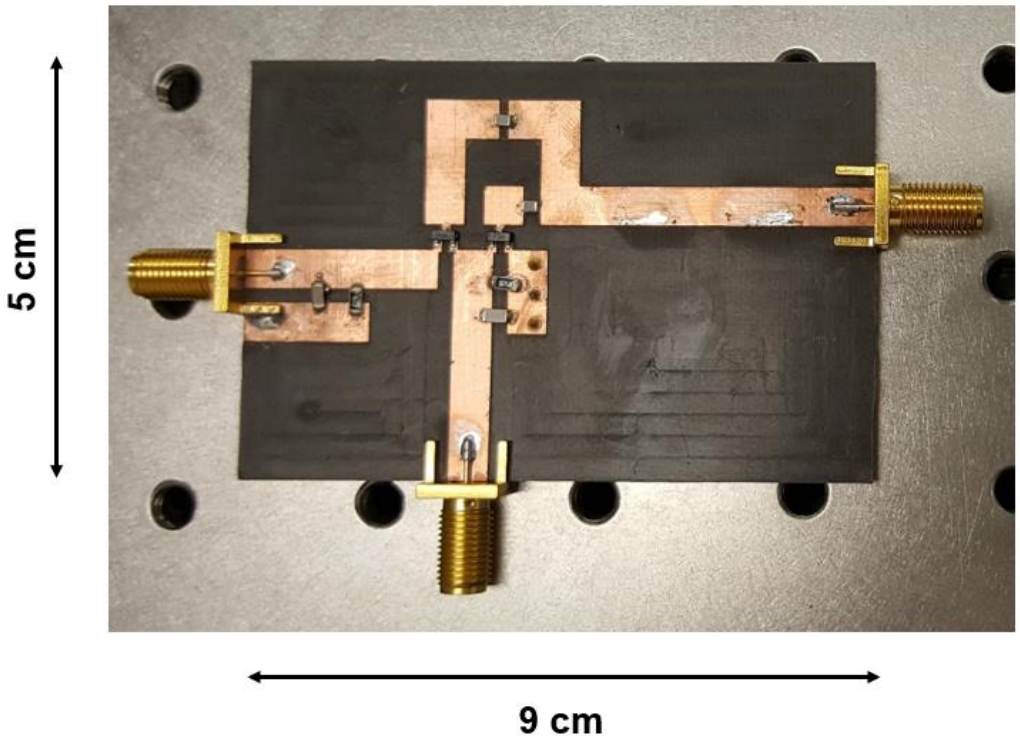

Figure 3.9 Fabricated two-stage rectifier prototype

A block diagram for the measurement setup for simultaneous wireless power transfer and communication is shown in Fig. 3.10. A 50 GB/s Tektronix AWG70001A was used to transmit the ASK-modulated waveform, which was amplified by a Mini-circuits ZVE-3W-83+ 2-8 GHz power amplifier (PA) which can output up to 2W of power. An isolator was used to protect the output of the PA from any strong reflections that might come back from the tri-coil link. The precise output power of the transmitter was controlled using a tunable attenuator, which also improved the return loss seen at the load to the PA.

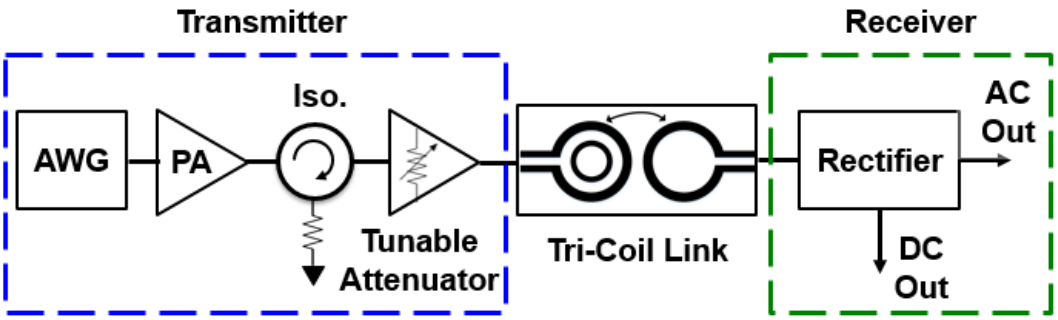

Figure 3.10 Block diagram of the system for simultaneous wireless power transfer and communication

The source and load coils of the tri-coil link were wirebonded to PCBs in order to interface with the transmitter and the customized rectifier. The tri-coil link was aligned using a modified version of the customized experimental testbed described in the previous chapter and is shown in Fig. 3.11. The output of the rectifier was measured using an Agilent MSO7104B oscilloscope. A 20 dBm RF waveform with a carrier frequency of 2.48 GHz was modulated at a rate of 1 Mb/s and transmitted to the input of the tri-coil link. The modulated signal contained an arbitrary repeated bit sequence of 1101010 with a modulation depth of 3 dB. The tri-coil link and rectifier successfully delivered 0.136 mW of DC power to the 4.7 kΩ load while simultaneously providing a demodulated baseband signal for communication. The large RF-DC efficiency of the link and rectifier was boosted by the parasitic coupling of the PCB transmission lines.

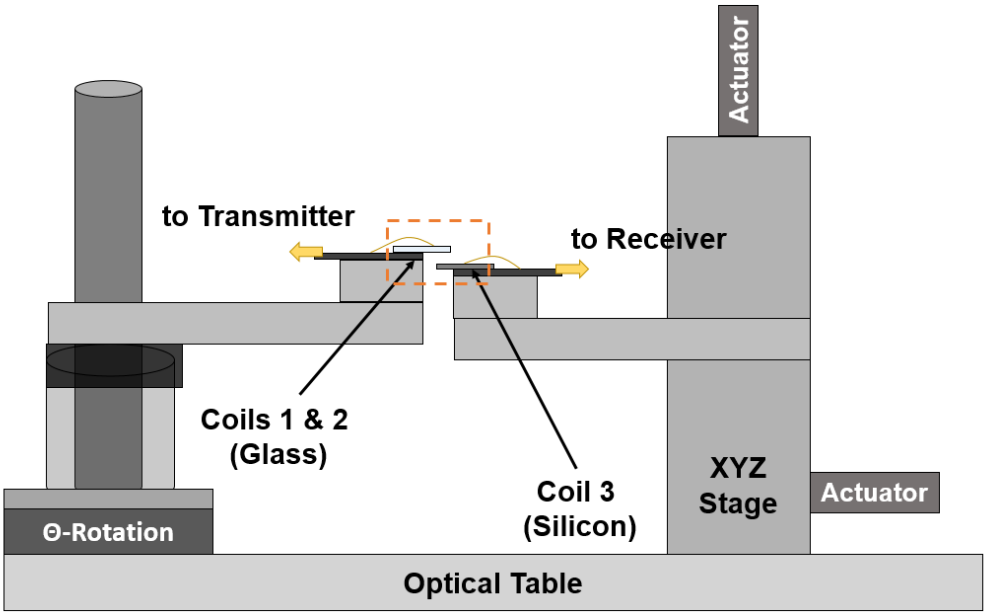

Figure 3.11 Modified experimental testbed for wirebonded samples

As shown in Fig. 3.12, the measured DC output of the rectifier had a steady state value of around 800 mV, corresponding to 136 µW of power delivered to the 4.7 kΩ load. The measured 0 – 90% rise time of the DC output was around 28.4 µs. The discrepancy between the measured and simulated results can be attributed to the imperfect impedance match between the rectifier and coil, as well as the parasitics introduced by the wirebonds, RF connectors, and PCB transmission lines. In Fig. 3.13, it can be seen that the simulated and measured results of the demodulated output of the envelope detector stage are in good agreement. The measured demodulated output had a DC offset of about 415 mV and a voltage swing of about 30 mV.

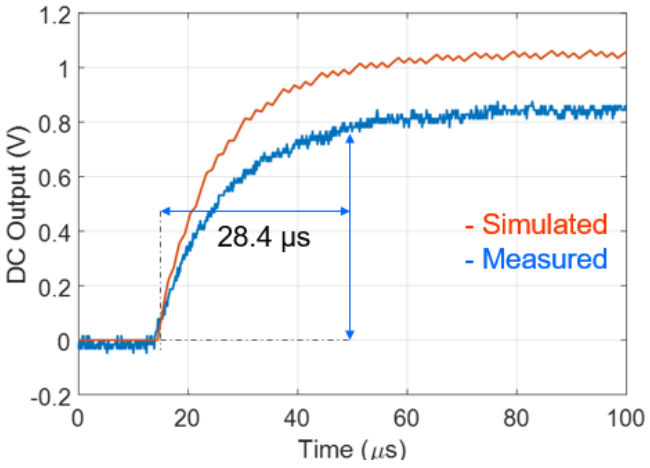

Figure 3.12 Simulated and measured results for the DC output of the rectifier

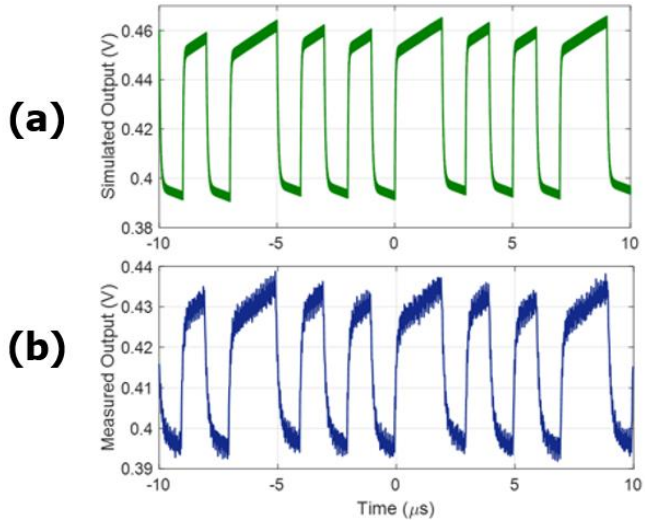

Figure 3.13 (a) Simulated and (b) measured output of the envelope detector for a repeated bit sequence of 1101010 at 1 Mb/s

Chapter 4: Chip-Scale Integration

Now that a system has been demonstrated to provide simultaneous wireless power transfer and communication, the next step is to implement it in a chip-scale platform. This chapter will focus on integrating the tri-coil wireless power link with a CMOS IC. The load coil and rectifier designs mentioned in the previous two chapters will be adjusted in order to account for the CMOS fabrication process. There are several nuanced details involved in the CMOS IC design procedure, so first a comprehensive overview of the design environment will be presented.

4.1 Design Environment

The computer-aided design (CAD) software used for this project was the Cadence Virtuoso Platform (version ICADV12.2 -64b 09/27/2016), an Electronic Design Automation (EDA) tool used for analog, mixed-signal, and RFIC design. Schematic simulations were done in Cadence Spectre, which is capable of performing transient, harmonic balance, and LSSP simulations, all of which were used to validate the circuit designs. The circuit layouts were constructed using Cadence Layout XL, which maps the conceptual schematic designs to the physical metal layers that make up the IC.

The physical verification software used for this project was the Mentor Graphics/Calibre suite (version v2016.3_36.23), which was used to perform Design Rule Checks (DRCs), Layout-versus-Schematic (LVS) checks, and Parasitic EXtraction (PEX) simulations. It is required to pass these physical verification checks in order for a CMOS foundry to accept the designs for fabrication. The design submission process involved purchasing space on a multi-project wafer that was facilitated by MOSIS (Metal Oxide Semiconductor Implementation Service). The design kit used for the project was the TSMC 65nm Low-Power Mixed-Signal process design kit (pdk). There were nine metal layers used for this project (designated by M1 thru M9), where the uppermost metal layer (M9) was used for the inductor.

4.2 Adjusted Circuit Topologies

As mentioned in the previous chapter, Schottky diodes are preferred for wireless power transfer applications due to their low turn-on voltage and fast switching time. Since the pdk used for this project does not support Schottky junctions, a diode-connected transistor must be used for the

rectifying element, which is shown in Fig. 4.1. As can be observed from the figure, the diode-connected transistor can be comprised of an N-type or P-type MOSFET.

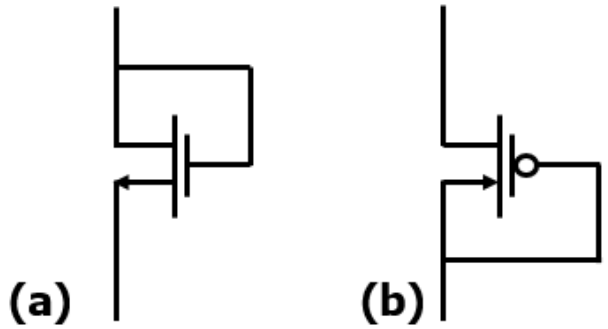

Figure 4.1 Diode-connected transistors for (a) NMOS devices and (b) PMOS devices

There are a few benefits to using transistor-based diodes for the on-chip rectifier. The transistors can be sized flexibly, so the diodes can be custom-designed for a particular application. They can also be designed to take up minimal area in the physical layout, which is important for chip-scale applications. One major downside of diode-connected transistors is their high turn-on voltage, and even when low voltage threshold (V_{th}) devices are used, they cannot outperform their Schottky equivalents.

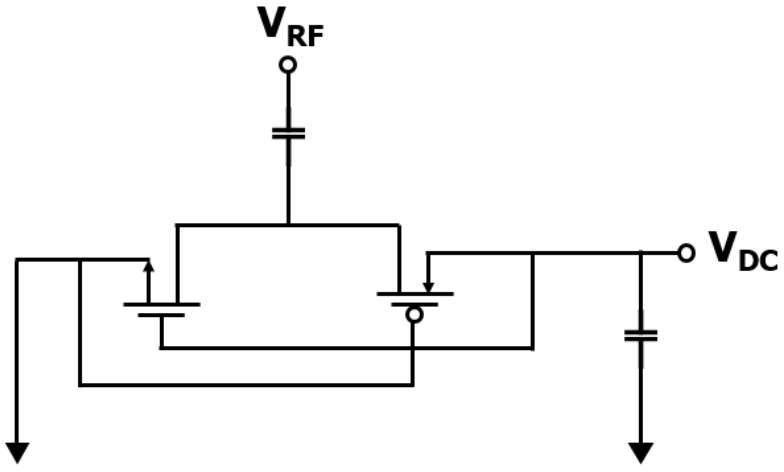

Figure 4.2 Self-V_{th} cancellation scheme for rectifier applications

Recently, it has been increasingly popular to use a topological approach to reduce the voltage threshold of these devices for low-power rectifying applications [24]–[26]. An example of this type of scheme is shown in Fig. 4.2, which shows a self-V_{th}-cancellation technique to bias the

gates of the transistors. As can be seen from the figure, the NMOS device is biased from the output DC voltage, whereas the PMOS device is biased from the circuit ground. This technique not only reduces the effective V_{th} of the transistors, but also reduces the reverse leakage current of the circuit by applying a stronger reverse-bias to the device that is supposed to be off. This improves the rectification efficiency of the circuit compared to when conventional diode-connected transistors are used.

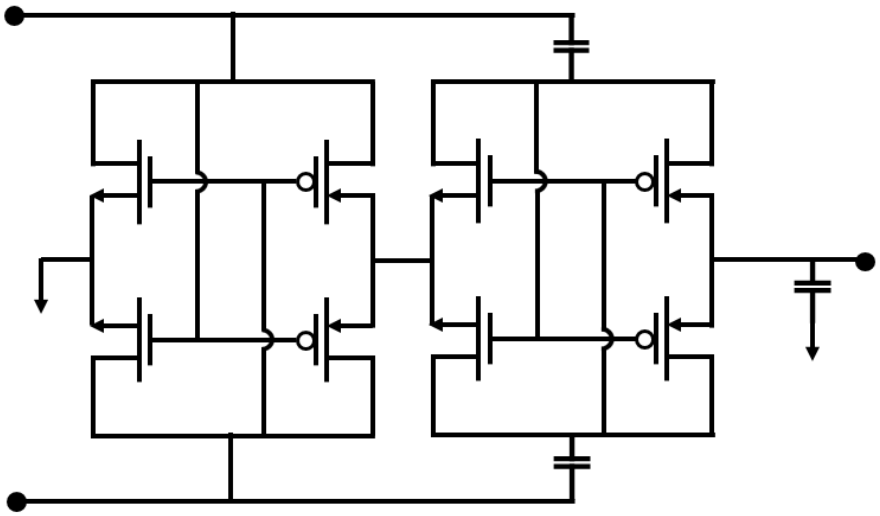

Figure 4.3 Full-wave Dickson-based rectifier schematic using cross-coupled transistors

This self-biasing concept is employed in the rectifier circuit shown in Fig. 4.3, which is commonly used in passive RFID applications [12], [24], [25], [27]. The circuit consists of a two-stage Dickson rectifier, much like the one discussed in the previous chapter, but with some modifications to account for the IC environment. A differential version of the Dickson multiplier is used for two reasons. First, this circuit is capable of rectifying lower incident power levels than its single-ended version since it can conduct on both the upper and lower halves of the waveform. Second, the differential version of the circuit uses smaller capacitors than its single-ended counterpart to achieve the same output DC level. This means that the rectifier takes up less space on the chip, which can be used for other circuitry. The rectifier uses a cross-coupling structure to achieve the self-cancellation scheme discussed previously.

Coil Designs

In order to interface with a differential rectifier, the load coil design needs to be modified such that it can distribute current evenly across its terminals. This can be done using a symmetric design. The size of the load coil was increased to 200 μm by 200 μm in order to compensate for the low Q of CMOS inductors and to allow enough inner area for the communication circuits. Three load coil designs were investigated, as shown in Fig. 4.4. The designs used different segment widths and spacing to explore their effects on the self-resonant frequency and Q of the coils at the operating frequency. The specific parameters of each design are listed in Table 4.1. The coil properties were extracted using HFSS simulations, an example of which is shown in Fig. 4.5. In addition to the load coil, the HFSS model includes several metal patches directly underneath the coil segments that model the dummy metal that needs to be placed underneath the inductor to satisfy the metal density requirements for the CMOS foundry. Also shown in the figure is a large metal sheet in the center of the coil that models the metal layers comprising the communication circuits and inner metal fill. The effects of these metal parasitics can lower the self-resonant frequency of the inductor by as much as ~ 500 – 600 MHz and can cut the Q down by half.

Table 4.1 Properties of Load Coil Designs

Design #	# of Turns	Width	Spacing	Q	SRF (GHz)
1	5	9 μm	3.5 μm	5.7	7.5
2	5	5 μm	6 μm	8.78	7.9
3	3	5 μm	2.5 μm	6.17	8

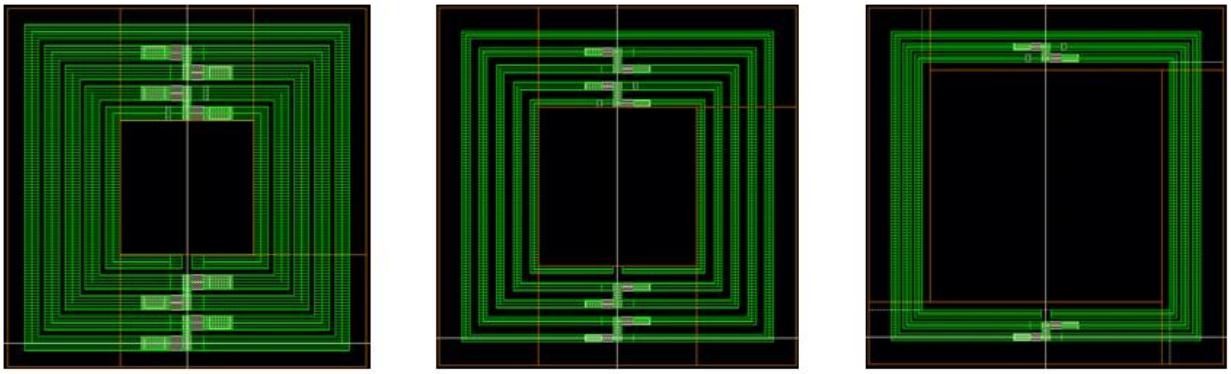

Figure 4.4 Three symmetric load coil designs in Cadence layout

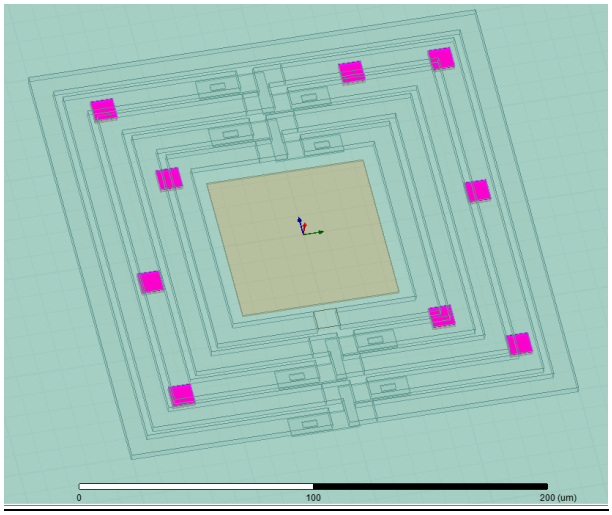

Figure 4.5 HFSS model for a 200 μm x 200 μm load coil

Rectifier Designs

The schematic of the differential rectifier is shown in Fig. 4.6. If the on-chip circuit draws 100 μW of power and requires 1 V of DC input, the output load of the rectifier can be modeled as a 10 kΩ resistor. The transistors can consist of standard N-channel or P-channel low-V_{th} MOSFETs, or RF low-V_{th} MOSFETs. The RF transistors take up more space, but they have fewer discrepancies between the pre-layout and post-layout simulations and better reliability at high frequencies compared to the non-RF devices.

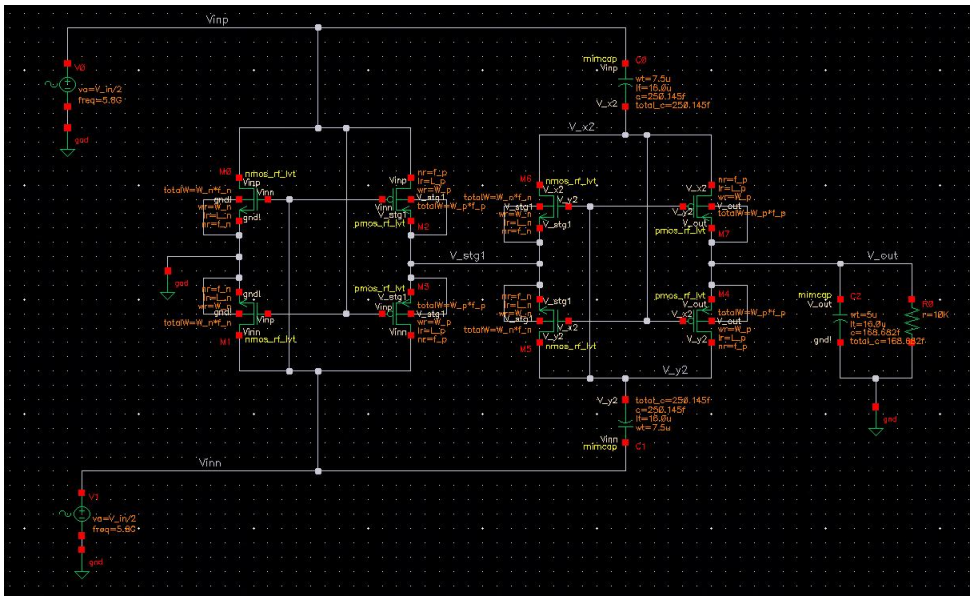

Figure 4.6 Cadence schematic of the two-stage differential rectifier circuit

There are two types of capacitors that can be used in this pdk: metal-insulator-metal (MIM) capacitors and metal-oxide-metal (MOM) capacitors. An example of each type is shown in Fig. 4.7. The standard MIM capacitors are more bulky in terms of area-per-capacitance in comparison to MOM capacitors, and their terminals are located on M8, meaning that circuits using metal layers lower in the stack need several vias in order to route to the capacitors. Some advantages of using MIM capacitors are that they have good reliability at high frequencies and that circuits can be placed underneath them in order to save area. The MOM cap design shown in Fig. 4.7 uses interdigitated fingers consisting of metal layers M1 thru M7 and achieves a high capacitive density per area, but no circuits can be placed underneath them.

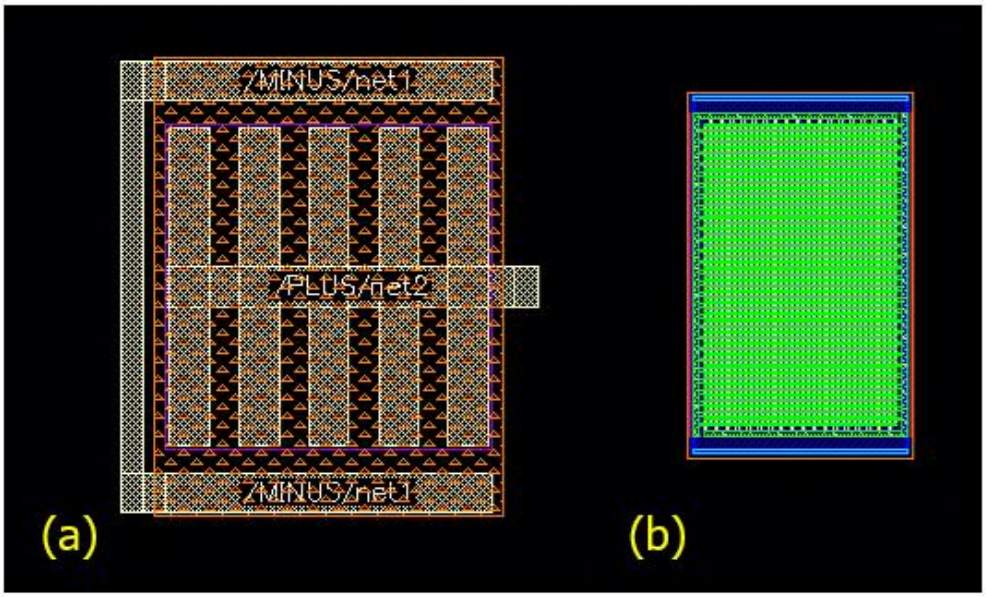

Figure 4.7 300 fF capacitors implemented as an (a) MIM capacitor and a (b) MOM capacitor

Figure 4.8 shows two rectifier designs: one that uses MIM capacitors and RF transistors and one that uses MOM capacitors and non-RF devices. Both circuits occupy a physical area of about 32 μm x 21 μm. A 1 V peak-to-peak differential excitation was used as the input for both circuits, and the post-layout simulation results are shown in Fig. 4.9. Since the MOM capacitors and non-RF transistor version of the rectifier had better performance, it was selected to form the base for the rest of the communication circuits.

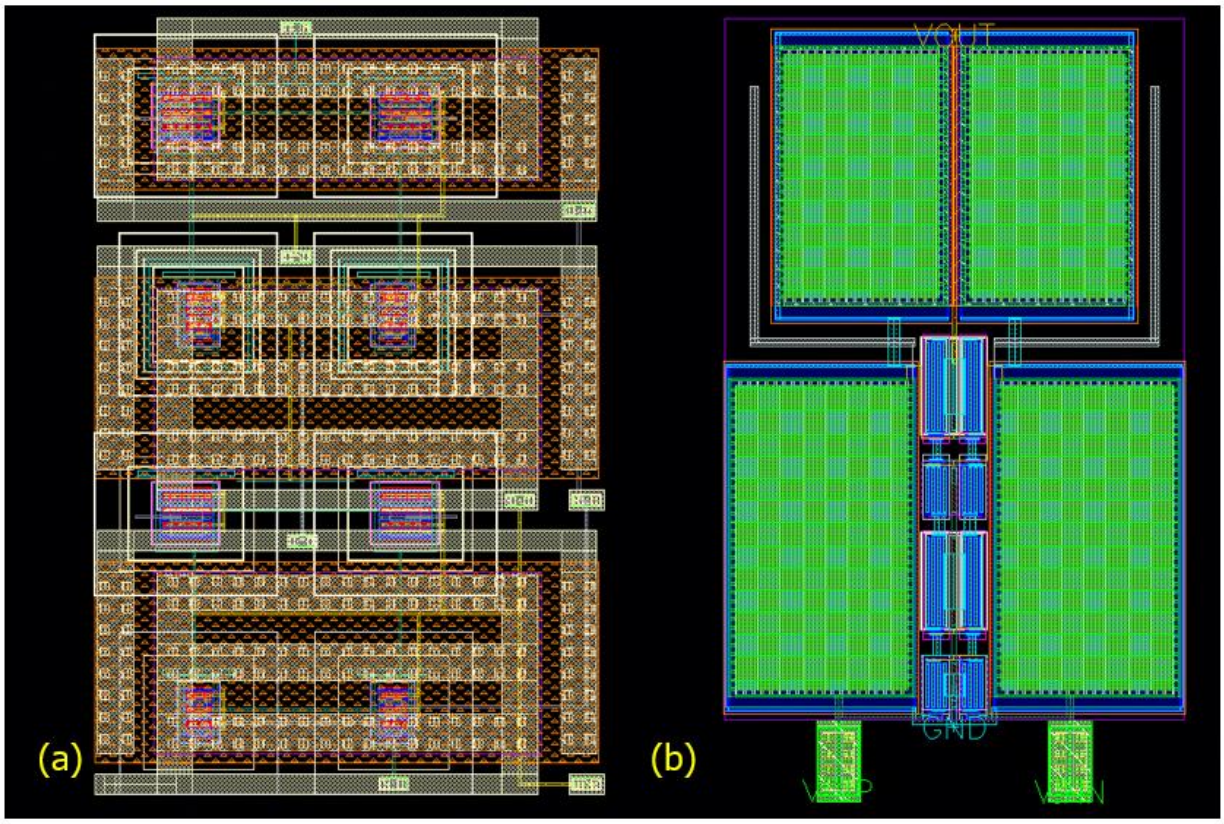

Figure 4.8 Rectifier layouts using (a) MIM capacitors and RF transistors and (b) MOM capacitors and non-RF transistors

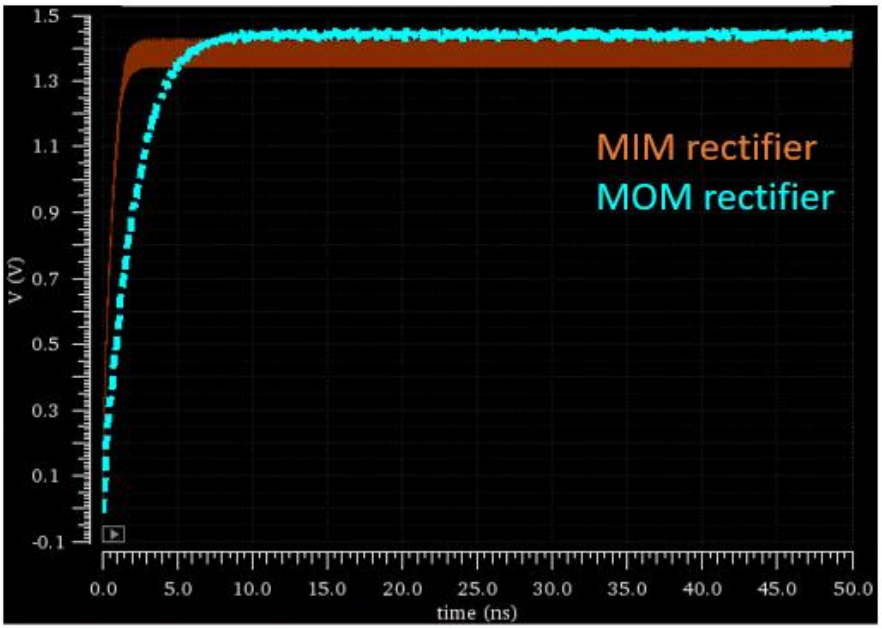

Figure 4.9 Post-layout simulation comparison between MIM-based rectifier (orange) and MOM-based rectifier (blue)

A harmonic balance simulation was performed to extract the input impedance of this rectifier at 5.7 GHz, the desired operating frequency of the link. Figure 4.10 shows the input impedance of the rectifier as a function of input power in dBm. The input impedance of the rectifier was determined to be 58.5 – j564 Ω for an input power of 0 dBm. The RF-DC conversion efficiency of the rectifier at this frequency was around 11%.

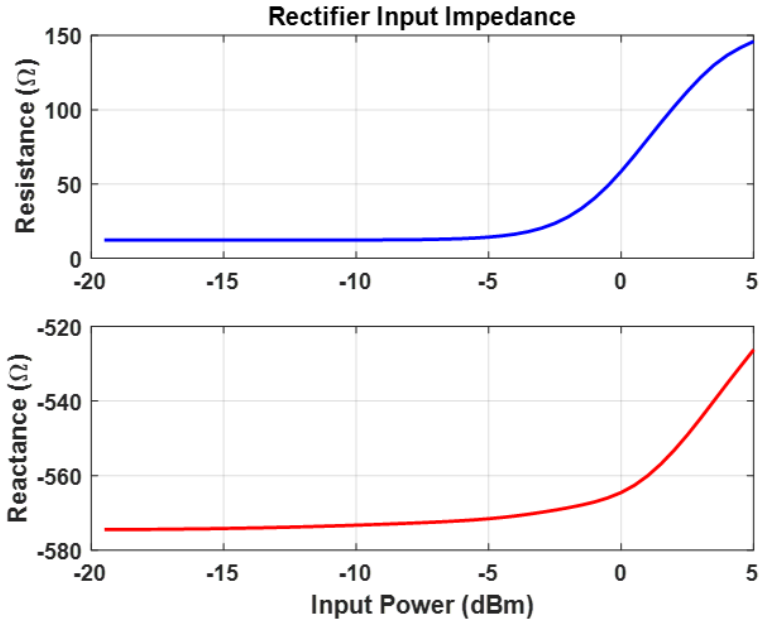

Figure 4.10 Rectifier input impedance as a function of input power at 5.7 GHz

4.3 Link Budget

Now that the on-chip inductor and rectifier have been designed and characterized, the forward link budget for the RF to DC power transfer from the near-field reader coil to the on-chip load can be calculated. A diagram illustrating the boundaries of the forward link budget is shown in Fig. 4.11, which accounts for the tri-coil power transfer efficiency, the effects of misalignment and vertical separation, the mismatch loss between the load coil and the rectifier, and the RF-DC conversion efficiency of the rectifier. The mismatch loss is the logarithmic equivalent of the mismatch factor, which characterizes the impedance mismatch between the load coil and the rectifier. The mismatch factor is calculated using the following equation:

$$Mismatch\ Factor = \frac{4R_C R_R}{|Z_C + Z_R|^2} \tag{4.1}$$

where R_C and R_R are the input resistances of the load coil and rectifier, respectively, and Z_C and Z_R are the input impedances of the load coil and rectifier, respectively. The calculated mismatch loss between the first coil design and the rectifier was evaluated to be around 3 dB. A conservative estimate was used for the misalignment effects on the peak RF-RF efficiency (denoted by PRFE in the figure) based on the previous measurement results using a 100 µm by 100 µm load coil. Under these conditions, at least 50 µW of DC power is still delivered to the IC load.

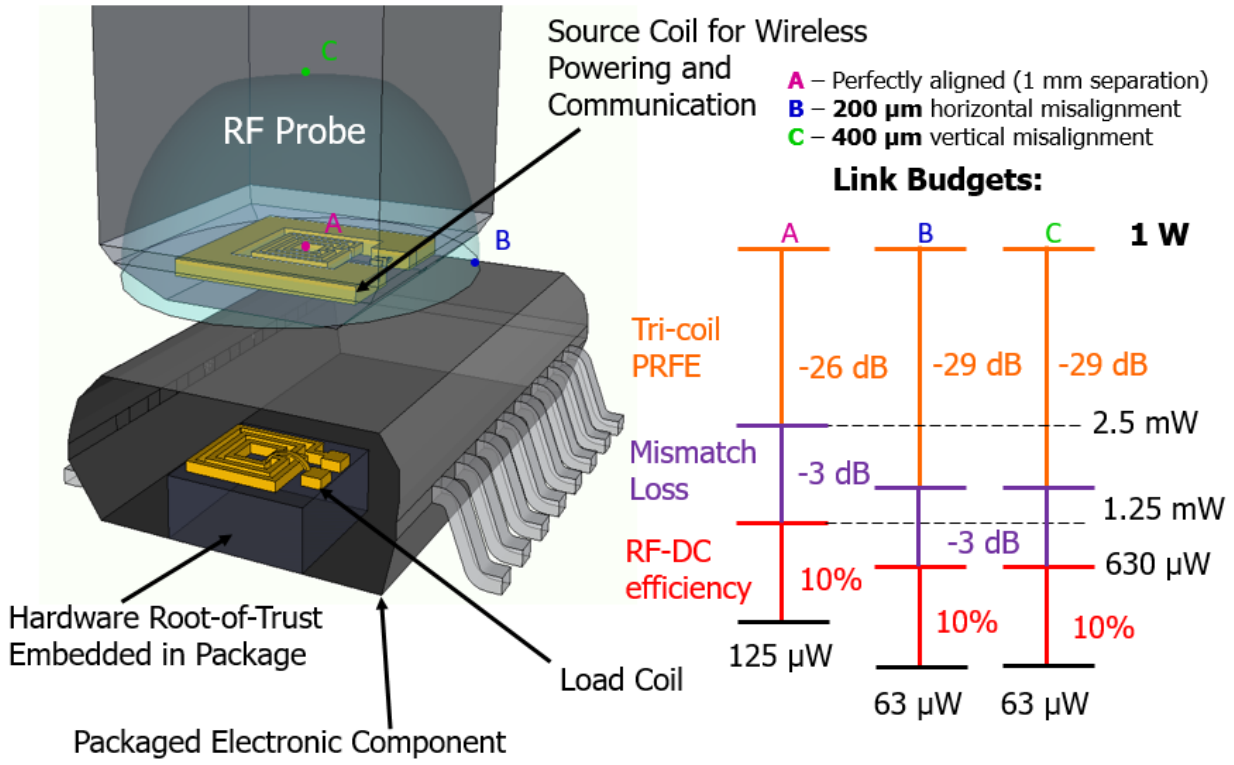

Figure 4.11 Forward link budget for the full RF-DC efficiency of the tri-coil system at 5.7 GHz using a 200 µm by 200 µm load coil

4.4 Communication Circuits

The rectifier design discussed in the previous sections can be modified to perform basic communication functions, such as demodulation or backscattering. The techniques for performing backscattering communication will be discussed first.

Backscattering Circuits

As discussed previously, backscattering is a method of communication that involves modulating the load impedance of an RFID tag such that it creates a perturbation in the waveform that can be detected by the RFID reader. The schematic for employing a rudimentary backscattering scheme is shown in Fig. 4.12. At the differential input, two MIM capacitors of roughly 300 fF each were placed with shunt paths to ground by means of two RF transistors operating as switches. When the switches are "OFF," the shunt path to ground is disconnected, and the input impedance is largely determined by the differential rectifier itself. When the switches turn "ON," the input is loaded with the two MIM capacitors, which changes the overall input impedance of the circuit. From harmonic balance and large-signal S-parameter simulations, the input impedance was determined to be 38 – j456 Ω when the switches were "OFF," and 19 – j139 Ω when the switches were "ON" for an operating frequency of 5.8 GHz.

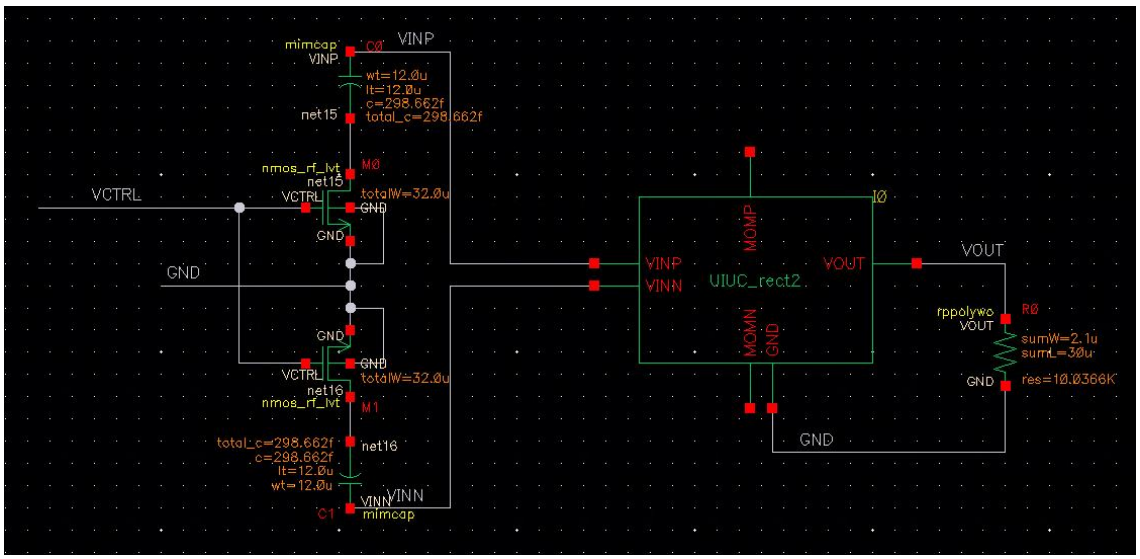

Figure 4.12 Cadence schematic for the backscattering circuit

The layout for the combined differential rectifier, resistive load, MIM capacitors, and switches is shown in Fig. 4.13. Symmetry and RF devices were utilized to avoid large discrepancies between the pre-layout and post-layout simulations. The control signal that determines the switch states was routed to an external pad. In the final implementation, the control signal would be provided by the on-chip IC using sub-carrier modulation.

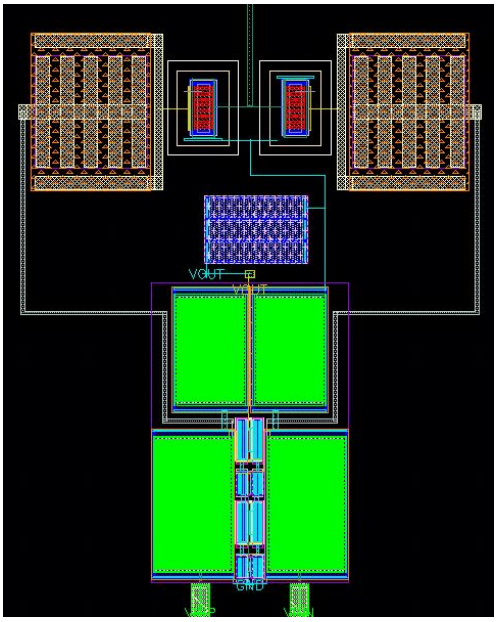

Figure 4.13 Cadence layout for the backscattering circuit

The quality of the backscattered signal is characterized by its modulation depth, which describes how much the modulated signal impressed on the carrier frequency varies around its unmodulated level. A higher modulation depth means that it will be easier for the receiver to distinguish between the two different states in the logic waveform. Various switched capacitance values can be used to alter the modulation depth of the signal perceived at the receiver of the near-field reader, but there is a tradeoff between the modulation depth and the power delivered to the on-chip load. This tradeoff is investigated using an elaborate simulation procedure, which is described below.

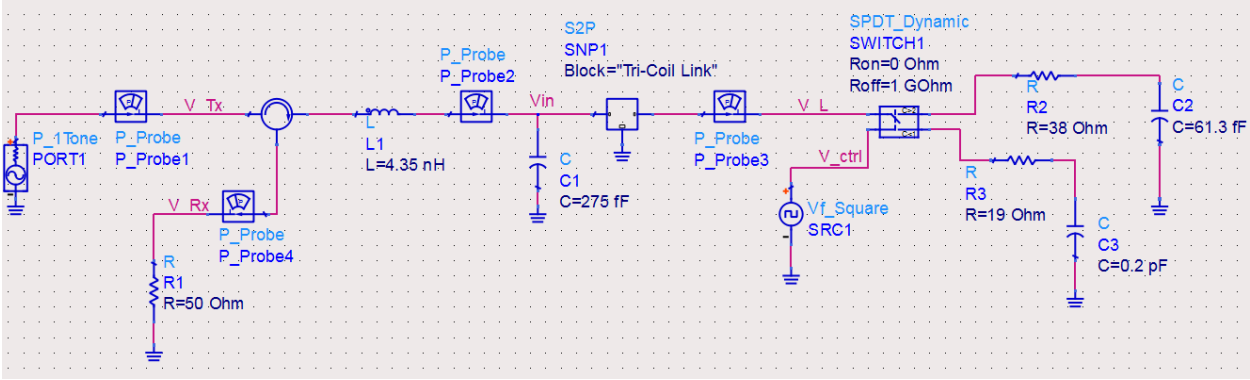

Figure 4.14 ADS schematic for the backscattering simulation including the tri-coil S-parameter block, reader matching network, and lumped element models for the rectifier impedances when the switch is "OFF" and "ON"

Backscattering link simulation procedure:

1. Design a load coil with a high enough Q and self-resonant frequency for the intended frequency for the application. In this work, three 200 µm x 200 µm coil designs were used with an intended operating frequency of 5.8 GHz.
2. Simulate the load coil with the tri-coil link in HFSS and extract the resulting two-port S-parameters.
3. Instantiate the tri-coil S-parameters in ADS (see Fig. 4.14) and design a matching network for the link on the reader side. There are space limitations for an on-chip matching network, but there are no such limitations on the reader side. The matching network is critical for improving the modulation depth perceived at the reader receiver since the perturbations in the signal due to the on-chip modulations are typically very small.
4. Extract the backscattering circuit input impedances when the switch is OFF or ON in Cadence Virtuoso using harmonic balance simulations. A wide range of switched capacitance values should be investigated in order to determine a trend between modulation depth and power delivered to the IC load.
5. Model these extracted impedances using lumped components in ADS and use a single-pole-double-throw (SPDT) switch, and perform transient simulations to obtain the backscattered modulation depth (an example is shown in Fig. 4.15).
6. Determine the amount of power delivered to the IC load when the switch is "ON" and "OFF" by running transient simulations in Cadence Virtuoso (see Fig. 4.16). The "ON" state is typically the limiting case for delivering sufficient power to the IC load.

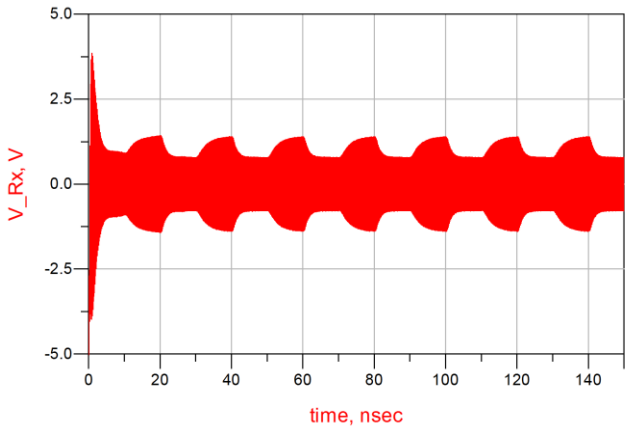

Figure 4.15 ADS simulation results for the backscattered signal measured at the reader receiver

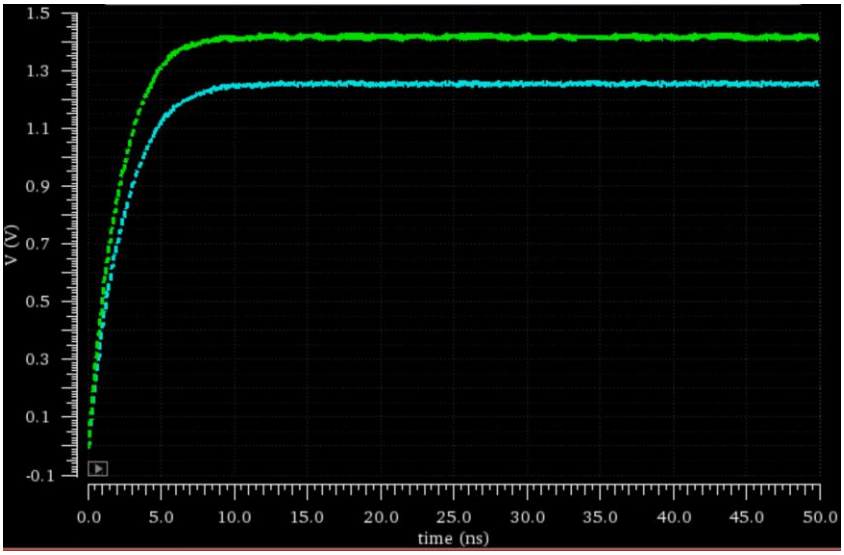

Figure 4.16 Cadence transient simulation results for the backscattering circuit when the switch is "OFF" (green) and "ON" (blue) for an input power of 0 dBm

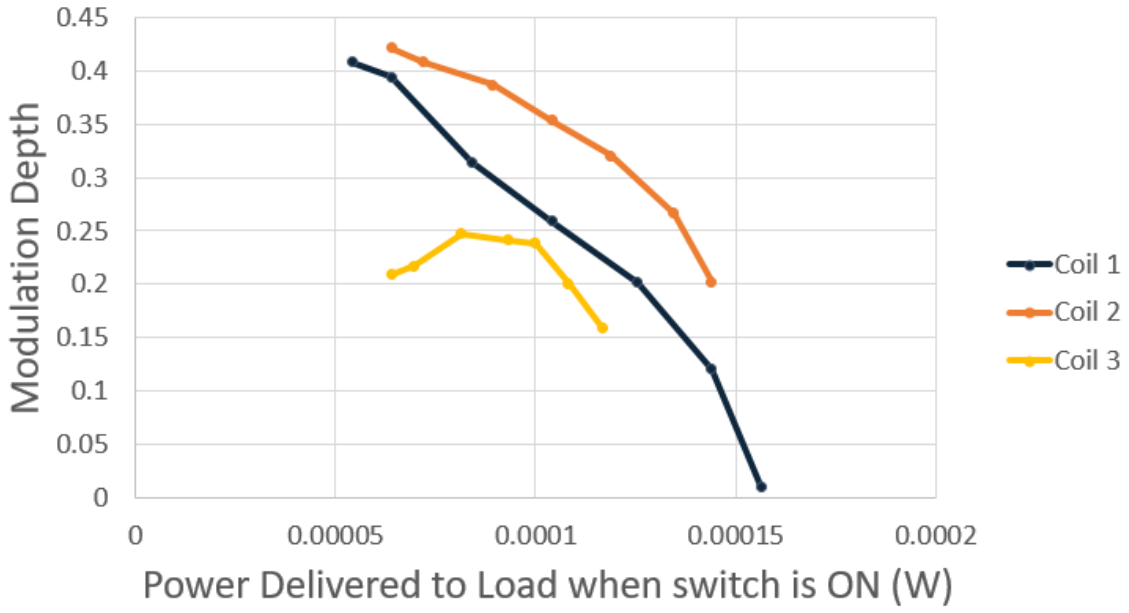

Figure 4.17 Modulation depth vs. power delivered to the IC load when the switch is "ON" for three different load coil designs

The tradeoff between modulation depth perceived at the reader and power delivered to the IC load is illustrated in Fig. 4.17. In general, the more power delivered to the load, the smaller the modulation depth. The curves depend on the simulated incident power level used at the input to the rectifier (0 dBm was used to generate this graph). A higher incident power level (which can be

obtained by increasing the reader output power or improving the wireless power transfer efficiency of the link) would result in shifting the curves to the right.

Demodulation Circuit

In order for the rectifier to support simultaneous RF-DC conversion and envelope detection, the same power-splitting technique in the previous chapter was employed but for a differential topology. The layout for the differential rectifier and envelope detector circuit is shown in Fig. 4.18. The large set of capacitors that comprise the upper part of the circuit are necessary to smooth out the fluctuations due to the downlink modulation. The differential topology is a necessary feature at this point since a single-ended version of this circuit would require much larger capacitors to achieve the same performance. As can be seen in the figure, an additional resistor was used at the output of the first stage to perform the envelope detection. The parasitic capacitance at this node is sufficient to complete the RC load for the envelope detector.

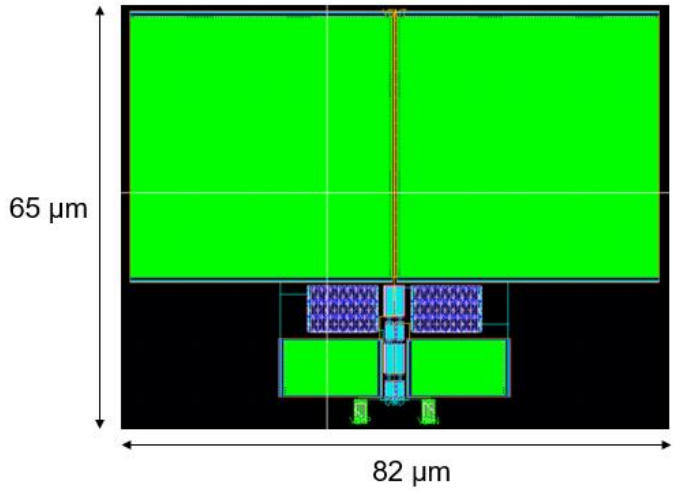

Figure 4.18 Cadence layout for the differential rectifier and envelope detection circuit

Bi-directional Circuit

The demodulation circuit discussed previously can be converted into a bi-directional circuit by simply adding switched MIM capacitors at the input to the rectifier. The layout for this circuit is shown in Fig. 4.19. As can be seen in the layout, the MIM capacitors can be placed below the load capacitors in a way that does not increase the overall footprint of the device. When this is integrated with the load coil, the device can perform wireless bi-directional communication, meaning that it

can demodulate a message signal from the near-field reader and send back a response using backscattering.

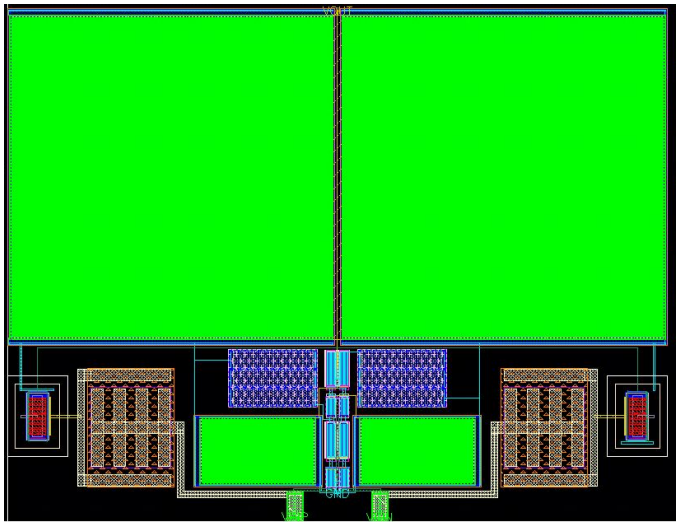

Figure 4.19 Cadence layout for the bi-directional communication circuit

4.5 Test Chip

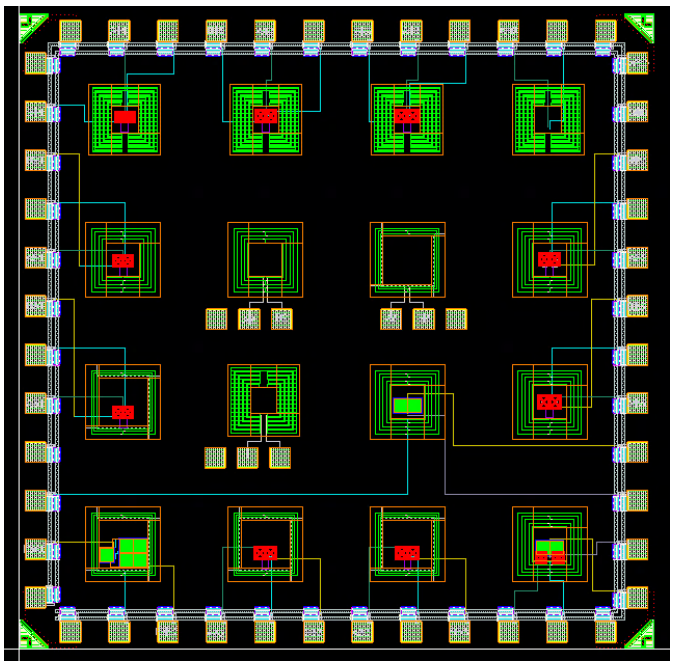

Figure 4.20 Test chip layout for various load coils, backscattering, and demodulation circuit designs

As mentioned previously, in order to fabricate these devices, space needs to be allocated on a multi-project wafer (MPW) and every circuit to be fabricated needs to be arranged within that

space. TSMC provides TinyChip runs, where universities can purchase a 1960 μm by 1960 μm area for research projects. The foundry provides a seal-ring that encloses this area, around which are dicing streets that a third-party vendor uses to release the test chip from the MPW. The customers are required to make their own pads and electro-static discharge (ESD) protection circuits to include in their design. The test chip layout for this project is shown in Fig. 4.20. The test chip includes forty-eight 65 μm by 65 μm custom-designed pads with a pitch spacing of 150 μm. There are 16 test circuits on the chip, including:

1. The three coil designs integrated with three different backscattering circuit designs (9 circuits total)
2. One backscattering test circuit (a coil loaded with a switch that changes from an open-circuit to a short-circuit)
3. Three standalone inductors (to verify the Q and self-resonant frequency of each design)
4. Two demodulation circuits integrated with a load coil (one is a single-ended circuit design, the other is the differential circuit design)
5. One differential bi-directional circuit design

There are large gaps between the coils on the test chip, which primarily serve as available area for dummy metal fill. The inductors are so large that it is hard to meet the metal density requirements for the CMOS foundry since it is undesirable to have metal fill directly underneath the coil segments, as this decreases the Q and self-resonant frequency of the coils. When the large gaps are used for metal fill, this helps satisfy the metal density DRCs.

Chapter 5: Conclusion

5.1 Findings of this Work

This work has covered design strategies and techniques for near-field simultaneous wireless power transfer and communication to chip scale devices. A tri-coil link has been demonstrated to wirelessly deliver power to a device on the order of 100s of μm over a distance that is ten times the smallest coil diameter. The design was experimentally validated using a customized testbed that was used to characterize the RF-RF power transfer efficiency of the link. Design techniques were introduced for a system to support simultaneous wireless power transfer and communication using a modified Dickson rectifier. The measurement testbed was modified in order to experimentally validate the simultaneous power and communication link using a prototype PCB rectifier. Finally, the designs were incorporated in an IC environment and backscattering and bi-directional communication circuits were explored. The work presented in this thesis can be used to design a hardware root-of-trust for electronic supply chain security applications.

5.2 Future Work

There are several avenues of future research to increase the performance of a system that supports simultaneous wireless power transfer and communication to chip-scale devices. A few of them will be discussed here.

IC Power Management Unit

As mentioned in Chapter 3, one way to perform RF-DC conversion as well as AM demodulation is to have a separate power management unit regulate the output of the rectifier, and the ripple in the rectifier output can be used as the logic input to the chip. The power management unit could consist of a charge pump, a low drop-out regulator, or a combination of both depending on the voltage supply requirements of the IC. The power management unit would also ensure a stable DC voltage supply to the circuit even when the input power to the rectifier changes (e.g. if the root-of-trust is moved closer to the near-field reader or more power is transmitted by the reader coil).

Fully Integrated On-Chip Solution

In Chapter 4, an external pad was used to send a control signal to the on-chip switch that facilitated the backscattered modulation. In the actual deployment of a hardware root-of-trust, the modulation control signal would need to be provided internally by the IC by means of subcarrier modulation. Designing an IC that does not require input from any external pads is a crucial component for the completion of the hardware root-of-trust for its intended application.

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