

THIN-FILM GaN HEMTs FOR FLEXIBLE ELECTRONICS

By

Josh Perozek

Senior Thesis in Electrical Engineering

University of Illinois at Urbana-Champaign

Advisor: Professor Can Bayram

May 2017

Abstract

As the demand for faster, more efficient, and more robust electronics continues to grow, new materials beyond silicon need to be explored. In the field of power electronics, gallium nitride (GaN) is a strong candidate for next-generation devices due to its wide bandgap (3.4 eV), high electron mobility ($>1500 \text{ cm}^2/\text{V}\cdot\text{s}$), and large electron sheet concentration (10^{13} cm^{-2}). These properties enable high performance devices that are mechanically and electrically stable in harsh conditions such as high temperatures or extreme bending. Due to the prohibitive cost of free-standing GaN, GaN wafers are typically created through epitaxial growth on sapphire, silicon carbide, or Si (111) substrates; through substrate removal processes, the $<5 \text{ }\mu\text{m}$ thick GaN layers enable new thin-film technologies such as flexible electronics. In this project, we develop a wet etching based low-cost substrate removal process for GaN on Si (111) and characterize the structural and electrical properties of the material before and after substrate removal as well as at various bending conditions.

Subject Keywords: GaN; high electron mobility transistors; flexible electronics

Acknowledgments

To begin, I must express my sincerest gratitude to my advisor, Professor Can Bayram, who had the willingness to welcome a naïve sophomore into his research group and offer nothing but patience, support, and helpful criticism over the last two and a half years. Of all my experiences at the University of Illinois, his guidance has been by far the most influential and valuable. The ever-increasing responsibilities he allowed me to take on and the freedom he has afforded me throughout my time here has shaped me into the scientist I am today.

I also would like to thank all the members of Professor Bayram's ICORLAB, particularly, Hsuan-Ping Lee, Richard "Dicky" Liu, and Kihoon "Grand-dad" Park for all their teaching, support, and advice, as well as for putting up with my distractions over the last year. I must also acknowledge and thank Ryan Grady for going through the senior thesis and graduate school admissions process with me and for reminding me of deadlines as well as the periodic morale boosts (generally in the form of bad physics jokes). I could not have asked for a better group of people to work with and call my friends.

Additionally, this work would not have been possible without the support of the technical staff at the Micro and Nanotechnology Laboratory (MNTL), Micro-Nano-Mechanical Systems (MNMS) Laboratory, and Materials Research laboratory (MRL) at the University of Illinois. I must particularly thank Edmund Chow and Joe Maduzia for the various trainings and process support over the years.

This work was supported in part by the Air Force Office of Scientific Research (AFOSR) through Young Investigator Program Grant FA9550-16-1-0224 and the Undergraduate Independent Study Funds of Electrical and Computer Engineering Department, University of Illinois at Urbana-Champaign, IL, USA.

Contents

| | |
|--|----|
| 1. Introduction | 1 |
| 1.1 GaN HEMTs | 2 |
| 1.2 Flexible Electronics..... | 4 |
| 2. Literature Review | 5 |
| 3. Preliminary Tests and Characterization | 7 |
| 3.1 SEM Structural Analysis | 8 |
| 3.2 AFM Defect Density Calculations..... | 8 |
| 3.3 XRD Strain Determination..... | 10 |
| 3.4 Hall Measurement Electrical Characterization | 11 |
| 4. Substrate Removal Process and Results | 13 |
| 5. Conclusion..... | 21 |
| Appendix A: Processes and Results..... | 22 |
| Appendix B: Characterization and Methods..... | 36 |
| B.1 Hall Measurements..... | 36 |
| B.2 AFM Defect Counting..... | 38 |
| References | 40 |

1. Introduction

Since the 1960s, the silicon-based transistor has been the core component of all modern electronics [1]. Decade by decade, as the need for smaller, faster, more robust, and more efficient transistors grew, industry continuously kept up with the demand through countless innovations such as the metal-oxide-semiconductor field effect transistor (MOSFET), insulated gate bipolar transistors IGBT, strained silicon-germanium alloys [2], high k gate dielectrics, etc. However, as we continue to advance our solid-state technology, we are pushing the theoretical limits of silicon-based devices. This has forced researchers to seek alternate materials with properties that allow them to achieve higher performance in specific areas.

One major area that can benefit from alternate materials is robust and high power electronics. Table 1 lists several common semiconductors and some key properties for their performance in different areas [3]. For robust and high power applications, a parameter of particular interest is the material's bandgap, which is directly related to the critical electric field. Since the bandgap quantizes how tightly electrons are held to the material lattice, a high bandgap is desired for high power applications where electric fields become large enough to provide sufficient energy to electrons to break the bonds of the material. Moreover, with tightly bound electrons from a high bandgap, a semiconductor device can withstand higher temperatures and radiation from extreme environments because excess carriers will not be generated by the environment. From Table 1, it is apparent that gallium nitride (GaN) is an excellent choice for high power and robust electronics due to its wide bandgap and critical electric field. A second feature of GaN that differentiates it from other wide bandgap semiconductors like silicon carbide (SiC) is its ability to utilize a high electron mobility (HEMT) structure that allows it to perform well in higher frequency applications such as radar and communication systems.

Table 1. Material Properties of Several Semiconductors

| MATERIAL | BANDGAP (eV) | CRITICAL ELECTRIC FIELD (10^6 V/cm) | ELECTRON MOBILITY ($\text{cm}^2/\text{V-s}$) | THERMAL CONDUCTIVITY (W/cm-K) |
|----------|--------------|--|--|-------------------------------|
| Si | 1.12 | 0.3 | 1,400 | 1.5 |
| GaAs | 1.43 | 0.4 | 8,500 (2DEG) | 0.46 |
| 4H-SiC | 3.26 | 3 | 1,000 | 4.9 |
| GaN | 3.45 | 5 | 2,000 (2DEG) | 1.3 |

1.1 GaN HEMTs

Over the last decade, GaN high electron mobility transistors (HEMTs) have been a promising candidate for next-generation electronics where it enables faster, smaller, and more efficient transistors than current silicon-based technologies. Thanks to the wide bandgap of 3.4 eV, large critical electric field (~ 3 MV/cm), and high electron saturation velocity (2.7×10^7 cm/s), GaN is particularly well suited for high power and high frequency applications such as high power radar systems, electric vehicle power supplies/inverters, and high speed wireless communication systems [4].

An important property of GaN is its ability to form a two-dimensional electron gas (2DEG) when AlGaIn is grown on top of a GaN surface. This 2DEG is a highly mobile and dense sheet of electrons that forms the basis of the HEMT and is a result of the spontaneous and piezoelectric polarization differences present at an AlGaIn/GaN interface. This method of 2DEG formation differs from that of the GaAs-based HEMT in that the GaN HEMT does not require doping. Since the electronegativity differences between the Ga and N atoms is large, they tend to align in their lattice and form a wurtzite crystal structure while GaAs, which has lower electronegativity differences, forms the close-packed Zinc-Blende structure as shown in Figure 1 [5]. Due to the alignment of the Ga and N atoms in GaN, they create a spontaneous polarization field. By further straining the crystal, we can introduce piezoelectric polarization as well that further enhances the 2DEG. Figure 2 shows the formation of the 2DEG in a triangular quantum well due to the conduction band offsets and polarizations.

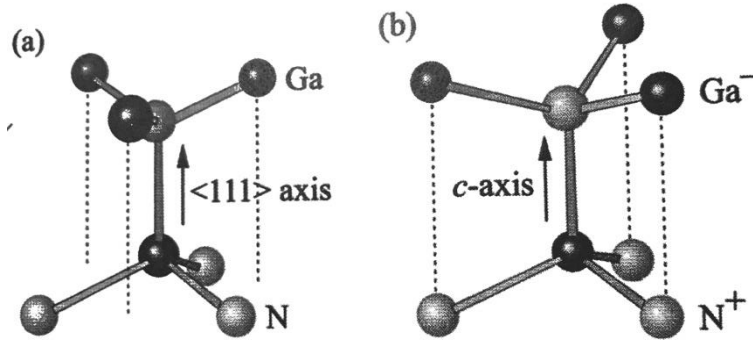


Figure 1. (a) Zinc-Blende structure of GaN (b) Zinc-Blende of GaN

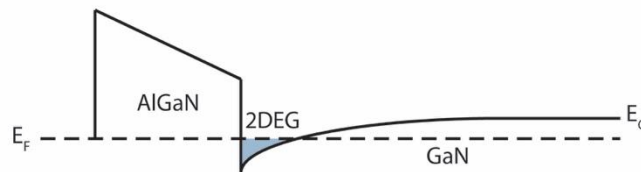


Figure 2. 2DEG formation at AlGaN/GaN interface

Since the 2DEG is the main conductive channel the HEMT, its electrical properties are of major importance to the transistor's performance [6]–[9]. In addition to increased scattering, threading dislocations can act as deep traps within the bandgap, which can lead to detrimental effects in a HEMT such as current collapse or virtual gating [10]. Thus, it is very important that high quality GaN is used for high performance devices. Traditionally, GaN has been grown on Al₂O₃ or SiC where the lattice constant and coefficient of thermal expansion are relatively closely matched [11]. However, when trying to scale GaN to larger wafer diameters to reduce cost, this causes problems because of the limited availability and high cost of Al₂O₃ or SiC growth substrates. To circumvent this issue, several groups have grown GaN on large Si(111) substrates where various buffer layers are used to produce high quality wafers (defect density <10⁹ cm⁻²) despite poor lattice matching [6], [7], [12]–[18]. Using Si provides a large cost improvement, but also enables another interesting application: substrate removal.

Because free-standing GaN is only available in extremely limited quantities, by using Si as a growth substrate, we can easily remove the silicon and be left with the thin GaN layer grown on top. Typically, for high power devices, buffer breakdown is one of the first failure mechanisms. This is where a device that is in the off-mode conducts through the substrate instead of the 2DEG channel resulting in a conducting transistor instead of one that is cut off. By removing the substrate, this breakdown mode can be suppressed and the overall voltage blocking capabilities of the transistor are improved.

1.2 Flexible Electronics

As technology continues to progress, the desire for flexible electronics to enable exciting new technologies such as wearable electronics, minimally invasive bio-sensors, or more robust and lightweight solar cells continues to grow [19].

While several methods for flexible electronics are discussed in Chapter 2, an interesting application of the previously mentioned substrate removal process for GaN HEMTs is that it allows for high performance bendable devices. When mounted on flexible substrates such as a plastic, devices on very thin GaN films ($<5 \mu\text{m}$) can be bent without breaking. While flexible circuits have been produced using organic materials, their poor performance makes the use of thin film semiconductors highly desirable.

2. Literature Review

As mentioned in Chapter 1, several methods of creating flexible electronics have already been attempted. For example, Sekitani et al. have demonstrated organic semiconductor devices capable of stable bending with a radius of curvature as low as several millimeters [20]. However, as is typical of these organic semiconductors, mobilities in these devices are as low as $0.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Other thin-film transistors (TFTs) have been made using metal oxides [21] or amorphous silicon [22], with the highest mobility on the order of $\sim 10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ coming from polycrystalline silicon [23]. Besides the low mobility, these TFTs are also often plagued with high operating voltages ($>20 \text{ V}$) making them impractical for wearable applications. An alternative to these materials is GaN, which has an electron mobility greater than $1500 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and is mostly transparent for discrete bio-applications.

While GaN is promising material, some considerations need to be addressed. One problem that has only been minimally studied is the effect of bending on device performance. For nearly all types of semiconductor (organic, metal oxide, or typical semiconductor), the mobility has been experimentally shown to vary linearly with bending radius, R , according to [24]:

$$\frac{\mu(R)}{\mu_0} = 1 + m\epsilon \quad (2.1)$$

where $\mu(R)$ and μ_0 are the mobility during bending and flat conditions respectively, ϵ is the strain, and m is an experimentally determined constant. However, since the 2DEG properties of a HEMT depend on the piezoelectric polarization of the AlGaIn and GaN materials, it is reasonable to expect that bending will further effect their electrical performance by altering the free carrier concentrations of the electron gas.

Several thin-film GaN HEMTs made through substrate removal have already been studied [25]–[27]. In these studies, it has been concluded that by bending GaN devices, the on-resistance decreases

and the 2DEG sheet concentration rises. Theoretically, this change in sheet concentration, n_s , is determined by [27]:

$$n_s = \frac{\sigma_s}{q} = (P_{sp,GaN} + P_{flex,GaN}) - (P_{sp,AlGaN} + P_{pz,AlGaN} + P_{flex,AlGaN}) \quad (2.2)$$

where σ_s is the sheet charge density at the GaN/AlGaN interface, q is the electron charge, P_{sp} , is the polarization contributions due spontaneous polarization, and P_{flex} , and P_{pz} are the piezoelectric polarization contributions due to external flexing and internal layer stress respectively for GaN and AlGaN. The change due to bending is determined by the values of P_{flex} , which is given by:

$$P_{flex} = \frac{(\sigma_x + \sigma_y) \left(e_{31} - e_{33} \left(\frac{C_{13}}{C_{33}} \right) \right)}{(C_{11} + C_{12}) - \frac{2C_{13}^2}{C_{33}}} \quad (2.3)$$

where σ is the layer strain, e and C are the piezoelectric and elastic coefficient matrix elements for their respective subscripts.

To create their samples, these studies have either employed mechanical lapping followed by a silicon etch, or silicon reactive ion etching (RIE) to gently remove the silicon. As of very recently (after starting this project), a team from France has improved a substrate removal process for transferring GaN thin-films on to flexible tape [2]. They concluded that over-etching in the hydrofluoric/nitric/acetic (HNA) acid etchant solution leads to cracks in the GaN films which destroys device performance. Due to the over-etching, they altered their initial approach of mechanical lapping of the Si down to 100 μm followed by an aggressive wet etch to lapping followed by a gentler reactive ion etch (RIE). Typically, RIE tends to be significantly more expensive than wet etching, so it was avoided in this senior thesis project in favor of finding a more affordable and scalable process.

3. Preliminary Tests and Characterization

To determine the effects of substrate removal on device performance, it is important to have a baseline for the properties of our material before any processing. Properties of interest for our wafers include structural confirmation, defect densities, crystalline quality, electron mobility, and electron sheet concentration. Scanning electron microscopy (SEM), atomic force microscopy (AFM), X-ray diffraction (XRD), and Hall measurements were employed to fully characterize the samples.

The desired device structure for our HEMT samples is shown below in Figure 3 [7]. It consists of an 8 inch Si (111) substrate followed by an AlN nucleation layer to prevent gallium melt-back etching of Si [28] and linearly step graded AlGa_N buffer layers. The buffer layers are used to control wafer bow and establish compressive strain to prevent cracking in the subsequently grown GaN layers. After the buffer stack, an initial GaN layer and AlN interlayer reduce dislocation density and control wafer curvature [29]. Carbon doping is employed as an auto-compensator to remove the effects of any unintentional doping caused by residual oxygen impurities during growth. Through compensation, we lower the GaN's conductivity and reduce leakage currents in the device, which help prevent premature buffer breakdown [30]. The top GaN/AlN/AlGa_N layers form the HEMT structure. The AlN layer is used to increase the conduction band offset and better contain the 2DEG, and the 14 nm Al_{0.25}Ga_{0.75}N layer forms the 2DEG. The final 2 nm GaN cap layer improves surface morphology and minimizes electrical contact resistance [31].

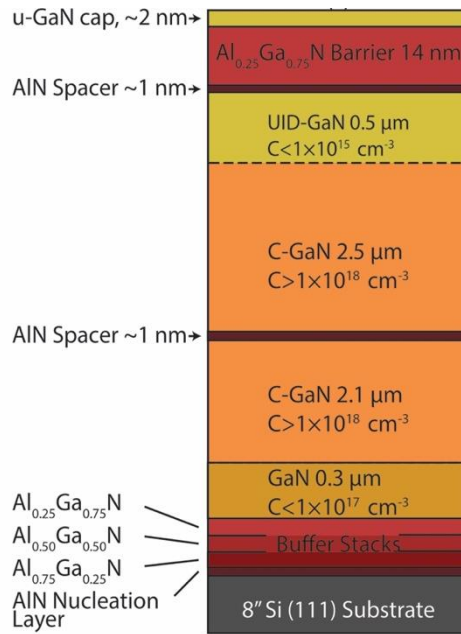


Figure 3. GaN on Si HEMT structure

3.1 SEM Structural Analysis

To confirm the structure, the wafer was cleaved and the cross-section was observed using SEM as shown in Figure 4. In this image, the layers are clearly defined with the desired thicknesses.

3.2 AFM Defect Density Calculations

An important metric that can affect HEMT performance is defect density. When viewed with AFM, threading dislocations can be seen as small, round, dark circles. Using software created with Python (see Appendix B), these defects can be accurately counted and defect densities can be calculated. For the wafer probed here, a defect density of $0.89 \times 10^9 \text{ cm}^{-2}$ was measured for the mid-radial portion of the wafer, which was determined to be the highest quality [7]. This value is comparable with other high quality GaN crystals grown on SiC and sapphire. An example of the AFM images with defects marked in blue on the right of the image is shown in Figure 5.

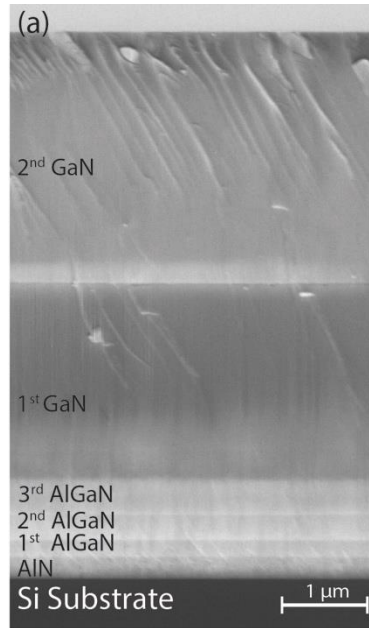


Figure 4. SEM of wafer cross-section

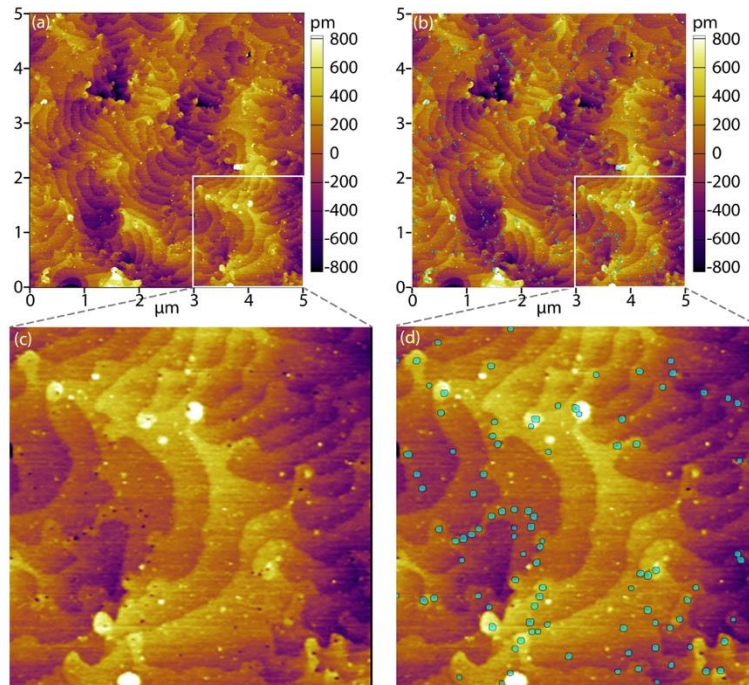


Figure 5. AFM defect determination

3.3 XRD Strain Determination

Using XRD, it is possible to measure the strain for each layer in our HEMT structure. Due to the high lattice mismatch between GaN and Si, when we release the GaN from the Si substrate, we expect to see a change in the measured strain.

To determine layer stress, XRD reciprocal space mappings of the (0002) and (1015) planes are required. From here, we can use the d-spacing (distance between adjacent planes) as determined by XRD to compute the a and c lattice of the crystal with [32]

$$\left(\frac{1}{d}\right)^2 = \frac{4}{3} \left(\frac{h^2 + hk + k^2}{a^2} \right) + \frac{l^2}{c^2} \quad (3.1)$$

where h, k, i , and l are the Miller indices of the scan planes ($h k i l$), and a and c are the measured lattice constants of the material.

By solving Poisson-Vegard's law [32] shown in Equation (3.2), we can compute the alloy composition and lattice constants of the strained lattices. In these equations, a bowing parameter has been added.

$$\frac{c_m(x) - c_0(x)}{c_0(x)} = -\frac{2\nu(x)}{1 - \nu(x)} \times \frac{a_m(x) - a_0(x)}{a_0(x)} \quad (3.2)$$

where

$$c_0(x) = xc_{AlN} + (1 - x)c_{GaN} - b_c x(1 - x) \quad (3.3)$$

$$a_0(x) = xa_{AlN} + (1 - x)a_{GaN} - b_a x(1 - x) \quad (3.4)$$

$$\nu(x) = x\nu_{AlN} + (1 - x)\nu_{GaN}. \quad (3.5)$$

In these equations, $c_m(x)$ and $a_m(x)$ are the measured c-axis and a-axis lattice parameters and $c_0(x)$ and $a_0(x)$ are the relaxed lattice parameters for the Al content percentage, x . We use the a and c-axis bowing parameters, b_a and b_c for the $Al_xGa_{1-x}N$ lattice constants where $b_a = 0.018$ and $b_c = -0.036$ along with Poisson ratios $\nu_{AlN} = 0.272$ and $\nu_{GaN} = 0.183$ [32], [33].

Using the calculated lattice constants, we can also determine the in-plane (ϵ_{xx}) and out-of-plane strain (ϵ_{yy}) using:

$$\epsilon_{xx} = \frac{a_m(x) - a_0(x)}{a_0(x)} \quad (3.6)$$

$$\epsilon_{yy} = \frac{c_m(x) - c_0(x)}{c_0(x)}. \quad (3.7)$$

After completing these measurements, the layer compositions of the buffer layers were determined to be $\text{Al}_{0.82}\text{Ga}_{0.18}\text{N}$, $\text{Al}_{0.59}\text{Ga}_{0.41}\text{N}$, and $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ for the first, second, and third AlGaN layers respectively. Additionally, the layer stress before substrate removal for each layer from the mid-radial wafer position is shown in Figure 6.

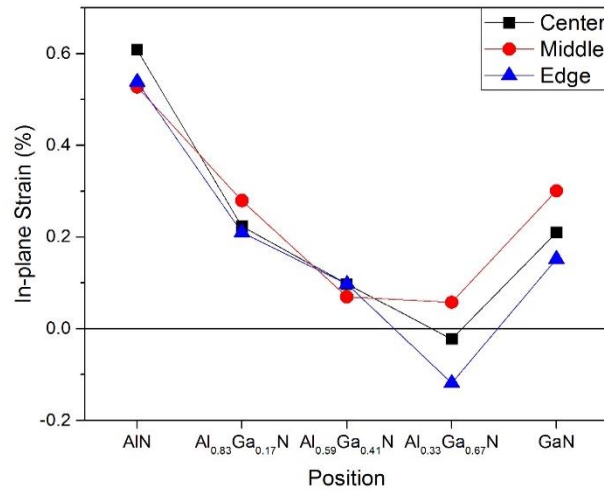


Figure 6. In-plane Strain for each layer

3.4 Hall Measurement Electrical Characterization

Because we expect the electrical characteristics to change as a function of layer strain, we also performed Hall measurements to determine the electron mobility and sheet concentration for the HEMT samples. The fabrication process for Hall measurement samples is described in Appendix B.

With Hall measurements, it is easier to determine whether a device is cracked or not. With a cracked device, we would see very poor mobility or (more likely) not even be able to make a complete measurement. Thus, with Hall samples that are working before substrate removal, we can confirm that the transferred GaN films are still crack free if they have comparable mobility. Any changes should be due to changes in strain after transfer as well as non-cracking defects.

For the sample before substrate removal, Table 2 summarizes the results of the Hall measurement at both room temperature (RT) and low temperature (LT) which was obtained by submerging the samples in liquid nitrogen (77 K) during measurements.

Table 2. Hall Effect Results

| POSITION | 2DEG CONC. [$10^{13}/\text{cm}^2$] | | MOBILITY [$\text{cm}^2/\text{V-s}$] | |
|----------|---|----------------|--|----------------|
| | RT | LT | RT | LT |
| MIDDLE | 1.20 ± 0.05 | 1.20 ± 0.1 | 1447 ± 54 | 5561 ± 820 |

4. Substrate Removal Process and Results

As discussed in Chapters 1 and 2, the most commonly used method for substrate removal of GaN on Si is to use mechanical lapping followed by reactive ion etching (RIE). However, due to the complexity of the equipment and chemicals used, this process is somewhat expensive and difficult. An alternative approach used in this project is a wet etching process. The most common silicon etchant is KOH, but this chemical shows strong anisotropy in its etching with a very slow etch rate on the (111) plane (the surface plane of the Si substrate). Thus, we instead use an etchant made from hydrofluoric, nitric, and acetic acids, commonly referred to as HNA etchant. Another benefit of using this solution is that it will not etch AlN or GaN, so in theory, there is no danger of over-etching. The etch rates of this solution are shown in Figure 7 [34]. The ratio of HNO_3 :HF: $\text{HC}_2\text{H}_3\text{O}_2$ used here is 5:3:3, which has an etch rate of ~3 mils/minutes (75 $\mu\text{m}/\text{min}$). This was chosen for its moderate etch rate and because it was readily available from our supplier.

Since the goal of this project is to test the quality of the material before and after substrate removal as well at various bending conditions, it made sense to use the same Hall measurement samples that had already been measured. These samples already had ohmic contacts deposited in the corners, were conveniently sized to not waste material, and provided direct sample-to-sample comparison. Figure 8 shows the Hall sample before etching. The ohmic contacts made of titanium and nickel are visible in the corners.

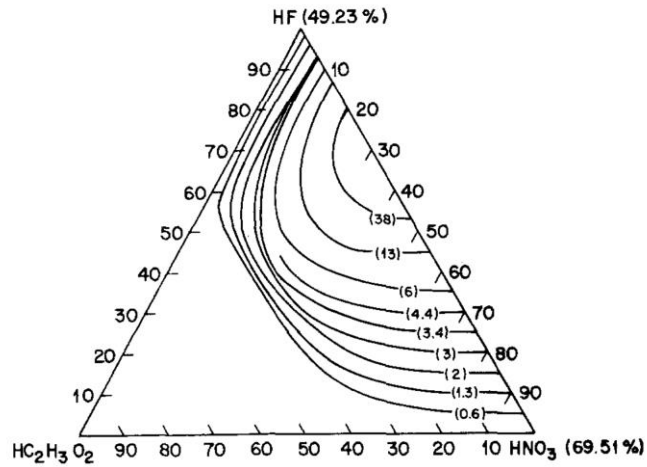


Figure 7. Etch rates of Si in mils/min for solution of 48% HF, 70% HNO₃, 100% HC₂H₃O₂

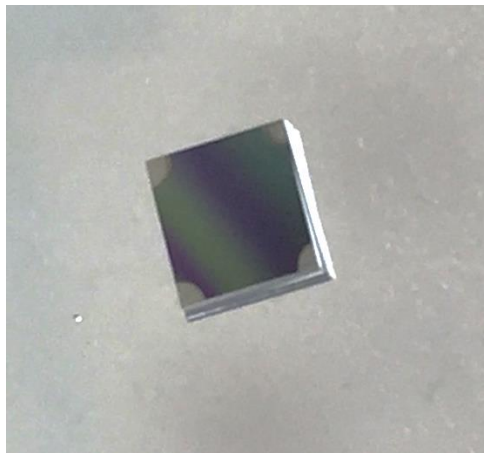


Figure 8. A 4 × 4 mm Hall sample

After the silicon is completely etched away, we are left with a several micron thick piece of GaN that is extremely fragile. Thus, the first issue to resolve was that of sample handling. To allow easier handling, 2 inch sapphire wafers were cleaved into quarters and the samples were bonded to the surface GaN-side down. Sapphire was used due to its complete resistance to the etchants used. The next hurdle was determining the proper adhesive to use for bonding the GaN sample to the sapphire. We

needed a material that could provide a strong hold, was completely acid resistant, and could be easily removed. Typically, for bonding processes such as this, crystalbond, double-sided tape, or thermal release tape is used. However, after testing these materials, none of them could withstand the acid solution. To ensure we used a strong enough adhesive, we then turned to black wax, which is completely chemically inert and can be melted at temperatures greater than 110 °C to mount and remove the sample. This wax holds up very well in the solution, but tends to be too sticky to easily remove the sample after etching. As an attempt to simplify the release, many different mounting techniques were developed and tested including using thermal release tape, double-sided tape, photoresist and combinations of all the materials listed. Appendix A outlines all the various methods tried with illustrations and results when available.

While sample mounting proved to be the most difficult portion of this project, another major concern was sample cracking. Figure 9 shows a successfully transferred GaN layer, but it is apparent that the sample is clearly cracked along the typical 60° cleave planes we see in GaN. In the image, we can also see some un-etched Si as the black dot in the center and some remaining wax on the back side of the GaN. Unfortunately, results like this were very common and nearly every transferred GaN sample was cracked and most were missing pieces. Figure 10 shows a microscope image of another cracked sample with complete silicon removal and visible contacts.

For several samples, it was possible to achieve crack-free etching as shown in Figure 11. However, to transfer the samples properly requires a rinse in a chlorinated solvent; here, trichloroethylene (TCE) and 1,1,1-trichloroethane (TCA) were used. During the rinsing process, any sample that was un-cracked would be washed away and be lost in the solution, so we could not retrieve it. While not cracked, a closer inspection of the sample also shows some stress lines along the edges of the sample. We are currently unsure of what is causing these and how they affect performance, but

their existence should be noted. A positive takeaway from this image is that the metal contacts can still be seen in the corners of the sample, which indicates the wax is fully protecting the surface and if complete transfer is achieved, Hall measurements will be possible without reapplying contacts.

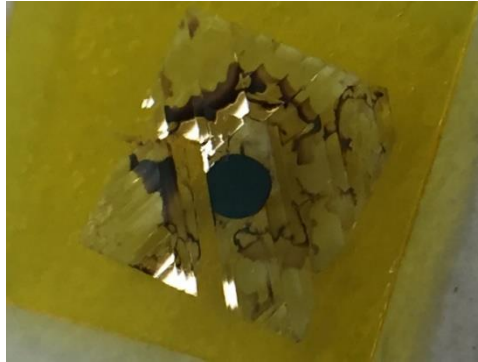


Figure 9. Fully transferred, cracked GaN sample

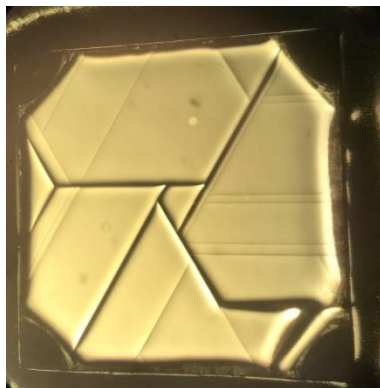


Figure 10. Cracked GaN before transfer

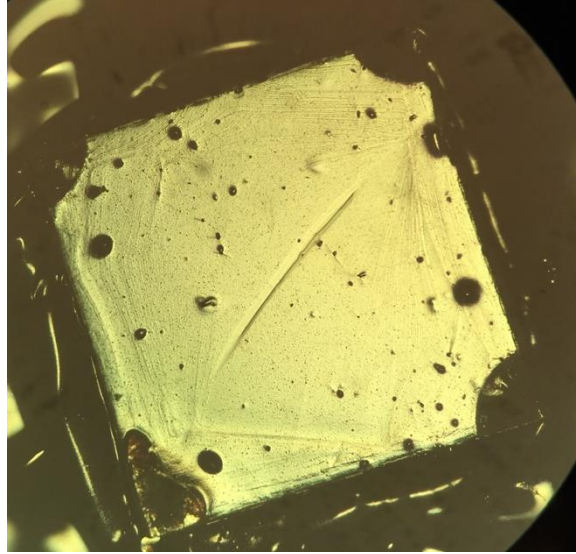


Figure 11. Un-cracked with complete Si removal before transfer

Although many more complex procedures have been attempted in this project, the most recent and most promising technique starts with mechanical lapping. To begin the process, samples are mounted on the unpolished side of the sapphire wafer using the black wax at 200 °C. The unpolished side is used with the hope that the slightly increased surface area will improve adhesion. Then, all excess wax is removed with TCA, which differs from initial processes where this was done after etching. We do this to avoid losing the sample in the rinsing step after etching since it is no longer necessary. Etching was attempted at this point, but the samples were continually cracked. According to Mhedhbi et al., a major cause of the cracking is prolonged exposure of the GaN layers to the acid solution [2]. As can be seen in Figure 12, the etchant removes the silicon from the edges faster than the center, which we would expect because the corners and edges have more exposed surface area than the middle. This means that while the center of the silicon is still etching, the edges are over exposed and will tend to crack. In an attempt to combat this, mechanical lapping was employed to thin the silicon and therefore reduce the etch times. The sapphire wafers with mounted GaN samples were attached to the lapping chuck using crystalbond and then, using 15 μm diameter Al_2O_3 powder, the samples are thinned down

from 750 μm to approximately 200 μm at a rate of about 150 $\mu\text{m}/\text{hour}$. As the samples approached their final thickness, care had to be taken to reduce the grinding rate so that the samples would not crack as seen in Figure 13. Because lapping can ruin the adhesion of the wax around the edges of the sample, an additional step is added where more wax is heated next to the sample and we slide the sample onto the new wax. Once again, we remove the excess wax with TCA and then etch the sample. To remove the sample, a glass slide with double-sided tape is pressed on the sample and then heated to 200 $^{\circ}\text{C}$ to melt the wax. Then, we lift the slide with the sample attached to the tape. Finally, residual wax is gently removed in a TCA rinse and the transfer is complete. Images summarizing the process and the final result are shown in Figure 14-Figure 17. While nearly complete sample transfer was achieved, the sample was badly cracked with the contacts etched away. Further refinement in the process is needed to prevent cracking.

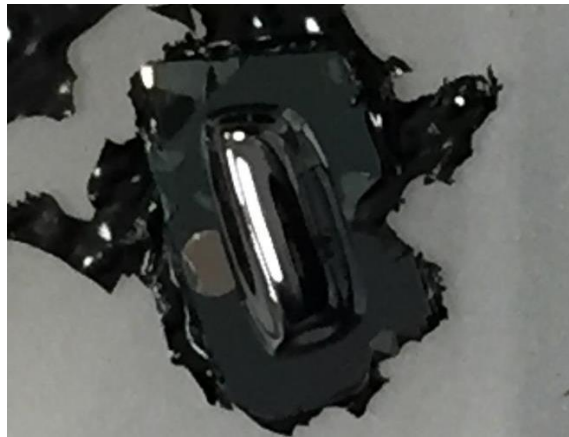


Figure 12. Example of uneven Si removal; the shiny portion in the middle is remaining Si



Figure 13. Cracked sample after aggressive lapping

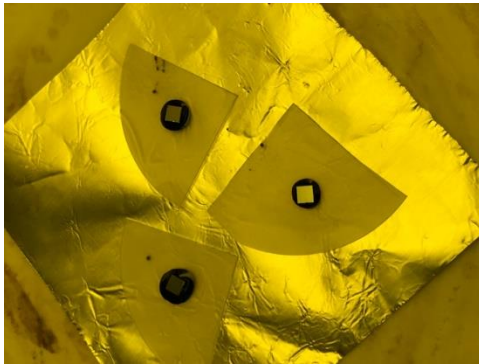


Figure 14. Samples mounted on sapphire with black wax on hotplate

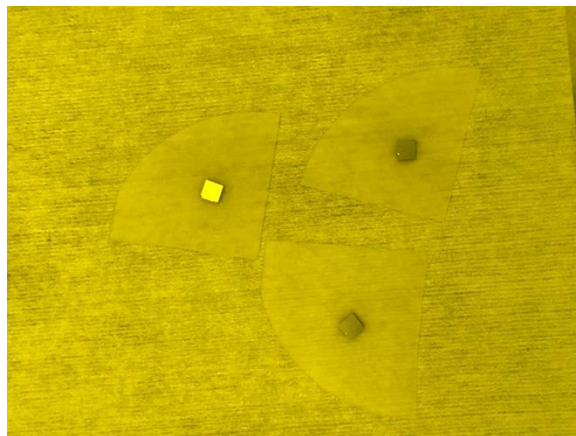


Figure 15. Samples after lapping with excess wax removed with TCA

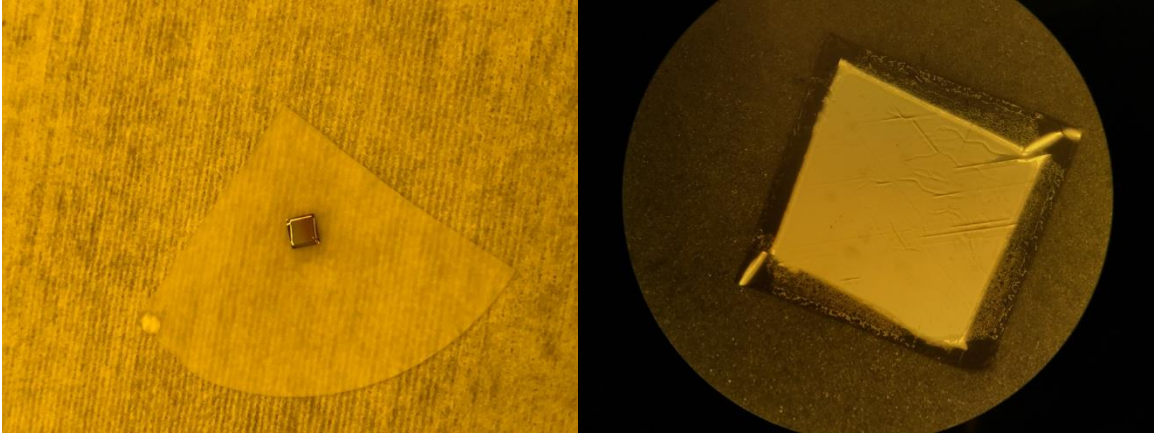


Figure 16. Sample after etching all Si with image through (left) camera and (right) microscope. Cracks are visible at this stage though faint

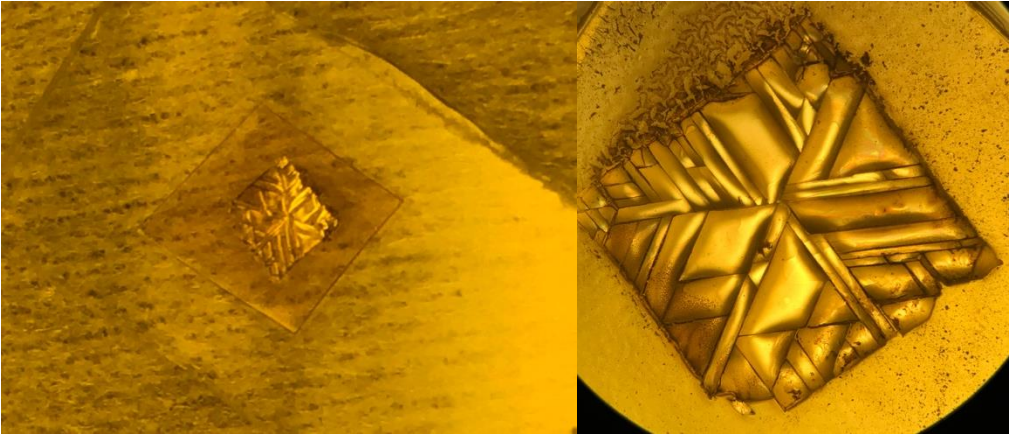


Figure 17. GaN transferred to tape on glass slide. Cracks are more apparent

5. Conclusion

Gallium nitride has many properties that make it ideal for transistors used in high power and high frequency applications. When grown on Si (111), it is possible to grow high quality GaN epitaxial layers. Through substrate removal processes, we can obtain GaN thin-film devices that are suitable for flexible electronics. The properties of these GaN layers were explored in-depth before the substrate removal process with the goal of comparing the properties before and after removal. Using a mechanical lapping and wet-etching based approach as a cheaper alternative to reactive ion etching, we are able to create flexible GaN thin-films. However, in many cases, possibly due to over-etching or uneven strain from anisotropic etching of Si, these films are often cracked. Moreover, when the samples do not crack, the removal process is often difficult and results in lost samples. Further investigation is needed to prevent these cracks and a more reliable process for un-mounting the samples after etching needs to be developed.

Appendix A: Processes and Results

This appendix compiles the various processes attempted and their results during this senior thesis project. Each method is listed with a step-by-step process, illustration, and discussion of results. When images of the actual process are available, they are shown as well as discussed further.

Method 1: Black wax only with HNA etch

Process: Shown in Figure 18

1. Heat up black wax on sapphire wafer at 120° C until liquid.
2. Place the GaN side of a GaN on Si sample into the wax.
3. Etch in HF/Nitric/Acetic (HNA) acid to remove all Si.
4. Permanently attach the back of the GaN to a new substrate.
5. Heat at 120 °C to release the wax.

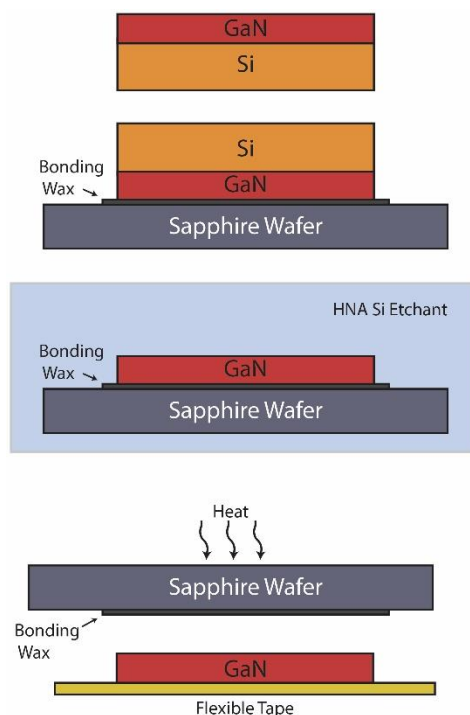


Figure 18. Black wax only process

Results:

Using this method, the Si could be successfully removed and the contacts remained intact as shown in Figure 19. However, it was very difficult to remove the sample from the sapphire after the etching was done. Every time, it was necessary to slide the fragile GaN layers off the edge (slip release technique), which tended to crack the GaN. Since the silicon removal worked but the release kept breaking the samples, a new method for mounting the GaN was needed.



Figure 19. Initial results for only black wax

Method 2: *Sample holder with no mounting*

Process:

1. Use a sample holder made of Teflon; place the sample in the HNA acid etchant.
2. After etching, remove the sample.

Results:

Using this method was nearly impossible without a more professionally made sample holder. The sample holder made here was essentially a Teflon basket with a handle. When it was made as a shallow basket (small walls), the sample would get lost and float away during the etching. Since the extremely delicate sample was floating somewhere in a dangerous acid mixture, it was impossible to find and retrieve it, so it was considered lost. A second attempt with deeper walls in the sample holder could

keep the GaN in place, but due to the delicacy of the thin film, the sample cracked immediately upon the attempted retrieval. This method proved too uncontrollable and was set aside in favor of other processes.

Method 3: *Black wax with double-sided tape*

Process: Shown in Figure 20

1. Place double-sided tape on sapphire wafer *without* removing the plastic film from one side.
2. Cover the tape (and the protective plastic film) with black wax by heating, and make sure all parts of the tape are covered.
3. Place the GaN side of the sample into the hot wax and allow it to cool.
4. Etch silicon in HNA etchant.
5. Using TCE, remove the excess wax. Wax will remain between the sample and tape where the TCE cannot reach.
6. Lift off the protective plastic film with the GaN and permanently mount the GaN side to a new substrate.
7. Using heat, melt the wax and remove the plastic (which should stick less to the wax than the sapphire wafer).
8. Clean off any residual wax with TCE.

Results:

Slight variations on this method (Figure 20) were tested many times with various levels of success.

Initially, wax was melted at only 120 °C, which left it fairly thick. When done this way, the samples tended to crack (it is possible there were cracks already existing in the sample). Mechanical lapping was also used to remove about half the silicon prior to etching to reduce etch times and hopefully make less stress on the sample and the silicon varies in thickness. Unfortunately, the samples were again cracked before etching. While initial tests were performed with sample 1205 (thick silicon and GaN layers), we later used 1614 (thinner silicon and GaN layers) which tended to be more crack-free. Using these samples and the wax and double-stick tape process the substrate could be completely removed without cracking as shown in Figure 21. Unfortunately, whenever the GaN was un-cracked, during the TCE wash,

the samples would fall off the sapphire carrier wafer. Looking at Figure 21, it appears that there is no wax between the sample and tape, which is likely why it falls off during washing.

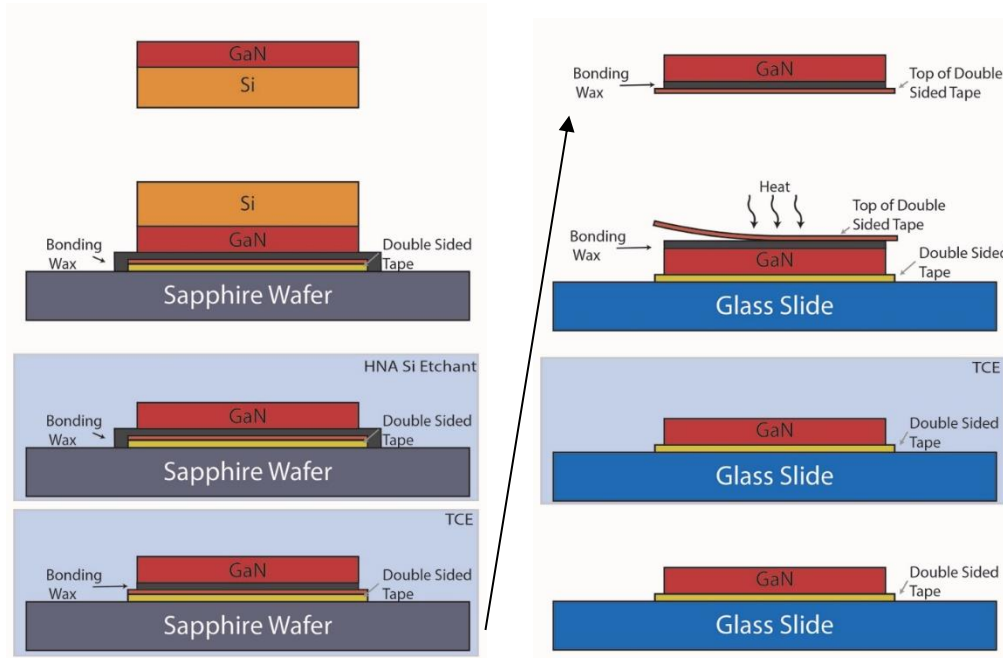


Figure 20. Black wax with double-sided tape process

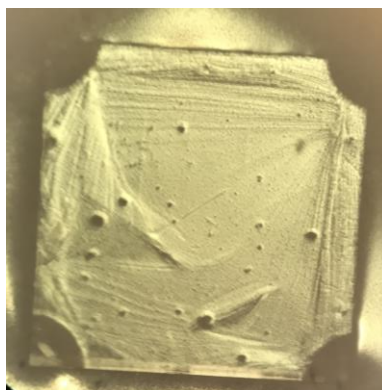


Figure 21. Un-cracked GaN after etching

Alternatively, the samples would occasionally crack as shown in Figure 22. When this happened, the samples did not fall off and nearly complete transfer of the thin film was possible. As can be seen in both images, there is some residual wax (black/brown portions) remaining on the top of the samples. Unlike in the un-cracked samples where no wax is visible, this is likely why the cracked samples did not fall off. While it seems possible that the wax beneath the samples is causing them to crack, it is still currently unknown whether this is the case.

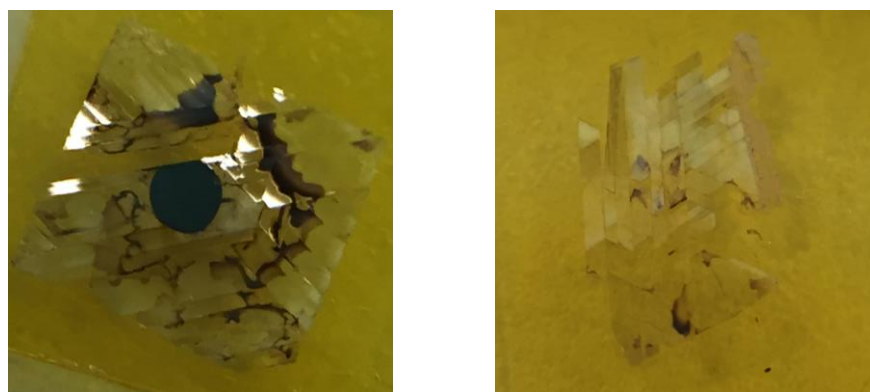


Figure 22. Cracked GaN samples after transfer (black dot in the center of the left image is remaining silicon)

Further variations of this technique had to do with wax application. In some cases, a thin layer of wax was rubbed on at a low temperature to get a more uniform layer, in others wax was heated to 160°C to give it a very low viscosity. In all attempts, either the sample was cracked or if it remained intact, it fell off and was lost during the TCE rinse.

Method 4: *Thermal release tape*

Process: Shown in Figure 23

1. Using double-sided thermal release tape, mount the sample on a sapphire wafer.
2. Remove the silicon with HNA etchant.
3. Permanently mount the back of the GaN film on a new substrate.

4. Release the tape with heat to un-mount the sample from the sapphire.

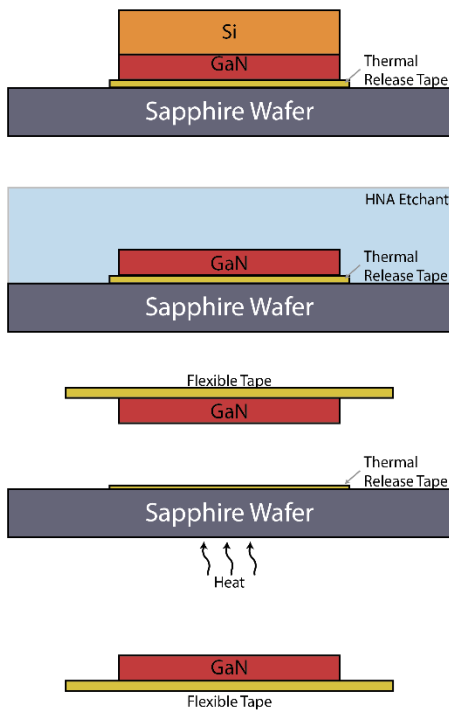


Figure 23. Thermal release tape process

Results:

Revalpha double-sided thermal release tape was used for this (Figure 23) and subsequent processes. It has an adhesion of 3.7 N/20 mm and a release temperature of 150 °C. Using this process, the sample always fell off during the etching process and was never found. The acid seemed to react with the thermal release adhesive and release the sample. A new process was needed to protect the surface of the tape during etching

Method 5: *Thermal release tape with black wax*

Process: Shown in Figure 24

1. Place the regular adhesive side of thermal release tape on a sapphire wafer.

2. Melt the wax at the lowest possible temperature (~115 °C) to not cause the tape to release.
3. Press the sample into the wax.
4. Remove the silicon with HNA etchant.
5. Use TCE to remove the excess wax.
6. Permanently mount the back of the GaN film on a new substrate.
7. Thermally release tape to unmount the sample from the sapphire.

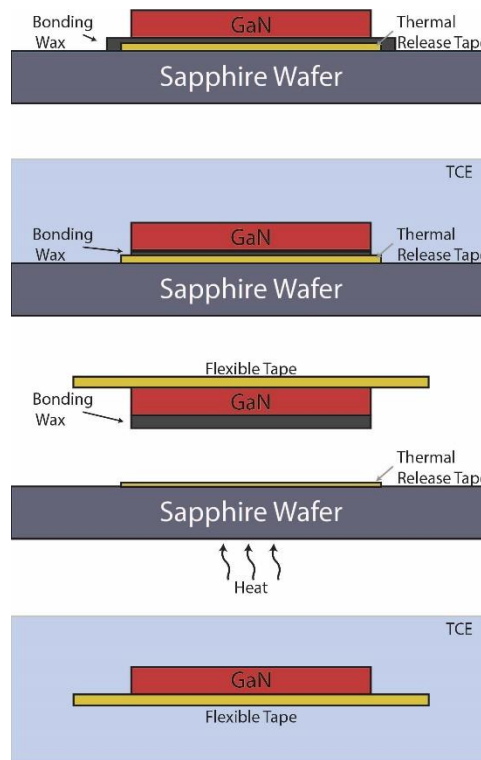


Figure 24. Thermal release tape with black wax process

Results:

Using this process (Figure 24) was tricky due to the mismatch between the melting temperature of the wax and the release temperature of the tape. Various amounts of wax was tried. Initially, a small amount of wax just beneath the sample was used to hopefully protect the adhesive that was immediately below the sample. This unfortunately fell off during etching. Next, more wax covering all

the tape was tried, but once again the sample fell off from the wax during etching (likely because the wax was never hot enough to adhere to the sample).

Method 6: *Crystalbond*

Process:

This process is very similar to Method 1 where Cystalbond is used instead of black wax in the hope that the release will be easier

1. Heat the sapphire wafer and apply a small amount of Crystalbond to the polished surface.
2. Mount the GaN side of the sample in the Crystalbond.
3. Remove the silicon with HNA etchant.
4. Use acetone to remove the excess Crystalbond.
5. Permanently mount the sample to a new substrate.
6. Use heat to release the remaining Crystalbond.

Results:

With this method, we hoped that the Crystalbond could hold up to the acid and then provide an easier release afterwards. Unfortunately, during the etching, all the Crystalbond dissolved and the sample was lost.

Method 7: *Thermal release tape with photoresist*

Process:

1. Place the regular adhesive side of the thermal release tape on a sapphire wafer.
2. Place several drops of photoresist on the thermal release tape.
3. Tilt and rotate the sapphire wafer to allow the photoresist to cover all parts of the tape and let excess photoresist drip off the side.
4. Place sample GaN-side-down into the photoresist and bake at 100 °C to solidify.
5. Remove the silicon with HNA etchant.
6. Use acetone to remove excess photoresist.
7. Permanently mount the GaN to a new substrate.
8. Heat the tape to release the adhesive from the photoresist and GaN.
9. Use more acetone to remove the remaining photoresist from the sample.

Results:

This process was used because we thought the lower baking temperature and more liquid application of the photoresist would allow better adhesion of the sample. However, during the etching process, the sample fell off the photoresist. Upon inspection, no photoresist remained where the sample used to be on the tape, so either there was none between the sample and tape, or it was etched away.

Method 8: *Thermal release tape with photoresist and heat treatment*

Process:

1. Place the regular adhesive side of thermal release tape on a sapphire wafer.
2. Place several drops of photoresist on the thermal release tape.
3. Tilt and rotate the sapphire wafer to allow the photoresist to cover all parts of the tape and let excess photoresist drip off the side.
4. Place the sample GaN-side-down into the photoresist and bake at 60 °C until solid.
5. Remove the silicon with HNA etchant.
6. Use acetone to remove excess photoresist.
7. Permanently mount the GaN to a new substrate.
8. Heat the tape to release the adhesive from the photoresist and GaN.
9. Use more acetone to remove the remaining photoresist from the sample.

Results:

After consulting the producers of the thermal release tape, we learned that it is possible to increase the adhesion of the tape through a low temperature heat treatment as shown in Figure 25. With this method, the adhesion for the tape used in the plot increases from 7 N/20 mm to 20 N/20 mm. We hoped that through heat treatment, we could make the sample not fall off, but this was not the case and it was once again lost. However, while writing this report, it was discovered that there are notes added to the pdf that are only viewable with the adobe pdf viewer which properly describes the heat

treatment process. When we performed the heat treatment, it was only heated to 60 °C for about 5 minutes until the PR was mostly solid. It was then immediately transferred to the acid solution. Reading the notes, however, it is necessary to heat the tape for at least 10 minutes (which would have the added benefit of further solidifying the photoresists, and then it needs to rest at room temperature for at least 30 minutes before continuing. This process will be attempted within the next week.

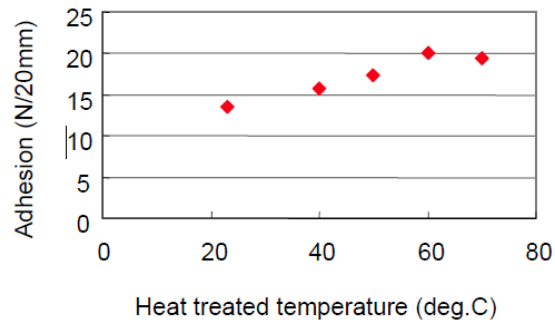


Figure 25. Thermal release tape heat treatment for improved adhesion (obtained through private correspondence with NittoDenka Corporation)

Method 9: *Thermal release tape with photoresist, HMDS, and heat treatment 1*

Process:

1. Place the regular adhesive side of the thermal release tape on a sapphire wafer.
2. Place several drops of photoresist on the thermal release tape.
3. Tilt and rotate the sapphire wafer to allow the photoresist to cover all parts of the tape and let excess photoresist drip off the side.
4. Spin HMDS adhesion promoter and photoresist onto the GaN sample and bake at 100 °C until solid.
5. Place the sample GaN-side-down into the photoresist on the thermal release tape and bake at 60 °C until solid.
6. Remove the silicon with HNA etchant.
7. Use acetone to remove excess photoresist.
8. Permanently mount the GaN to a new substrate.
9. Heat the tape to release the adhesive from the photoresist and GaN.
10. Use more acetone to remove the remaining photoresist from the sample.

Results:

Since the photoresist on the edges of the tape seemed to be sticking during the etching process, we thought the GaN may be falling off the photoresist and not the tape. Thus, we used HMDS to improve the adhesion of the PR to the GaN. Once again, the sample fell off the tape during etching and was lost.

Method 10: *Thermal release tape with photoresist, HMDS, and heat treatment #2*

Process:

1. Clean the sample in an ultrasonic cleaner with acetone for 5 minutes followed by an IPA and DI water rinse.
2. Spin HMDS and PR onto the GaN side of the sample. Bake at 60 seconds at 100 °C.
3. Put the thermal release tape on a sapphire wafer and coat the tape with PR. Spin the wafer briefly to evenly distribute the PR.
4. Place the GaN sample on the sapphire wafer and bake at 60 °C for 10 minutes until solid.
5. Let the sample rest and cool at room temperature for 1 hour.
6. Place the sample in acid and remove the silicon with HNA etchant.
7. Use acetone to remove the excess PR.
8. Permanently mount the GaN sample to a new substrate.
9. Heat the tape to release the adhesive from the photoresist and GaN.
10. Use more acetone to remove the remaining photoresist from the sample.

Results:

This process differs from Method 10 in that the PR layer on the sapphire/tape is briefly spun to evenly distribute it and create a thinner layer. The hope was that the thinner layer would allow it to better solidify at a low temperature to make it more resistant to acid. However, during the etching process, the photoresist was unable to protect the tape from the acid. The acid then ruined the tape's adhesion and the sample fell off the tape.

Method 11: *Thermal release tape with photoresist, HMDS, and heat treatment #3*

Process:

1. Clean the sample with an ultrasonic cleaner and acetone.
2. Spin HMDS and PR onto the GaN sample, but do not bake it.
3. Place the thermal release tape on a sapphire wafer and coat the tape with PR. Spin the wafer briefly to distribute.
4. Place the sample on the tape GaN-side-down and bake at 60 °C for 45 minutes.
5. Let the sample rest and cool at room temperature 4 days.
6. Place the sample in acid and remove the silicon with HNA etchant.
7. Use acetone to remove the excess PR.
8. Permanently mount the GaN sample to a new substrate.
9. Heat the tape to release the adhesive from the photoresist and GaN.
10. Use more acetone to remove the remaining photoresist from the sample.

Results:

This process adjusts the baking/rest times used in Method 11 and does not bake the HMDS/PR on the GaN sample before mounting on the tape. By not baking the GaN, we were hoping to form a more cohesive bond between the GaN and protective photoresist. The PR was also baked significantly longer so that it was guaranteed to solidify, which should strengthen its acid resistance. To make sure the tape reaches maximum adhesion, it was left for a weekend to cool and rest for four days. Once again, the sample fell off during etching and was not received.

Method 12: *High temperature wax mounting*

Process:

1. Heat wax on the UNPOLISHED side of a sapphire wafer at 190 °C until the wax runs freely.
2. Place the GaN sample in the wax and gently push down.
3. Use TCA to remove the excess wax from edges.
4. Place the sample in acid to etch the silicon.
5. Remove the sample from the acid and rinse thoroughly.
6. Prepare glass slide with a small piece of double-stick tape.
7. Press the tape onto the sample.

8. Heat the sample on a hot plate to 190 °C.
9. Lift off the glass slide to release the sample.
10. Use TCA to clean off the remaining wax.

Results:

In this process, the unpolished side of the sapphire was used to hopefully increase adhesion with the increased surface area. The wax was also heated to 190 °C to make it run easily and completely coat the area between the GaN and sapphire. Since in previous methods, the sample would fall off during the after-etching TCA rinse, the wax was this time removed prior to etching, thus eliminating that step. After etching, the sample was cracked, but much of it was still there. By heating to 190 °C, the sample was easily removed. However, during the double-sided tape portion, there was incomplete adhesion (more pressure was needed) and only part of the sample transferred. The rest of the sample fell off during the final TCA rinse to remove residual wax.

Method 13: *Mechanical lapping and high temperature wax*

Process: Shown in Figure 26

1. Check that sample is uncracked and perform an ultrasonic clean with acetone.
2. Heat wax on the UNPOLISHED side of a sapphire wafer at 200 °C until very liquid.
3. Place the GaN sample in the wax and gently push down.
4. Use TCA to remove excess wax from the edges.
5. Place the sample in acid to etch the silicon.
6. Remove the sample from the acid and rinse thoroughly.
7. Prepare a glass slide with a small piece of double-stick tape.
8. Press the tape and glass slide onto the sample.
9. Heat the sample on a hot plate to 200 °C.
10. Lift off the glass slide to release the sample.
11. Use TCA to clean the remaining wax off.

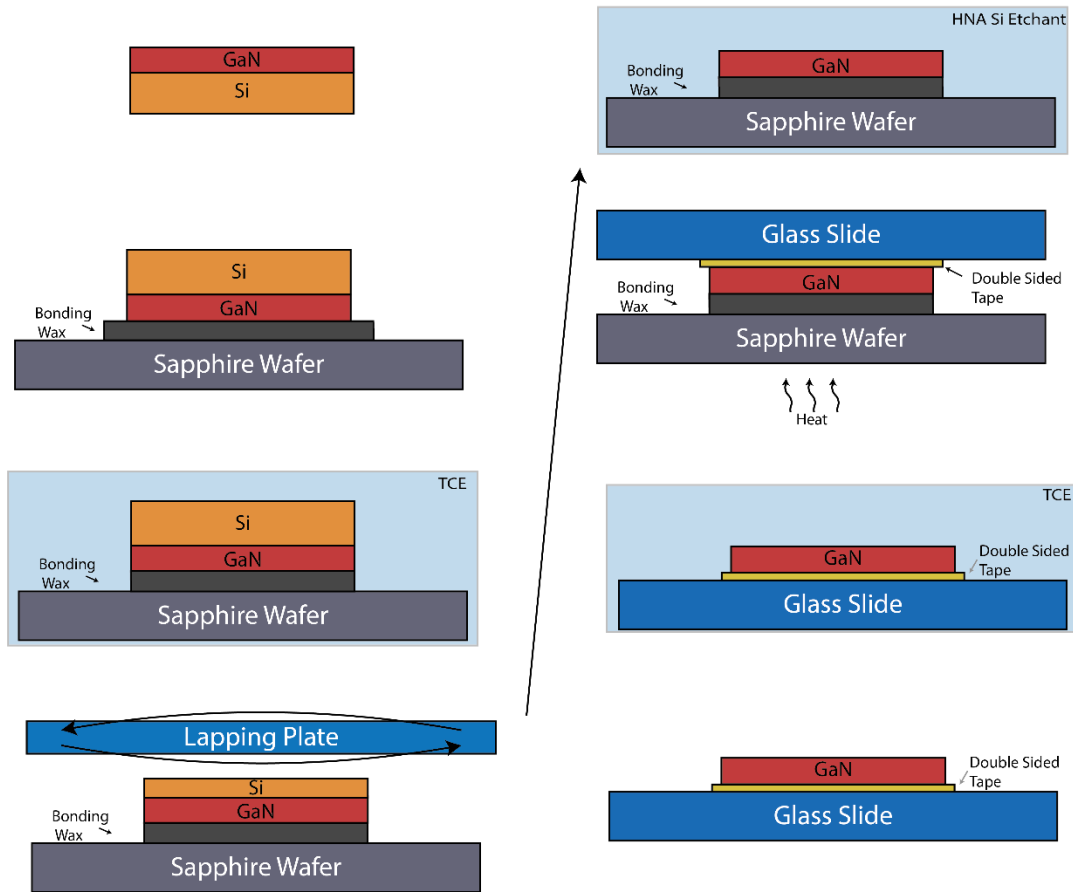


Figure 26. Mechanical lapping and high temperature wax process

Results:

For this process, the temperature was increased to 200 °C (arbitrarily for a round number). During normal processes, the Si etches faster from the sides exposing the GaN on the edges faster than the center. This may cause over-etching that could be a cause of cracking. To stop this, mechanical lapping was used to thin the Silicon and reduce the time it takes to completely remove the substrate and minimize over-etching. This process has provided the best results today because nearly complete transfer was achieved, but as can be seen in Figure 17, the sample is still severely cracked.

Appendix B: Characterization and Methods

B.1 Hall Measurements

To perform Hall measurements on the GaN samples, it is necessary to have square samples with small ohmic contacts in each corner as shown in Figure 27. Because the Si (111) substrate does not have 90° cleave planes (like Si (100)), it is extremely difficult to create Hall samples with a diamond scribe and cleaving. Instead, we have developed a method for Hall sample preparation using a dicing saw for device isolation.

To begin the process, a metal contact mask with a grid of 1 mm diameter holes spaced 4 mm apart is taped to the sample. Using an electron beam evaporator, 200 nm of Ti followed by 200 nm Ni is deposited on the samples through the openings of the mask. Titanium is used as an adhesion layer and nickel is used to make ohmic contacts with GaN due to its work function. For devices requiring longer lifetimes, a gold layer would have been used at the end to prevent oxidation. Figure 28 shows the mask and completed contact deposition. Following metallization, the contacts show a strong rectifying behavior. To make them ohmic contacts, we anneal them at 750 °C for 45 seconds in a nitrogen atmosphere. Contact improvement can be seen from the I-V curves in Figure 29 where the an N₂ atmosphere significantly reduces resistance and improves contact linearity.

After contact deposition, it is necessary to isolate the samples. To achieve this, a thick photoresist layer is coated over the entire sample and soft-baked to protect the surface during dicing. A dicing saw is then used to cut each circular contact in half. To keep the samples together during dicing and cleaning, only about 75% of the material is cut through. After complete dicing, the pieces are cleaned to remove the photoresist and then they are separated by gently breaking the remaining silicon. Figure 30 shows the resulting samples used to measure mobility and electron concentration with the MNTL Hall measurement system.

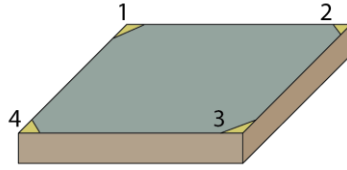


Figure 27. Square Hall sample example; gold triangles in the corners represent ohmic contacts

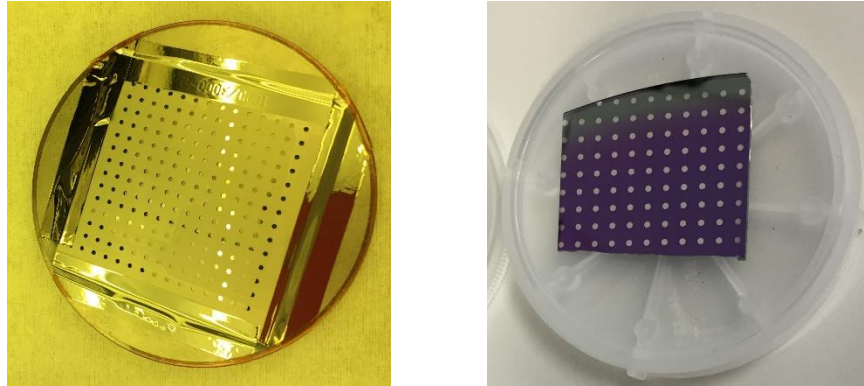


Figure 28. (left) Contact mask after metallization and (right) GaN with deposited contacts

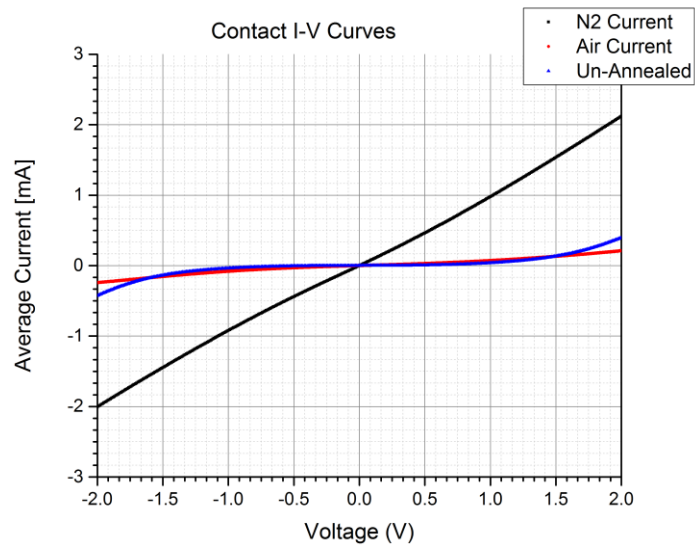


Figure 29. Contact comparison under various annealing conditions

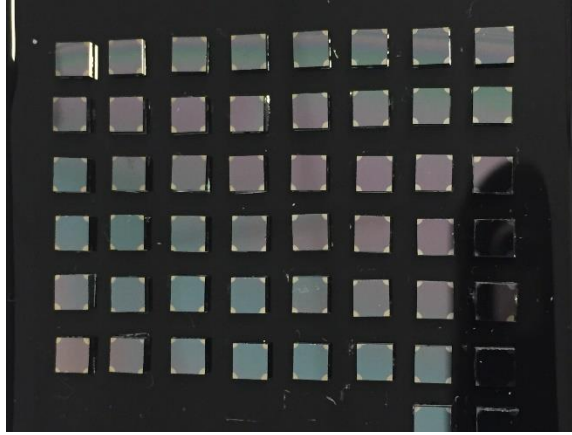


Figure 30. Hall effect samples after dicing

B.2 AFM Defect Counting

While processes like XRD can provide reasonable estimates to defect densities, to accurately measure defectivity of GaN samples requires physically counting the defects over large area scans. To achieve this, we used an atomic force microscope (AFM) to map the surface of the wafer. With a sharp probe tip, the threading dislocations appear as small pits in the sample surface as seen by the black dots in the left image of Figure 31 (may need to be viewed online to see). Since each $5 \times 5 \mu\text{m}$ scan can contain over 500 defects, counting by hand quickly becomes very tedious. To automate the process, we created a program using Python that will detect and count all defects in the image.

To implement the defect detection, each image is converted to greyscale and a light Gaussian filter is applied to remove some image noise. Each pixel is then scanned and the surrounding pixels are examined; if the current pixel is darker (meaning it represents a pit on the wafer) than a pre-determined threshold (found by taking a regional average of the pixel values), its location is marked in a separate image file by placing a blue dot so that it can be overlaid and accuracy can be measured. Using the Python library Mahotas and Scipy, the number of dots on the newly created image are counted and exported into an excel file. With this program, many images can quickly and accurately be analyzed.

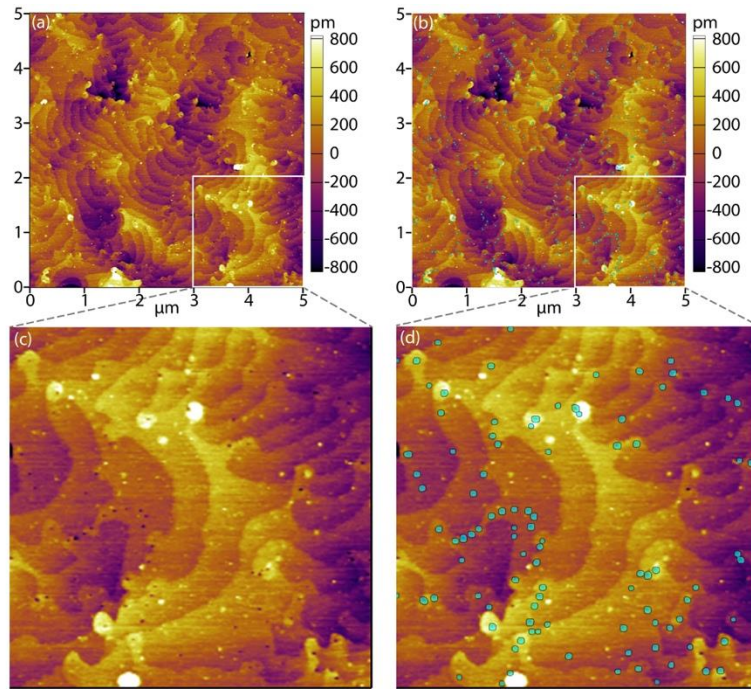


Figure 31. (left) AFM scan of surface with (right) defects marked in software

References

- [1] M. Riordan, L. Hoddeson, and H. Conyers, "The Invention of the Transistor," *Rev. Mod. Phys.*, vol. 71, no. 2, 1999.
- [2] S. Mhedhbi *et al.*, "Recent improvements of flexible GaN-based HEMT technology," *Phys. Status Solidi Appl. Mater. Sci.*, no. 1600484, 2017.
- [3] B. Ozpineci and L. M. Tolbert, *Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications*. 2003.
- [4] H. Morkoc, *Handbook of Nitride Semiconductors and Devices*. Weinheim: WILEY-VCH, 2008.
- [5] K. Y. Chent, *Compound Semiconductors and Devices - An Introduction*. ECE 488 Textbook, University of Illinois at Urbana-Champaign, 2010.
- [6] H.-P. Lee, J. Perozek, L. D. Rosario, and C. Bayram, "Investigation of AlGa_N/Ga_N high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations," *Sci. Rep.*, vol. 6, no. August, p. 37588, 2016.
- [7] J. Perozek *et al.*, "Investigation of structural , optical , and electrical characteristics of an AlGa_N / Ga_N high electron mobility transistor structure across a 200 mm Si (1 1 1) substrate," *J. Phys. D. Appl. Phys.*, vol. 50, p. 55103, 2017.
- [8] S. Mohammad Alavi and E. Bagani, "Electron mobility limited by scattering from threading dislocation lines within gallium nitride," *Int. J. Mod. Phys. B*, vol. 30, no. 9, p. 1650050, 2016.
- [9] F. A. Marino, N. Faralli, T. Palacios, D. K. Ferry, S. M. Goodnick, and M. Saraniti, "Effects of threading dislocations on AlGa_N/Ga_N high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 353–360, 2010.
- [10] a. P. Zhang *et al.*, "Correlation of device performance and defects in AlGa_N/Ga_N high-electron mobility transistors," *J. Electron. Mater.*, vol. 32, no. 5, pp. 388–394, 2003.
- [11] M. Leszczynski *et al.*, "Comparison of Si, Sapphire, SiC, and GaN Substrates for HEMT Epitaxy," *ECS Trans.*, vol. 50, no. 3, pp. 163–171, 2013.
- [12] A. R. Boyd *et al.*, "Growth of Ga_N/AlGa_N on 200 mm diameter silicon (111) wafers by MOCVD," *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 6, no. SUPPL. 2, pp. 1045–1048, 2009.
- [13] J. Cheng *et al.*, "Growth of high quality and uniformity AlGa_N/Ga_N heterostructures on Si substrates using a single AlGa_N layer with low Al composition.," *Sci. Rep.*, vol. 6, no. February, p. 23020, 2016.
- [14] S. L. Selvaraj *et al.*, "Process Uniformity and Challenges of AlGa_N/Ga_N MIS-HEMTs on 200-mm Si (111) Substrates Fabricated with CMOS-Compatible Process and Integration," *J. Electron. Mater.*, vol. 44, no. 8, pp. 2679–2685, 2015.
- [15] K. Cheng *et al.*, "AlGa_N/Ga_N/AlGa_N double heterostructures grown on 200mm silicon (111) substrates with high electron mobility," *Appl. Phys. Express*, vol. 5, no. 1, pp. 128–131, 2012.

- [16] T. N. Bhat, S. B. Dolmanan, Y. Dikme, H. R. Tan, L. K. Bera, and S. Tripathy, "Structural and optical properties of Al_xGa_{1-x}N/GaN high electron mobility transistor structures grown on 200 mm diameter Si(111) substrates," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 32, no. 111, p. 21206, 2014.
- [17] J. Su, E. Armour, S. M. Lee, R. Arif, and G. D. Papasouliotis, "Uniform growth of III-nitrides on 200 mm silicon substrates using a single wafer rotating disk MOCVD reactor," *Phys. status solidi*, vol. 213, no. 4, pp. 856–860, Apr. 2016.
- [18] D. Marcon, Y. N. Saripalli, and S. Decoutere, "200mm GaN-on-Si epitaxy and e-mode device technology," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, vol. 7, p. 16.2.1-16.2.4.
- [19] L. Petti *et al.*, "Metal oxide semiconductor thin-film transistors for flexible electronics," *Appl. Phys. Rev.*, vol. 3, no. 2, 2016.
- [20] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "extreme bending stability," *Nat. Mater.*, vol. 9, no. 12, pp. 1015–1022, 2010.
- [21] J. S. Discrete, K. Nomura, H. Ohta, A. Takagi, and T. Kamiya, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," vol. 432, no. November, pp. 3383–3386, 2004.
- [22] H. Gleskova, S. W. Soboyejo, and Z. Suo, "Electrical response of amorphous silicon thin-film transistors under mechanical strain Electrical response of amorphous silicon thin-film transistors under mechanical strain," 2002.
- [23] T. Kodaira, "A flexible 2.1-in. active-matrix electrophoretic display with high resolution and a thickness of 100 μm," pp. 107–111, 2008.
- [24] P. Heremans *et al.*, "Mechanical and Electronic Properties of Thin-Film Transistors on Plastic, and Their Integration in Flexible Electronic Applications," *Adv. Mater.*, vol. 28, no. 22, pp. 4266–4282, Jun. 2016.
- [25] M. Lesecq, V. Hoel, A. L. Des Etangs-Levallois, E. Pichonat, Y. Douvry, and J. C. De Jaeger, "High performance of AlGa_N/Ga_N HEMTs reported on adhesive flexible tape," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 143–145, Feb. 2011.
- [26] S. Mhedhbi *et al.*, "First Power Performance Demonstration of Flexible AlGa_N/Ga_N High Electron Mobility Transistor," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 553–555, 2016.
- [27] N. Defrance *et al.*, "Fabrication, Characterization, and Physical Analysis of AlGa_N/Ga_N HEMTs on Flexible Substrates," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1054–1059, Mar. 2013.
- [28] D. Zhu, D. J. Wallis, and C. J. Humphreys, "Prospects of III-nitride optoelectronics grown on Si.," *Rep. Prog. Phys.*, vol. 76, no. 10, p. 106501, 2013.
- [29] T. T. Luong *et al.*, "Performance improvements of AlGa_N/Ga_N HEMTs by strain modification and unintentional carbon incorporation," *Electron. Mater. Lett.*, vol. 11, no. 2, pp. 217–224, 2015.
- [30] W. Z. Wang *et al.*, "Effect of Carbon Doping and Crystalline Quality on the Vertical Breakdown

- Characteristics of GaN Layers Grown on 200-mm Silicon Substrates," *J. Electron. Mater.*, vol. 44, no. 10, pp. 3272–3276, 2015.
- [31] P. Makaram, J. Joh, J. a. del Alamo, T. Palacios, and C. V. Thompson, "Evolution of structural defects associated with electrical degradation in AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 96, no. 23, p. 233509, 2010.
- [32] M. A. Moram and M. E. Vickers, "X-ray diffraction of III-nitrides," *Reports Prog. Phys.*, vol. 72, no. 3, p. 36502, Mar. 2009.
- [33] B. T. Liou, S. H. Yen, and Y. K. Kuo, "Vegard's law deviation in band gap and bowing parameter of Al_xIn_{1-x}N," *Appl. Phys. A Mater. Sci. Process.*, vol. 81, no. 3, pp. 651–655, Aug. 2005.
- [34] K. Rykaczewski, O. J. Hildreth, C. P. Wong, A. G. Fedorov, and J. H. J. Scott, "Guided three-dimensional catalyst folding during metal-assisted chemical etching of silicon," *Nano Lett.*, vol. 11, no. 6, pp. 2369–2374, 2011.